Design and Modelling of RF GaN Class-E Power Amplifier for Broadband Applications

Dmitriy Kupreyev

Submitted in fulfilment of the requirements for the degree of

Master of Science in Electrical and Computer Engineering

NAZARBAYEV UNIVERSITY

School of Engineering and Digital Sciences

Department of Electrical and Computer Engineering

53 Kabanbay Batyr Avenue,

Nur-Sultan, Kazakhstan, 010000

Supervisor: Dr. Mohammad S. Hashmi

Co-supervisor: Dr. Galymzhan Nauryzbayev

April, 2021

Abstract

This thesis work presents design and modelling of highly efficient class E power amplifier for broadband applications. Nearly 900 MHz bandwidth has been achieved with the center frequency at 2.0 GHz. The PAE was more than 40% over the whole range with the maximum of 82% at 1.9 GHz. The maximum gain achieved was 12.2 dB with gain variations of less than 3dB. PA was designed using 10W GaN transistor from Cree, which can operate on up to 6 GHz frequencies. Rogers RO3003 substrate was used for the device.

Acknowledgements

This master's thesis has been completed by Dmitriy Kupreyev on the spring of 2021 at Nazarbayev University. The problem statement was challenging and interesting. I would like to thank my project supervisor Dr. Mohammad Hashmi for giving me the opportunity to work on this project and for his guidance and support. Furthermore, I sincerely thank my family members and my friends for their constant support and patience.

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1 Introduction

1.1 Motivation

The number of devices in the world connected together is rising exponentially. The requirements of constant updates, higher data rates, longer battery lifetime and the race for automation of the processes are always extending the limits of technologies. In order to ensure robust performance a device should be assembled of high quality components, therefore numerous research teams are trying to improve various components of different systems, such antennas, power amplifiers (PA), transmission lines, tranceivers, couplers, oscillators, etc. PA is the one of the most crucial components of each system. It consumes the most power of the circuit, thus improving it will improve the whole system [1]. Optimized PA will result in higher efficiency of the circuit, less power consumption and longer battery life, therefore it is important to study and focus on the PAs as the performance of the majority of the systems is highly dependent on them.

1.2 Research objectives

This paper aims to develop and model efficient Class E power amplifier for broadband applications. To provide literature review on the current state of the art of class E PA. It is planned to research and apply each step of the design, such as biasing, stability analysis, load-pull, matching. The center frequency is 2.0 GHz, and the bandwidth ranges from 1.2 GHz to 2.15 GHz. Moreover, gain variation should be minimized.

1.3 Thesis outline

This master's thesis focuses on the design and development of the broadband Class E power amplifier. The work is organized as follows. In section 2 PA basics explained with relevant theory and background. Analytical equations are presented and characteristics of different power amplifier classes are discussed. In section 3 the design is proposed with relevant assumptions. Building blocks of the PA will be presented and explained. Design steps will be shown in detail. The results will be presented in section 4. Simulation of the circuit schematics will be compared to RF microwave momentum simulation. Finally the work will be concluded in section 5.

2 Theory and Background

2.1 Power Amplifiers and Performance Metrics

Radio frequency (RF) power amplifiers (PA) are the critical building block of any communication system. The areas of application include various spheres, such as radar applications, wireless communication systems, biomedicine, etc. [2, 3, 4].

As the name suggests PAs are used to amplify the power of the device. The heart of the PA is an active device, which is a transistor. Two power sources are connected to the PA, namely RF source and DC source. DC source is used as an instrument to amplify the RF signal. The simple model of the PA can be seen on the Fig. 2.1. Basically, there is an RF power source (Pac) connected to the first side of the active device and a load (Zl) connected to the second side of the power amplifier. Pdc is a power source for amplification the signal. Zin and Zout are input and output impedance of the device, which should be matched to the source and load respectively in order to avoid power loss. PA can be characterized by three main metrics, namely power added efficiency (PAE), drain efficiency (η) and gain [2, 5]. These can be characterized by the following equations:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1}$$

$$\eta = \frac{P_L}{P_{DC}} \tag{2}$$

$$G = \frac{P_{out}}{P_{in}} \tag{3}$$

Depending on the requirements and areas of applications PAs can be classified into two groups namely conventional power amplifiers and switch-mode power amplifiers. Conventional PAs include classes A, B, C and they are possess linear amplification of the signal. The active device behaves as the voltage dependent current source model. These amplifiers are defined by their relatively low PAE. The

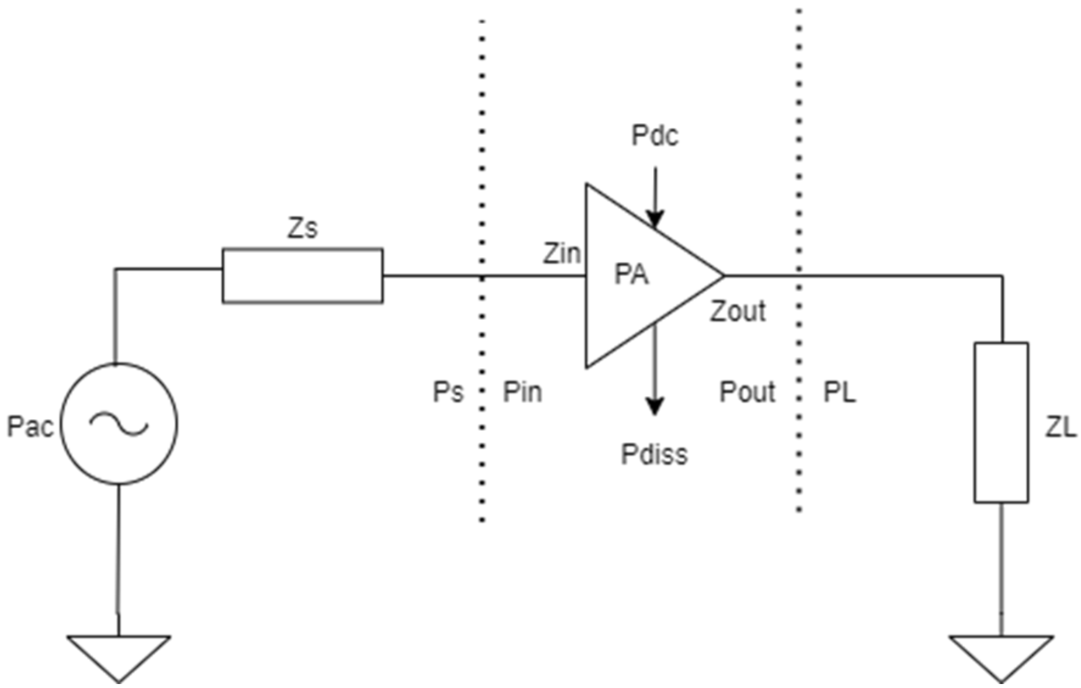

Figure 2.1: Simple Power Amplifier Circuitry

maximum PAE that can be achieved is 80%. Non-conventional PAs, on the other hand, operate in the saturation region and possess non-linear amplification. They are called switch-mode PAs, since transistor is utilized as a switch, which helps to minimize power dissipation and maximize efficiency. However, it is crucial to find a trade-off between linearity and efficiency. These PAs include classes F, E, J, etc.[2]. Theoretically, the maximum efficiency that can be achieved is 100%.

2.2 Conventional PAs

2.2.1 Class A

Class A power amplifier is the basic one. It is relatively simple to design, however the maximum efficiency that can be obtained here is 50% [6]. The biasing point is chosen at the middle of the I-V graph, see in the Fig. 2.2. The conduction

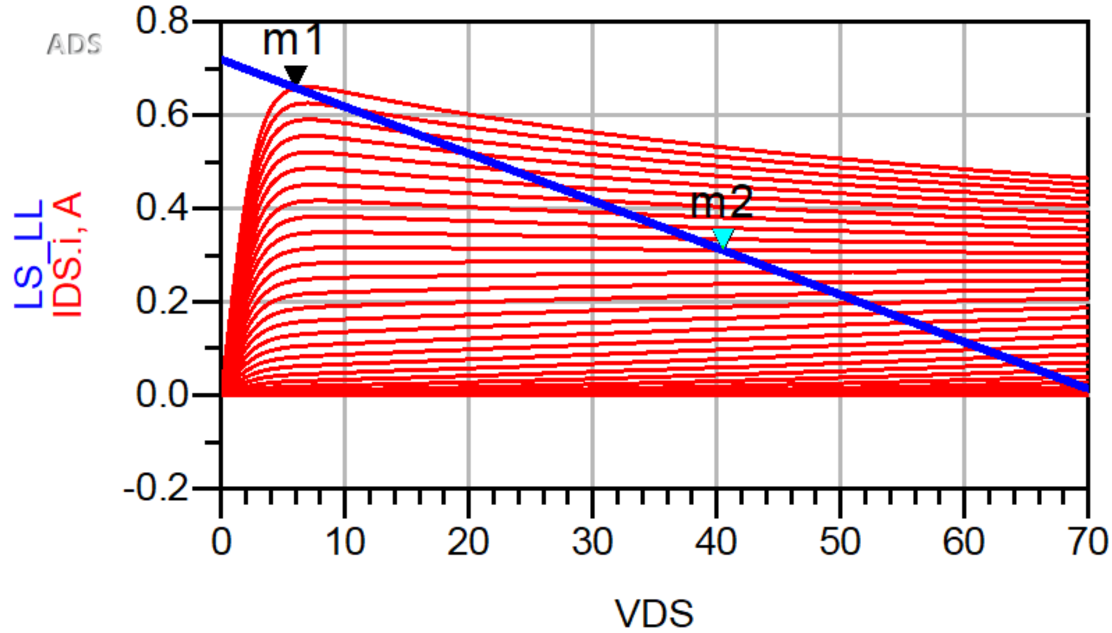

Figure 2.2: Biasing condition of class A PA

angle is 360 degree, thus the active device conducts complete RF cycle [2].

2.2.2 Class B

Class B amplifier is the device which has maximum efficiency amongst conventional topologies. The PAE in theory can reach up to 78.5%. This is due to the biasing conditions of class B [6]. The transistor is active only for the half of these cycle, hence the PA has the conduction angle of 180 degree, as shown in the Fig. 2.3.

2.2.3 Class AB

Class AB amplifier is a compromise between classes A and B. It has better efficiency than class A amplifier and better linearity than Class B amplifier. The PAE of this device lies between 50% and 78.53% [2]. The bias point is chosen

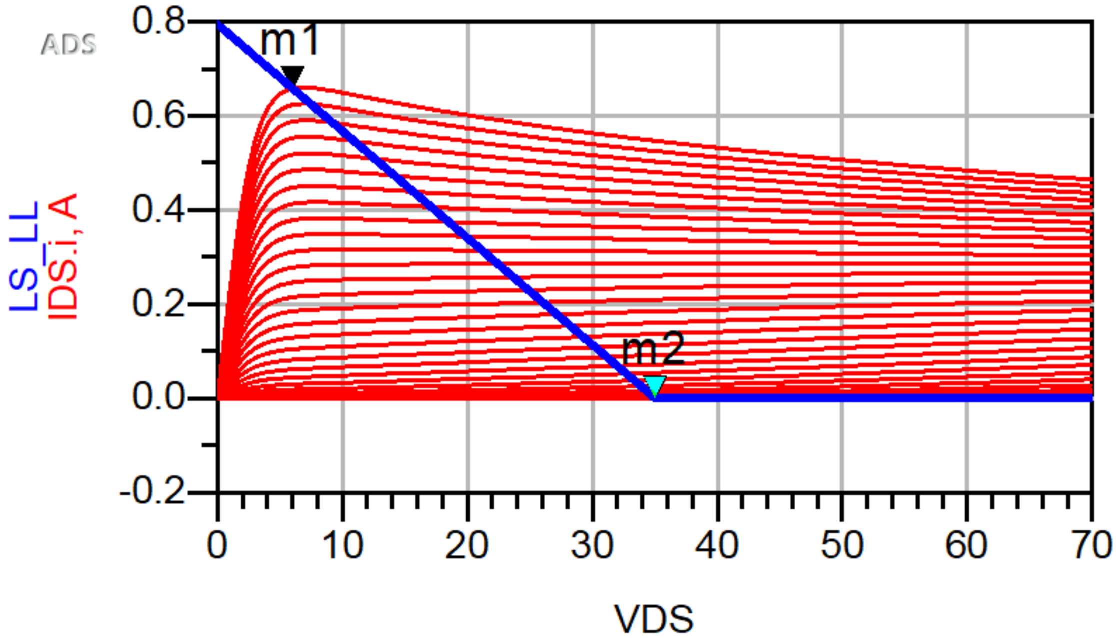

Figure 2.3: Biasing condition of class B PA

between bias points of classes A and B thus conduction angle can be anything between 180 and 360 degrees. The biasing condition of class AB can be seen on the Fig. 2.4.

2.3 Switch-mode PAs

Switch-mode power amplifiers have biasing point in saturation or non-linear region region. The active device behave like a switch and hence theoretically 100% efficiency can be obtained. Design of switch-mode PAs can be though as waveform engineering. The goal is to achieve sharp transition from maximum to minimum values on the I-V graph. Generally, the wave-forms in switch-mode PAs resemble squared pulses, as can be seen on the Fig. 2.5. This minimizes dissipated power and hence maximizes the efficiency. The examples of switch-mode PAs are PAs of

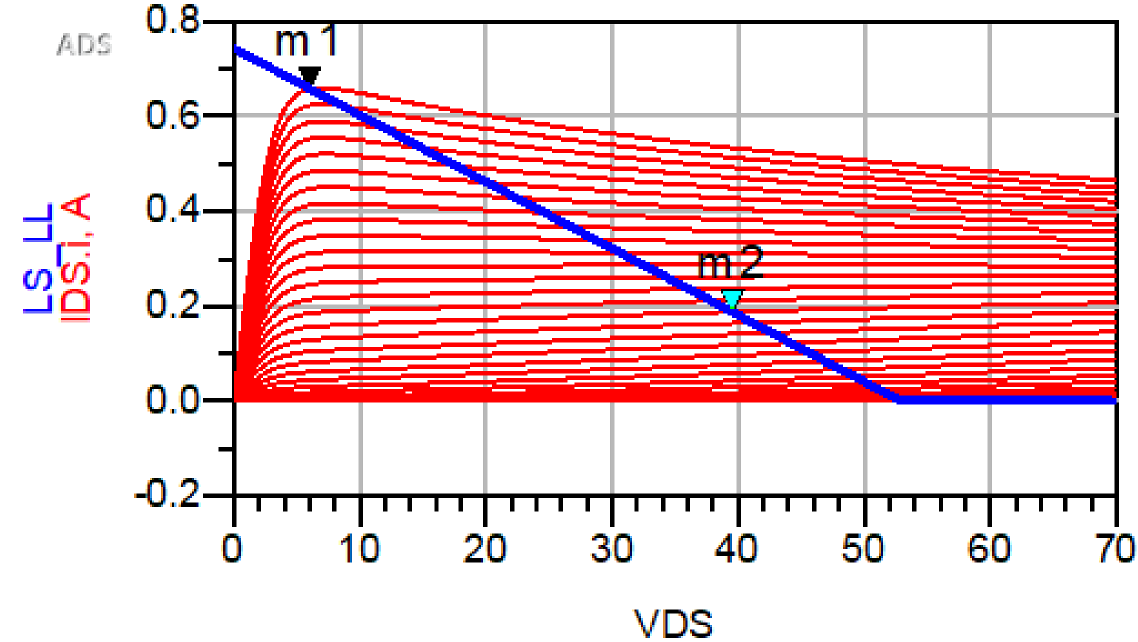

Figure 2.4: Biasing condition of class AB PA

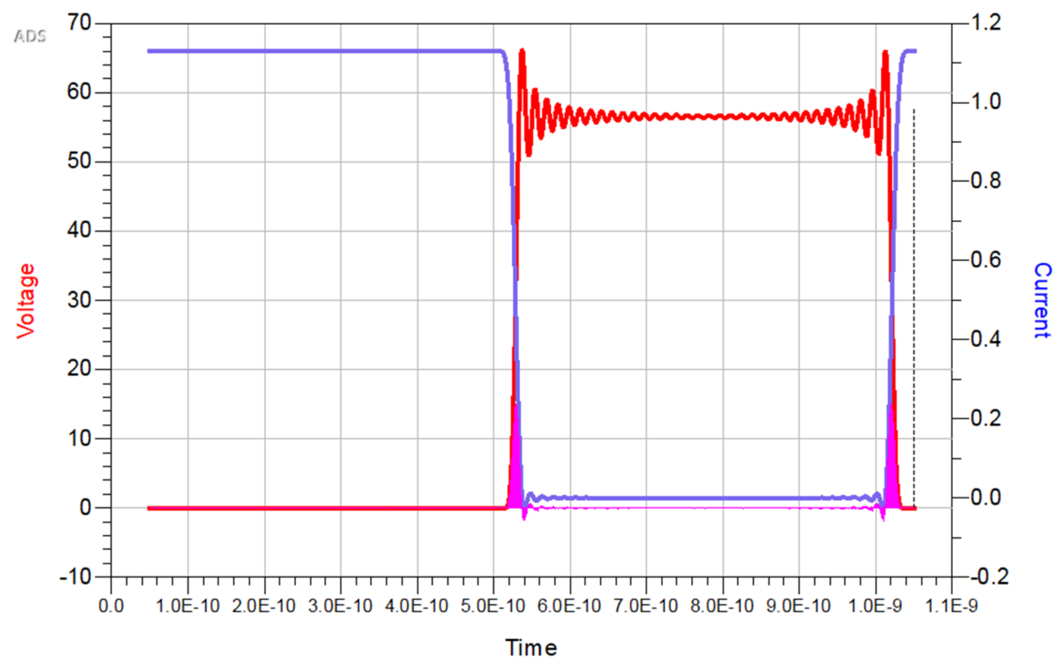

Figure 2.5: Switch-mode PA waveform example

Class F, and E.

2.3.1 Class F

Class F PA has similar characteristics as class B amplifier. However, to provide higher efficiency harmonic termination of the load network are introduced. This network resonates not only at operational frequency, but also at one or several harmonic frequencies [2]. In theory it can control infinite number of harmonics and can achieve 100% efficiency, however in real-life scenario it is usually challenging to control more than 4th harmonics.

2.3.2 Class E

Class E in theory can provide 100% efficiency, however in real life with all the distortion and component losses the maximum efficiency is usually around 80%. This PA is biased in the saturation region. It differs from other topologies by the approach it uses to deal with parasitics. In class E PA these are made as a part of the system, particularly of the tuning circuit [2]. For broadband application a reactance compensation technique is frequently utilized.

2.4 State of the Art Class E PAs

Class E power amplifier is defined not only by the operation point (Q point), but also by the load network of the device which is used as a tool for waveform engineering. The basic load network can be seen in the Fig. 2.6, where $C2$ is parasitic capacitor due to transistor and L_2 and C_3 connected in series are tuned at the fundamental frequency [7].

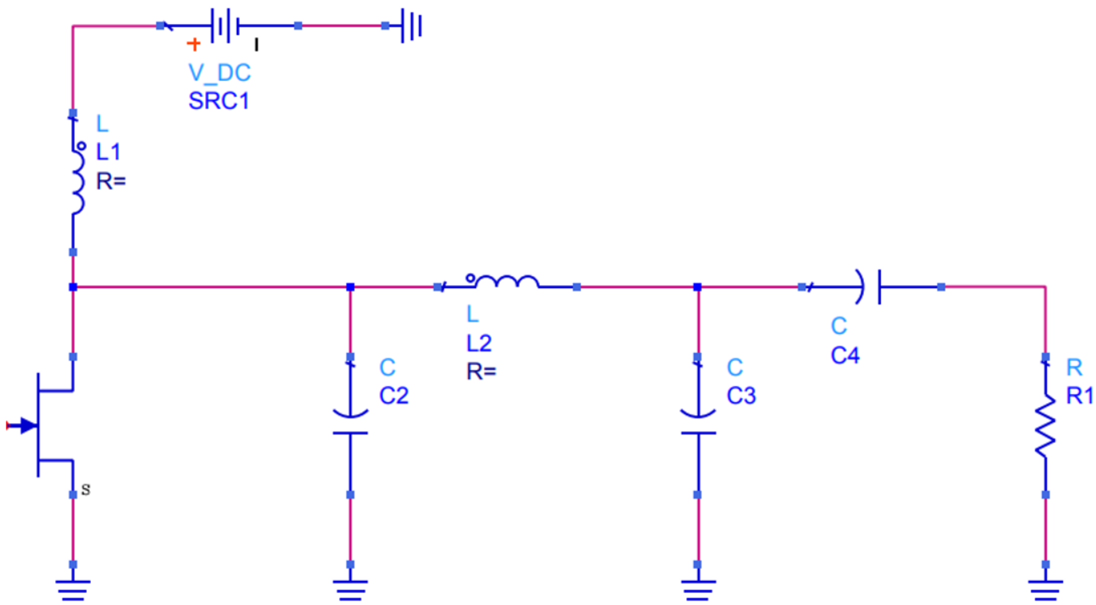

Figure 2.6: Load network of Class E PA

Different variations of Class E PA design are proposed in the last decade. The focus is set to wide broadband design or high efficiency designs. These two can be combined together, however generally it is much more easier to achieve high efficiency on the narrow bandwidth. High efficiency will help to solve the main problem in the circuits, namely high power consumption, which is mainly due to the power consuming device, i.e. power amplifier [8]. Reduction of power consumption will increase the battery life of the device.

Different approaches have been implemented to address these issues. In [8] authors propose Class E PA with tunable output matching network, which was realized using band-pass filter. The frequency band can be tuned on the range between 1 and 2.55 GHz, while having the PAE of not less than 50%. Moreover, the gain variations are less than 3dB, with the power output ranging from 40 to 41.5 dBm. For the tuning purposes varactor stack diode is utilized. Varying bias voltage in the device, it is possible to change the effective capacitance and affect the center frequency. Overall the designed device can provide up to 73% efficiency at a certain frequency. A sequential load pull approach has been implemented in [9]. Broadband Class E PA has been realized covering the bandwidth of 1.8-2.7 GHz. PA was designed using GaN HEMT transistor from cree, however the proposed methodology can be successfully applied to any device technology, such as GaAs, LDMOS, etc. The peak PAE acheieved at 2.21 GHz and is equals to 65.2%. Overall, the efficiency is greater than 48% over the whole band. The design can be successfully used for LTE application. Another Class E PA has been introduced in [10]. In this paper a dual band PA is proposed. The bandwidth at each frequencies is narrow, To realize the device a load compensation circuit has been proposed. The goal was to terminate first and second harmonics and simultaneously match impedance of the device to the load. As a result the circuit demonstrates good PAE of 74.9% and 75.9% at 1.72 GHz and 2.14 GHZ respectively. The highest efficiency for Class E PA have been reported in [11]. However, despite 90.3% efficiency the device operates at 1 MHz and has narrow band, which makes it not favourable in terms of practical applicability. Nevertheless, it can still be used for medical purposes. Another example of class E PA for medicine is presented in [12], where PA is used in inductive link to drive the power to the medical implants. In this scenario, additional factors, such as losses due to human body affect the efficiency of the system. The achieved power transfer efficiency was 25% at a distance of 6 mm. Even though the most preferred transistor topologies for PA are GaN and GaAs, CMOS based class E are also reported in this domain. In [13] single band Class E PA is designed

Table 2.1: Class E PA literature review summary

$Source$	$Freq.$ (GHz)	$Year$	PAE %	P_{in}/P_{out} (dBm)	Transistor Tech.
[15]	3.25	2002	90 (drain)	15 / 24	pHEMT
[16]	7.5	2007	67	29 / 38.3	AlGaN/GaN
[17]	8.5	2007	80	15 / 25.8	GaAs pHEMT
[18]	2.14	2007	70	30 / 43	GaN HEMT
[19]	2.67	2009	60.40	14 / 22.6	CMOS 90 nm
[1]	0.1	2010	86 (drain)	- / 51.61	Silicon LDMOS
[20]	0.2	2015	85.8 (drain)	28 / 42.5	GaN FET
[21]	1	2016	80	- / 43	GaN FET
[22]	1.8	2020	65 (drain)	28 / 42.3	GaN HEMT
[23]	0.155	2008	74 (drain)	28 / 39	LDMOS
[24]	0.8	2009	80.6	35 / 46.9	GaN HEMT
[25]	1.8	2019	79	27 / 39	GaN HEMT
[26]	3.2	2014	74	23 / 38.3	GaN HEMT
[27]	2.85	2009	73	34 / 41.2	GaN HEMT
[28]	2.14	2012	70	40 / 43	GaN HEMT

on 5.3 GHz, while providing the PAE of 42%. These design is one of the most compact reported. In addition, the effects of the various parameters, such as duty ratio, on the performance of class E PA, have also been investigated and reported. [14]. Another designs, with the performance results are reported in Table 2.1.

Based on systematic literature review, which is summarized to Table 2.1, following conclusions have been made:

- GaN HEMT is the most frequent device utilized in switch-mode PA design. The reason for that is its commercial availability, availability of the detailed software model, tolerance to high temperatures and high breakdown voltage.

- Designed frequencies are usually below 12 GHz, with the most focus on 0 to 4 GHz range.

- The following broadband design techniques can be emphasized as popular approaches:
  - Reaction compensation technique: Load network designed in such a way that it is not only matches impedances but also terminates the harmonics, moving multiples of f_0 to the right edge of the smith chart
  - Mining methods based on I-V curves: serious analytical work conducted to obtain values of lumped elements in the output network. For these purposes MATLAB is frequently used.
- Different filters and Kuroda transformations are used for output network design.

3 Design and Modelling of PA

Advanced Design Systems (ADS) software is utilized for the development and modelling of the power amplifier.

3.1 Proposed Design and Requirements

Class E PA is modelled with microstrip transmission lines based on Rogers RO 3003 substrate with the dielectric constant of 3.0. The conduction layer is made up of copper with the thickness of 35 micron. 10W GaN HEMT transistor is used as an active device. It can be used for operations below 6 GHz frequency. GaN HEMT is a good candidate for broadband amplifiers. It also can be used for radio, cellular infrastructure, linear amplifiers [29]. The device is designed to operate at 2.0 GHz frequency. The device is unmatched, therefore it is required to measure the optimum input and output impedances for proper matching. In addition, in order to avoid any signal interruptions it is important to ensure unconditional stability of the circuit.

3.2 Biasing

Class E power amplifier should be biased in the saturation non-linear region. The rest of the Class E characteristics achieved by proper load netowrk and harmonic control. To examine DCIV characteristic of the device FET Curve Tracer tool from ADS is used, as shown in Fig. 3.1. VDS is a drain source voltage which is DC supply. It is swept from 0 to 58V in the analysis. Although the device is 28

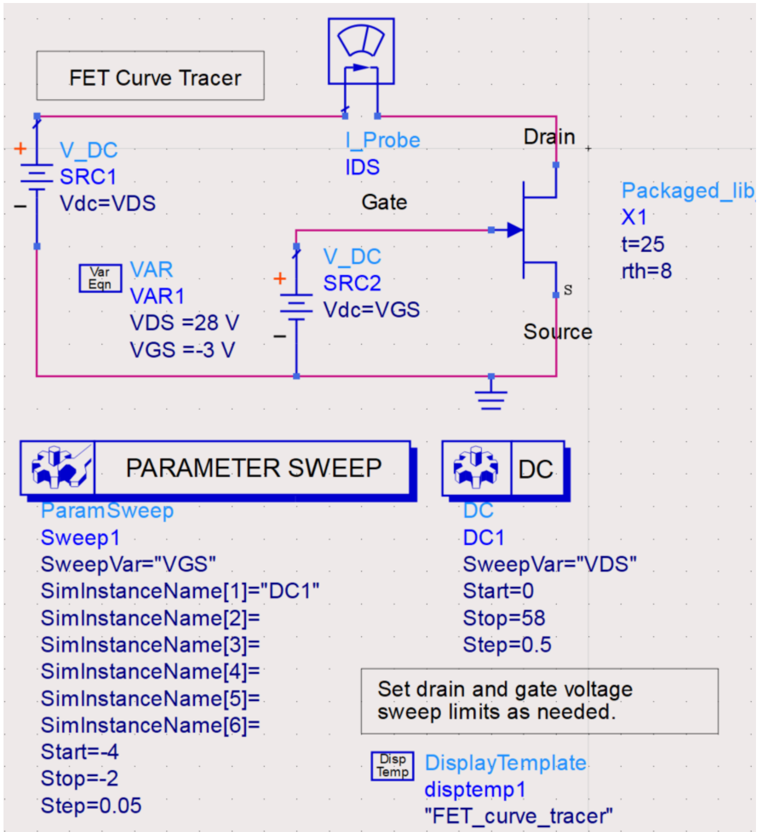

Figure 3.1: PA DCIV Analysis Setup

V, it always recommended to sweep two times of your desired voltage, since load line is utilized. VGS is a gate source voltage, which swept from -2 to -4 in the analysis. This analysis is required to obtain the initial view of the system. It gives the overview on waveform shapes, values of current, efficiency and power dissipation before the harmonic suppression or matching is applied. The results of the curve tracer can be seen in the Fig. 3.2. The operating voltages of the system are 28V and 2.9V respectively.

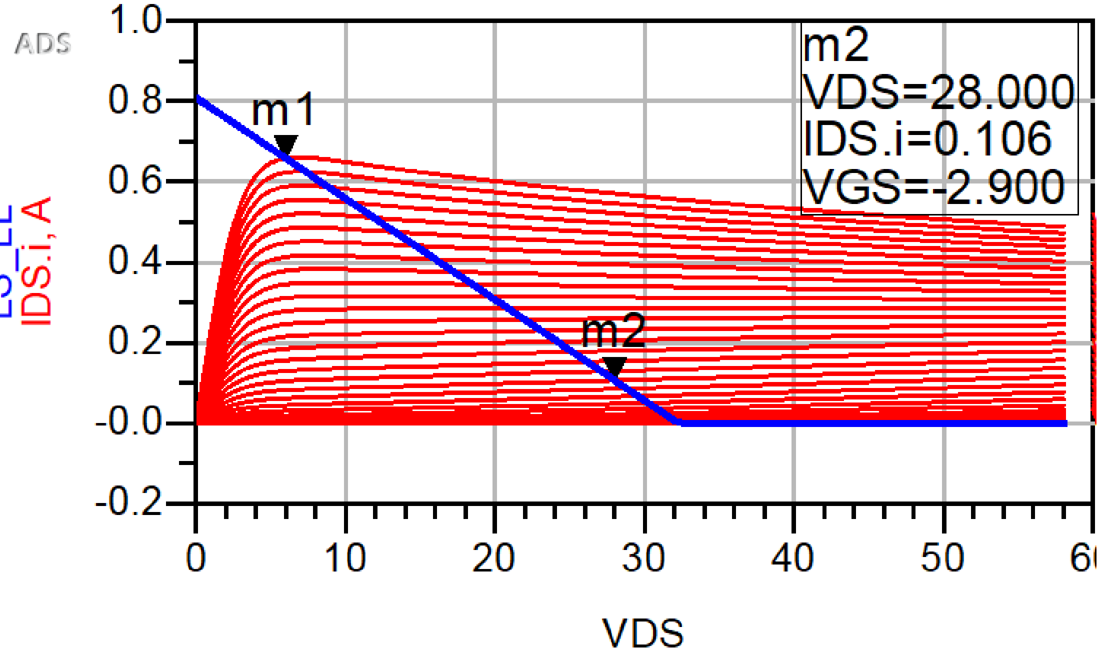

Figure 3.2: Biasing point of proposed Class E PA

3.3 Stability

Stability is another crucial parameter to consider during RFPA design. Unstable device will produce negative effects on the performance at desired frequency, thus it is required to stabilize the device on the desired frequency range. An LC network is usually used as a stabilizing tool. In some cases a resistor can be utilized. The stability circuit setup can be seen in the Fig. 3.3.

In order to achieve unconditional stability two conditions should be satisfied. $K > 1$ and $|\Delta| < 1$, where K and $|\Delta|$ are expressed as follows [30].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{12}S_{21}|} \tag{4}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5}$$

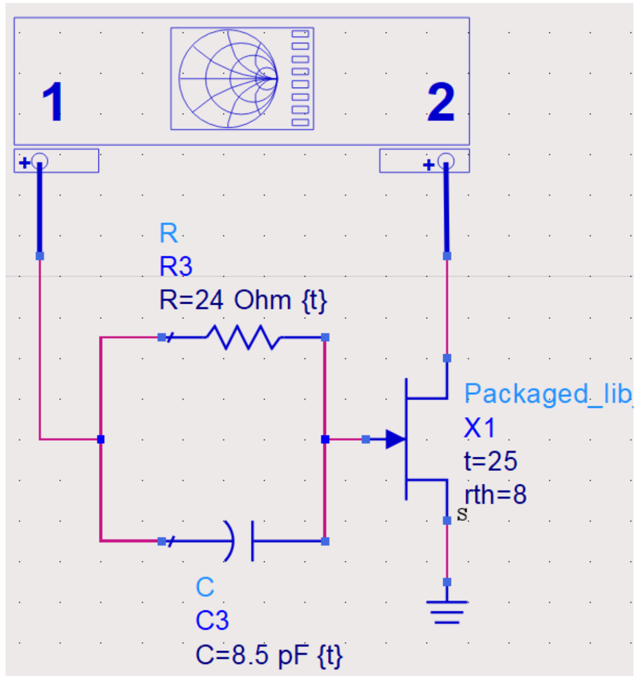

Figure 3.3: Stability Analysis Circuit

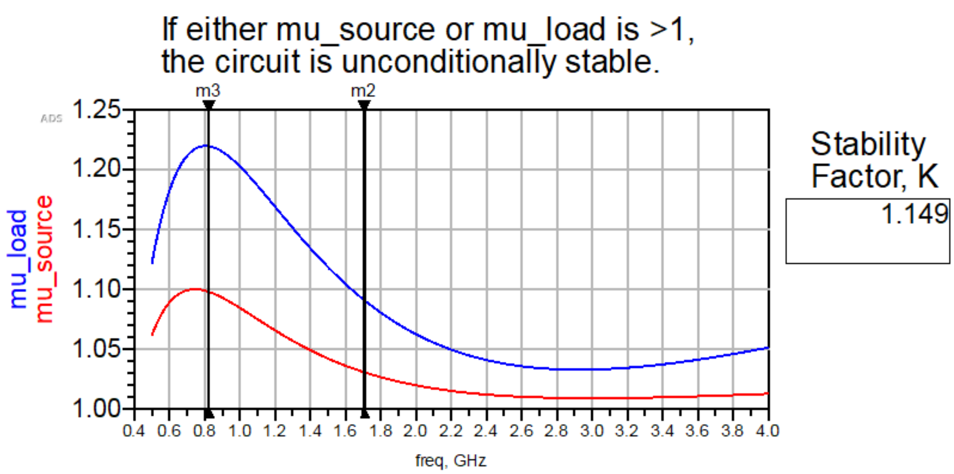

Figure 3.4: Stability Analysis Results

The results of the stability analysis can be seen on the Fig.3.4. The system is unconditionally stable over the desired frequency range. In addition, it is also important to consider the maximum gain, that can be achieved at these conditions. In this step the maximum gain was more than 12 dB over the whole range.

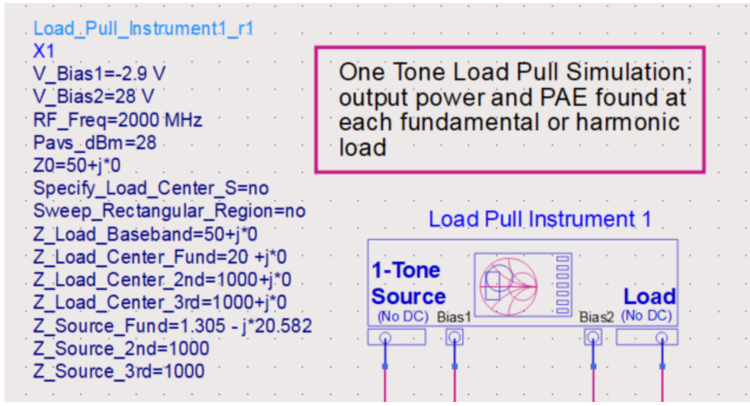

Figure 3.5: Load Pull Instrument

3.4 Load-Pull

Load - Pull is a crucial procedure in PA design. The primary objective of the load - pull is to extract the conditions under which the optimum performance of the device can be achieved. This is realized by applying different terminal impedances at a specific bias and frequency [31]. The load-pull setup is on the Fig. 3.5. The isntrument is connected to the device under test (DUT). Operating conditions of the DUT are set on the left, where driving power set to 28 dBm, bias voltages are -2.9V and 28V respectively and 2nd and 3rd harmonics are open-circuited. Before the analysis it is also important to deactivate inductors and capacitors in the instrument as shown in the Fig. 3.6.

By varying applied impedance optimum values for input and output impedance of the device are obtained. The final contours and the results are shown in the Fig. 3.7. The device can be optimized according to either power output or PAE level. This design has been optimized according to maximum PAE. Device has the potential of achieving 84% PAE.

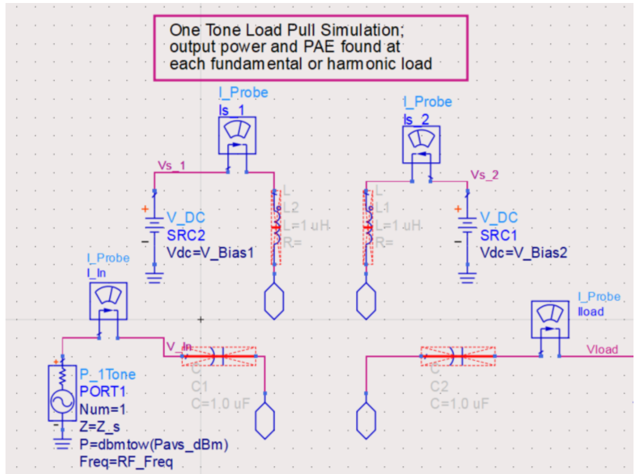

Figure 3.6: Load Pull Instrument Schematics

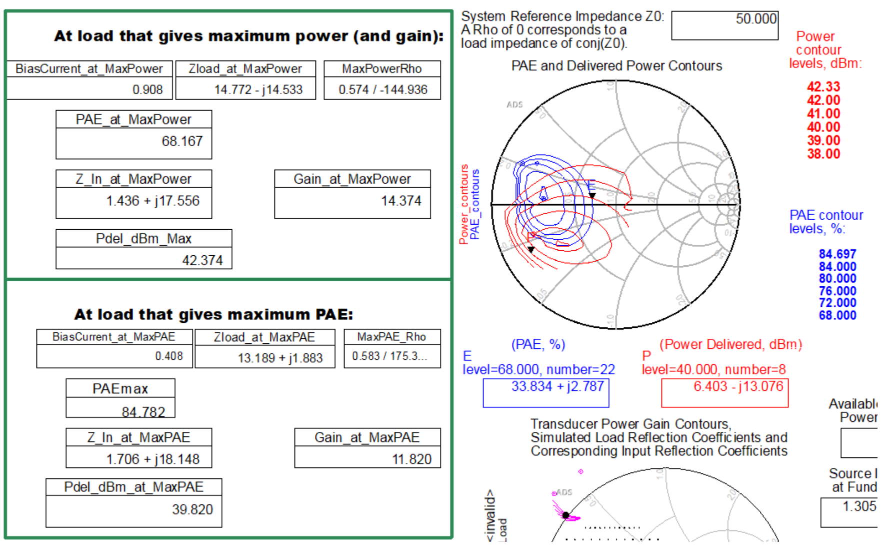

Figure 3.7: Load Pull Contours

3.5 Matching

From the load pull analysis it was figured out that input port should be matched to 1.706+j18.148 ohm at the input of the device, while the load impedance should be matched to 13.189 + j1.883 ohm. For this purpose distributed matching network has been chosen as the best option. The reason for that is parasitics that appear when using lumped elements. Moreover, wider bandwidth can be obtained using

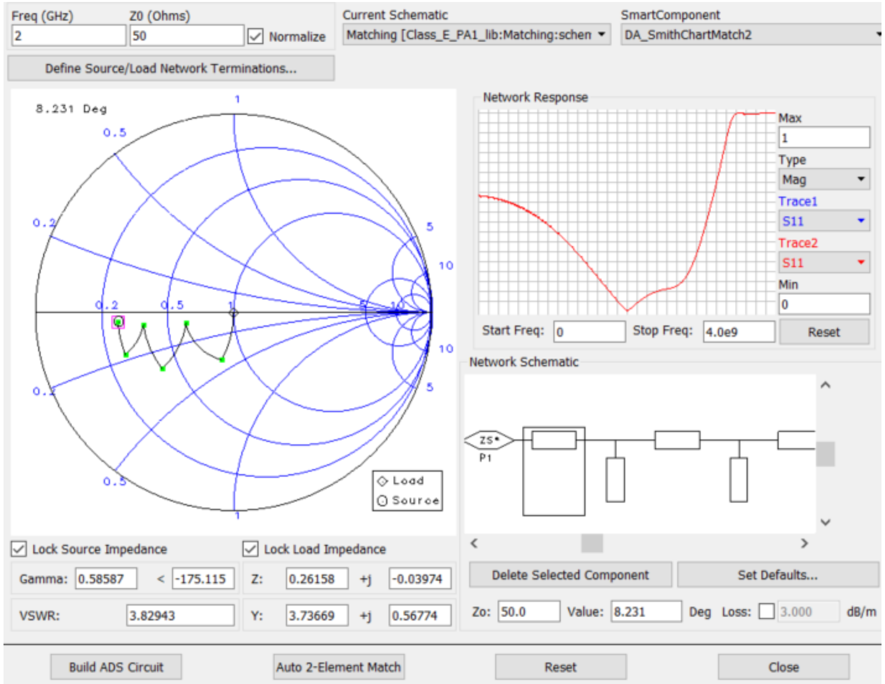

Figure 3.8: Matching utility

Figure 3.9: Optimization setup

distributed type network. Smith chart utility has been chosen as a first step as can be seen in the Fig. 3.8. Then resulting network has been optimized to achieve broadband operation. Optimization setup is shown in the Fig. 3.9, goals were to optimize the geometry of the network until the moment when dB(S(1,1)) < -11 and dB(S(2,1)) > - 0.7.

4 Results and Discussion

The schematics and the final result of the proposed model is on the Fig. 4.1. The bias tee is made up of butterfly stub for the purpose of wide bandwidth. By-pass capacitors on the bias tee are used for preventive measures, in case if RF signal somehow leaks to the DC supply. The design is based on the Rogers RO3003 substrate due to its low loss characteristics. The results of the simulation is shown on the Fig. 4.2. The model demonstrates PAE of higher than 40% from 1.2 GHz till 2.15 GHz. Moreover, higher than 60% PAE can be noted in the regions 1.35 GHz and 1.55 GHz and 1.8 GHz to 2.1 GHz. The peak PAE of 84% is recorded at 1.9 GHz, which is an excellent performance for switch mode PA. The gain of the PA is within the range of 10-12 dB with the variations of less than 3 dB. However, it starts declining significantly at 2.05 GHz. The maximum gain and power output are recorded at 1.45 GHz, where gain is 14.2 dB and the power output is 42.2 dBm.

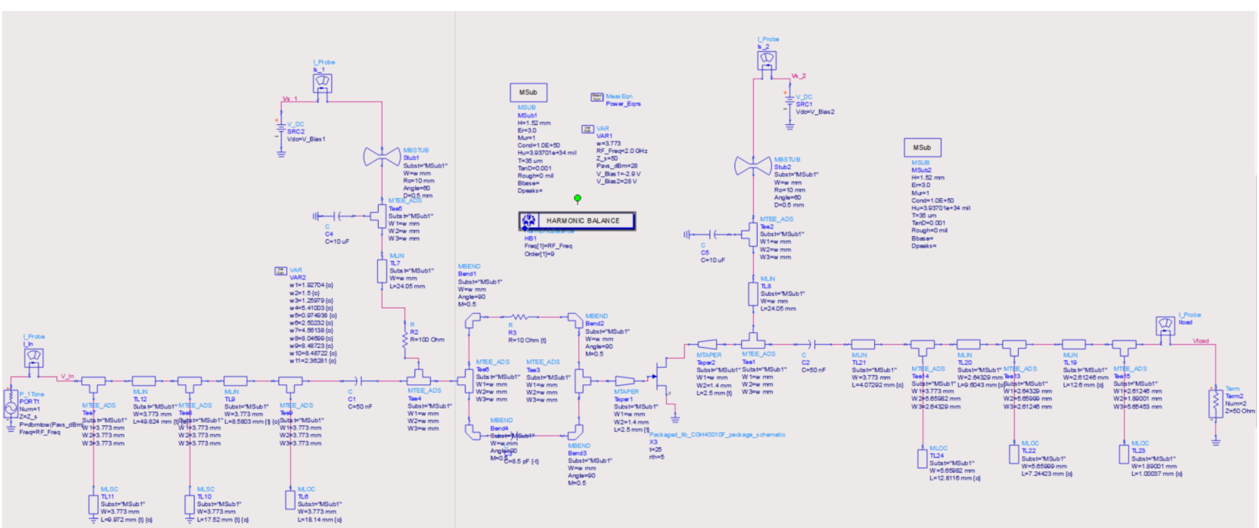

Figure 4.1: Proposed Circuitry

The schematics then was converted to layout representation in order to an-

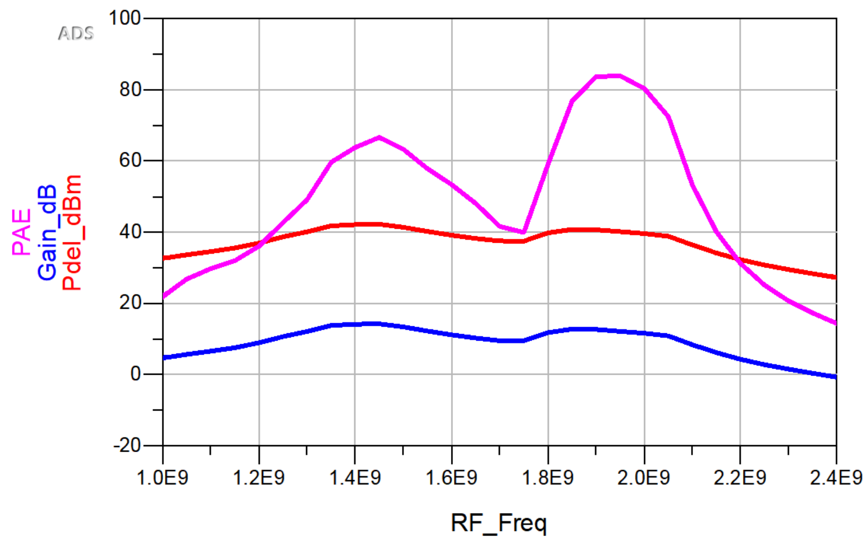

Figure 4.2: PAE, Gain and output Power

alyze the momentum microwave simulations. The layout representation is in the Fig. 4.4. The "layout" view was chosen for the simulation view, Fig. 4.5. The corresponding simulation results are in the Fig. 4.3 A slight deterioration of the performance of the model can be observed. This is due to the additional losses, which are introduced by the momentum simulations, as they are closer to the real life scenario as compared to schematics simulation, where components are nearly ideal. The maximum PAE achieved in momentum simulations was 82 %. Overall, both simulations in a good agreements and obey the same waveform pattern. However, it is important to access the device in a real-life scenario.

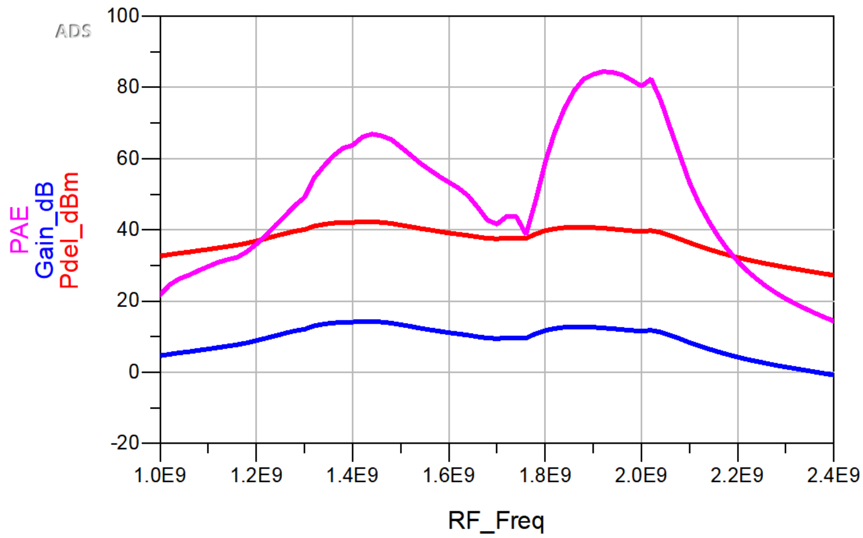

Figure 4.3: PAE, Gain and Output Power (layout)

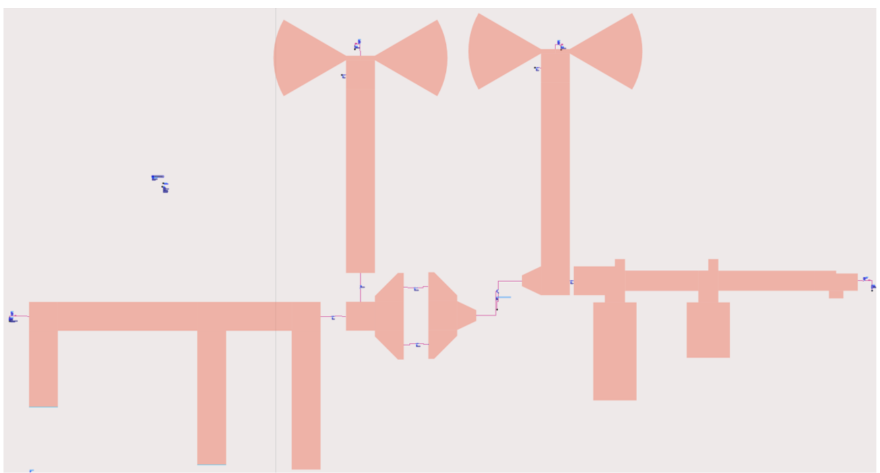

Figure 4.4: Layout representation

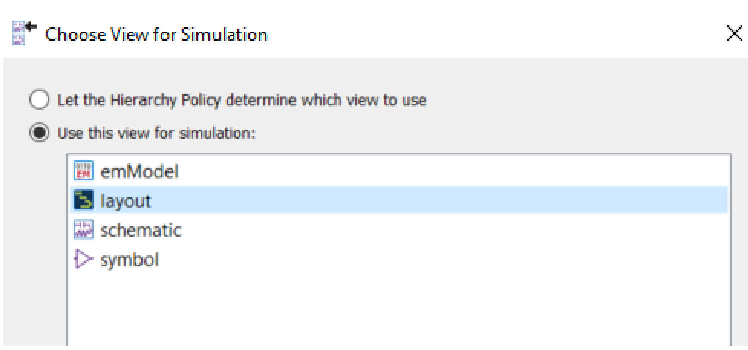

Figure 4.5: Simulation view

5 Conclusion and Future Work

This work reported design and modelling of highly efficient class E power amplifier for broadband applications. A 10 W GaN transistor from cree was used as an active device. PA was modelled on Rogers RO3003 substrate. Device operate at 2.0 GHz frequency and is driven by 28 dBm power input. Butterfly stubs are used for broadband bias - tee. An RC network is used to ensure unconditional stability of the PA. A maximum of 82% PAE have been achieved during microwave momentum simulations. Overall, the device have more than 40% PAE over the frequency range of 1.3 GHz to 2.15 GHz. The gain variations are less than 3 dB. Further work will include validation of the design in real-life, by manufacturing and measuring the device. In addition, before the manufacturing it is required to study and apply design techniques to address the PAE on the range of 1.5 GHz and 1.8 GHz.

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