NATURAL VOLTAGE BALANCING IN HYBRID FCC MULTILEVEL CONVERTER

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Submitted in fulfillment of the requirements for the degree of Masters of Science

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December 2016

Declaration

I hereby, declare that this manuscript, entitled “Natural Voltage Balancing in Hybrid FCC multilevel converter”, is the result of my own work except for quotations and citations, which have been duly acknowledged.

I also declare that, to the best of my knowledge and belief, it has not been previously or concurrently submitted, in whole or in part, for any other degree or diploma at Nazarbayev University or any other national or international institution.

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Acknowledgements

I want to express our great appreciations to project supervisor Dr. Alex Ruderman, for his useful recommendations and assistance during the development of this work. In addition, I would like to express my deep gratitude to the second supervisor, Dr. Yakov Familiant for his patient assistance required during the simulation process. Finally, I would like to thank school of Engineering for the provided access to internet databases.

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Abstract

Multilevel converters are frequently used in high and medium power applications. The challenge associated with successful operation of multilevel converters, is the voltage balancing. There are two major techniques dedicated to deal with the voltage balancing, namely: natural and active voltage balancing techniques. Natural balancing is more preferable, since it does not require sensing and in-time controlling equipment. Accepted methods of natural balancing investigation is based on the manipulations of the frequency components. This methods imply heavy computations and not general solutions. In contrast, time-domain analysis, proposed in this paper, produces simple closed-form solutions and requires simple mathematical calculations. The project is focused on performing time-domain analysis in order to investigate natural balancing characteristics of Combined H-Bridge Flying Capacitor Converter (HFCC) converter, for which natural balancing investigations is not reported in literature yet. Modulation strategy was obtained using Matlab software simulation and were implemented with PWM control and Matlab Simulink interface. Obtained results have demonstrated the fast balancing rates with natural balancing, for the majority part of modulation range. In addition, produced analytical equations, that describe voltage balancing dynamics do not require heavy computational effort and could be calculated online.

1. Introduction

Currently there is a great power demand in industry, and this demand is constantly growing. Therefore, both technically and economically efficient power conversion techniques have become a very popular topic among researchers. Multilevel converters present a well-established and industry accepted solution for high quality demanding, medium and high voltage applications. Medium power application of the multilevel converters are mainly limited by the field of the medium power drives [1]. On the other hand, there is variety of high power applications for multilevel converters including: industrial fans, pipeline pumps, power compensators and renewable power integration [2]. For instance, in order to achieve controllability and power transfer capability of the power multilevel converters are used to provide reactive power compensation in response to grid voltage transients (e.g. sag, swell, harmonics) [3].

Multilevel converter - is a power conversion system that is composed from an array of semiconductors, such as IGBTs, and capacitive voltage sources. By properly connecting and controlling them, voltage signals with adjustable amplitude and frequency could be produced [1]. This is achieved by specific connection of the capacitive voltage sources to the load, which require a proper selection of the switching states of the semiconductor devices.

Fig 1.1, demonstrates the classification of multilevel converters. There are plenty of different types of multilevel converters. These converters have become

widespread and popular because of several advantages over their two-level counterparts [3]. For example, they can operate at higher voltage levels using the same medium voltage semiconductor devices. In addition, reduced harmonic content, that provides higher voltage quality, is achievable in multilevel converters. Finally, they required less electromagnetic filtering, which sufficiently reduces the size of converter.

In order to operate properly as expected, multilevel converters need a voltage balancing of capacitor voltage sources. This balancing could be either natural or active. Active balancing requires online decision-making circuits with real-time capacitor voltage measurements [4]. Whereas, in natural voltage balancing technique, balancing is achieved by selecting a proper switching pattern and there is no need for additional voltage or current sensors [5].

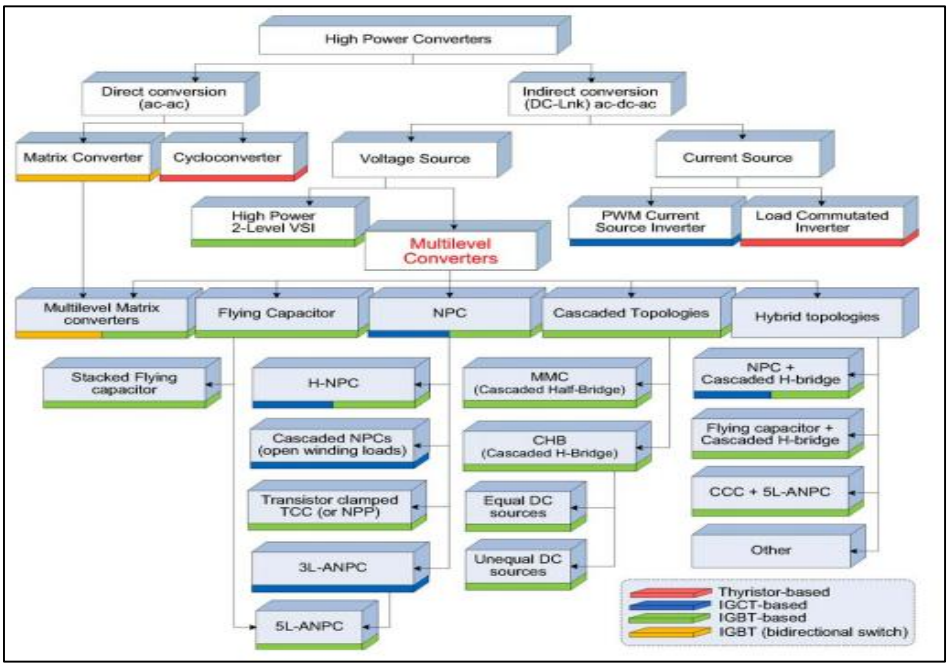


Fig1. 1: Classification of the multilevel converters [3]

Positive characteristics of multilevel converters along with advantages brought by the natural voltage balancing became a motivation to conduct presented research. The main objective of the given research is to investigate natural balancing characteristics of the single-phase multilevel converter, namely 5–level combined H-bridge Flying Capacitor Converter (HFCC). There were previously no reported attempts to analyze natural voltage balancing characteristics of selected converter topology.

The expected deliverables of the project are: optimal switching patterns, producing maximally rapid natural balancing and simple equations of capacitor sources voltage waveforms, describing average natural voltage balancing characteristics of chosen multilevel converters. Produced switching patterns are expected to be practically applicable with corresponding type of power converters without the cost of active balancing, while obtained voltage equations are expected to be helpful for natural balancing characteristics and suitability analysis for every individual application of the examined converters. Moreover, obtained strategies need to be scalable for increase in number of voltage levels for selected converter type.

2. Literature review

Multilevel voltage source converters (VSCs) have gained a significant interest in medium and high power applications, as mentioned earlier. The most popular topologies of multilevel converters are the multimodular converter, the modular multilevel converter, the diode clamped converter or neutral point clamped (NPC) converter, and flying capacitor converter (FCC).

FCC has attracted significant interest because it can be easily extended to converters of a higher number of levels (n>3), in comparison with another popular converter – NPC. This is implied by the fact that it is easier to achieve capacitor voltage balancing in FCC converter of a high number of levels. In addition, FCC could be applied in DC-DC applications, such as plug-in hybrid electric vehicle as it provides high efficiency and good quality of output voltage [6]. However, according to [7] one of the problems associated with traditional FCCs is its inability to control the real power flow between AC and DC sides on its own. This is due to the fact that the capacitors need to be charged and discharged equally and it is only achievable when the power angle is 90^{o}.

Moreover, majority of the authors mentioned in this section agree, that there are some issues that need to be considered in the design stage of the converter, including: initial FCC charging process, capacitor voltage ripples and voltage balance. Voltage ripples play significant role in the sizing of the capacitors used

in the design of FCC. Currently there is a practical interest to reduce the capacitance values of capacitors and consequently the size of the converter. Besides that, using a small capacitance values allows to use a thin-film capacitors, which have a lower losses and provide higher reliability as compared to conventional capacitors. On the other hand, small capacitors can introduce higher levels of the voltage fluctuations that may spoil the integrity of converter. Nevertheless, proper voltage - balancing method may ensure less voltage ripples and ensure safe operation of the power devices [8].

To make FCC with natural voltage balancing and applicable in practice, the challenge is to design proper switching patterns with corresponding modulation strategies that assure convergence and fast natural voltage-balancing dynamics [9].

Reasonable natural balancing rates were already reported for different types of multilevel converters, including FCC [10], NPC [11], Stacked Multicell FCC [12], etc. However, because of imperfections including finite rise and fall times of capacitor voltages on switching period, non-ideal semiconductor devices and asymmetry in switching times, balancing rate might significantly slow down. Such converters could not be used for any practical applications without the improvement of balancing stability margin. Moreover, inductance dominated loads typically require not practically acceptable amount of time for natural balancing.

There are methods that can accelerate the natural balancing characteristics of the converters. For example, balance boosters described by [13] - passive elements with low impedance at the sampling frequency. Another method described by [11] - to add zero-sequence voltage component to the load voltage.

Active balancing is another major solution for the voltage deviation. Common active balancing methods are based on the predictive control described by [14] and [15], dead-beat control [16] and rule based approaches [17]. In [18] they have proposed to control converter balancing based on continuous selection of the switching sequences and therefore minimize the deviation of capacitor voltage from desired value. Despite the fact that this method has proved its efficiency, it requires voltage measuring and decision – making equipment. In [19], [20] authors proposed similar voltage balancing schemes. Proposed methods require current and voltage sensors, low – pass filter and PI controllers that increase the overall cost of the system.

The main advantage of the active balancing is the fast balancing of the load voltage. However, it requires hardware for continuous voltage measurements and computational effort that are associated with additional cost of the system. Furthermore, active balancing becomes redundant and even harmful for steady – state conditions operation [21].

From these it is clear that natural voltage balancing is more preferable for multilevel converters. The common method to perform natural balancing analysis

is frequency domain transformation. Such approach is applied in the works of [22] and [23]. Mentioned authors utilize the Double Fourier Series, alpha-beta transformation and Bessel function coefficients in their investigations. These concepts make the methods computationally difficult and unsuitable for online application. Moreover, these works did not investigate natural voltage balancing on the whole modulation range. On the other hand, time domain analysis provides possibility to determine both, simple closed-form solutions, utilizing simple mathematical approach, and data required for the analysis such as dependence of damping time constant and oscillation frequency on the modulation index. In addition, time – domain energy based approach investigates the natural balancing by studying energy dissipation of the capacitor unbalance [24].

3. Methodology

3.1. Method selection

The major parameters that characterize converter are its: capacitances, load inductance and resistance, switching frequency and normalized voltage command D for DC PWM and modulation index M for AC PWM. In order to investigate the natural balancing in the converter, it is required to determine the dependence of the capacitor voltage's balancing average dynamic equations, including oscillation frequency and damping factors (time constants), on the aforementioned parameters. The method of the natural balancing investigation was selected based on the several constraints. The priority was to find simple closed-form representation of voltage waveform equations. In addition, such factors as reduced computational effort and versatility of obtained solution were taken into account. These requirements applied to the reviewed literature lead to the selection of the energy-based time domain analysis method described in [24].

3.2. HFCC converter operation

The 5-level HFCC converter is the combination of 3-level FCC converter in series with the H-bridge capacitor cell (Fig. 3.1). 5-level means that the converter can produce five nonnegative voltage levels on the load.

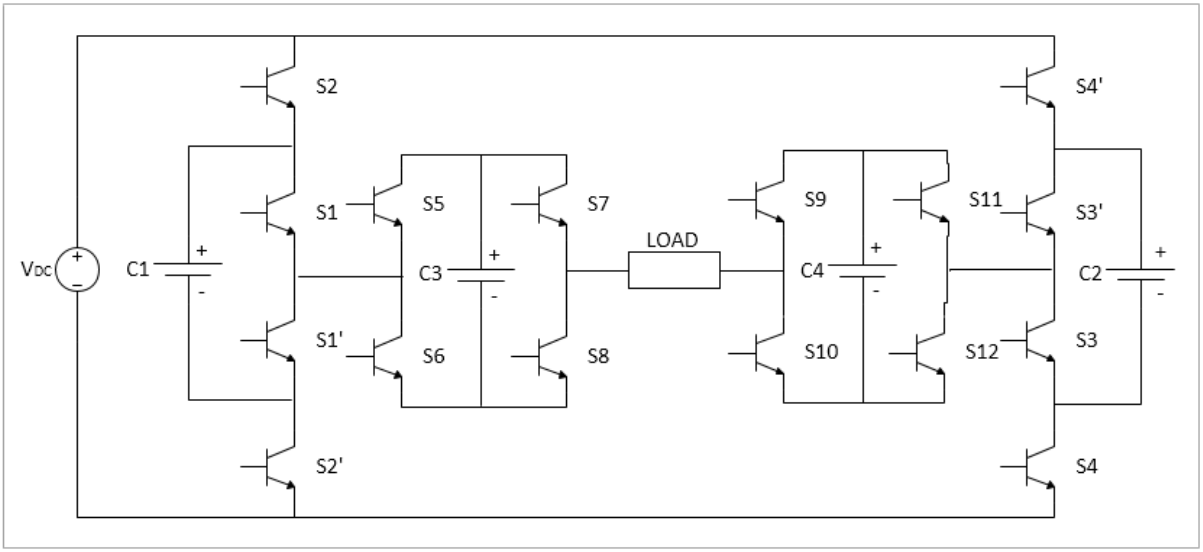


Fig3. 1: Circuit diagram of HFCC multilevel converter

Following multilevel converter topology has 16 controllable transistors (switches) with 8 pairs of the complementary switches (e.g. S1-S1', S2-S2', etc.). Complementary switches cannot be activated simultaneously, which implies that while one of the switches from given eight pairs is activated then its complementary switch should remain deactivated or circuit could be short-circuited.

The balanced values of the FCC capacitors (C1, C2) and H-bridge capacitors (C3, C4) are 50 and 25 percent of the V_{DC}, respectively. Therefore, according to the states of switches, load voltage is the result of addition or subtraction of these voltages from V_{DC}. This leads to five nonnegative levels of load voltage, corresponding to modulation factor D, with values - 0, 1/4, 1/2, 3/4 and 1. Where, modulation factor D is the ratio of average load voltage to the input DC voltage.

If required load voltage does not exactly lay on one of the levels, in other words, if D is not equal to one of the values mentioned above, Pulse Width Modulation (PWM) switching strategy is applied to obtain desired voltage on the load. In such cases, in order to take advantages of the natural voltage balancing, load voltage must be switched between two nearest levels. For instance, in order to obtain output voltage with modulation index D=3/8, load voltage needs to be switched between D=1/4 and D=1/2.

3.3 Energy-based time domain analysis

Energy-based time domain analysis requires understanding of time averaging technique, energy conservation law and natural balancing roots. In addition, in order to determine optimal switching patterns, programming skill is required. Moreover, knowledge of simulation software including PowerSim and MATLAB is necessary.

The approach of natural balancing investigation could be summarized in the following steps:

- Development of the modulation strategy
- Analysis of the modulation strategy using time – domain energy based approach described in [25].
- Verification of the modulation strategy effectiveness and comparison between obtained voltage balancing dynamics and accurate voltage waveforms using MATLAB simulation.

3.3.1 Modulation strategy

Modulation strategy – is the switching patterns that controls semiconductor switches of the circuit and is dedicated to provide the voltage balancing on the load. Identification of the modulation strategy is considered to be a painstaking work that requires understanding of the subject and certain part of physical intuition. There is variety of the switching topologies – different simplified circuit layouts, that correspond to certain voltage level. One of the important tasks is to selectively combine the switching topologies that correspond to the same voltage level into switching pattern. Selection criteria implies that amount of positive and negative currents flowing through each capacitor are maximum, and on the other hand, overall current flowing through each capacitor is zero. Moreover, the switching efficiency is also very important parameter to be consider during investigation of the modulation strategy. It implies that the states of each switch changes as rare as possible.

3.3.2 Description of the analysis

Time-domain energy based analysis requires identification of the equations that describe capacitor's voltage damping time constant and periodic oscillation frequency.

According to [25], after selecting proper topologies pattern on the PWM period, Ohmic power loss needs to be calculated using equation (1).

$$P(D) = \frac{1}{T_{PWM}} \int_0^{T_{PWM}} i^2(t) R dt \quad (1)$$

where,

i(t) – is the piece - wise capacitor current

Then, equation (2) is generated using continuous derivative approximation of an average capacitor energy, stored on PWM, and energy conservation law.

$$\frac{\Delta\left(\frac{CV_C{}^2}{2}\right)}{T_{PWM}} \approx \frac{d\left(\frac{CV_C{}^2}{2}\right)}{dt} = -P(D) \quad (2)$$

Then, equation (2) is modified to give equation (3)

$$\frac{d\,(V_C)}{dt} = \frac{-P(D)}{C} \quad (3)$$

Solution of linear ordinary equation – equation (3), contains the equation of damping time constant.

Periodic oscillation frequency – *ω(D)*, is determined using following steps:

1. Calculate piece-wise linear load current on a PWM period, assuming that voltage on a capacitor is constant
2. Calculate capacitor voltage increments on each of the switching subintervals and PWM period
3. Identify homogeneous differential voltage equations using continuous derivative approximation

4. Identify dependence of oscillation frequency on modulation index – D, by solving equations in step 3

Time – domain-averaging methodology allows identification of voltage dynamics' characteristics for and AC modulation. Time – dependent instantaneous modulation command is described by equation (4) [25].

$$D(t) = Msin(\omega_f t) \quad (4)$$

where,

M – AC modulation index with range of (-1; 1)

ω_f – fundamental AC angular frequency

AC oscillation frequency is found by averaging DC oscillation frequency on AC fundamental period, as in equation (5).

$$\omega_{AC}(M) = \frac{1}{T_f}\int_0^{T_f} \omega_{DC}[Msin(\omega_f t)]\, dt \quad (5)$$

Similarly, AC damping time constant is found by averaging DC oscillation frequency on AC fundamental period, as in equation (6)

$$T_{AC}(M) = \frac{1}{T_f}\int_0^{T} T_{DC}[Msin(\omega_f t]dt \quad (6)$$

Both, equations (6) and (7) require AC fundamental frequency to be significantly smaller than PWM frequency, because time-averaging is reasonable only if sufficient amount of PWM periods are considered.

3.4 Software simulation

3.4.1 Identification of the switching patterns

As it was mentioned before, identification of the switching patterns is a painstaking procedure that requires time and some physical intuition. Therefore, for the convenience, it was decided to develop Matlab codes, that would identify the switching patterns for each level and consequently the whole modulation strategy (see Appendix D). The working algorithm of these codes could be described as follows:

1. All possible switching topologies for the HFCC converter are identified
2. All topologies are separated to the corresponding voltage levels
3. Obtained topologies, are classified according to the states of H-Bridge capacitors (e.g. plus-plus, plus-minus, minus-plus and minus-minus)
4. Next, patterns, whose overall current flowing through H-Bridge capacitors is zero, are selected
5. Finally, the algorithm checks, whether the states of FCC capacitors, are similar: if, after certain shift, states of capacitor C1 are identical to the states of C2, topology is selected

Obtained switching topologies compose various switching patterns, for each modulation level. Therefore, it is important to identify patterns, with the fewest

number of state switching of the capacitors. This is achieved using 'Number_of_Switching' function presented in Appendix D.

As the result we get the switching topologies that have the least number of switching of the semiconductors. In addition, using the physical intuition and taking all voltage levels into account, the states of the capacitors are selected to give least number of switching between levels.

3.4.2 Matlab simulation

Simulation was performed using a MATLAB Simulink – modelling tool. Constructed model is illustrated on the Fig. 3.2. All the circuit elements were selected from the 'SimPowerSystems' components library. The states of the switches were controlled by PWM and generated tables that correspond to the switching patterns. During the simulation, ideal switches were used in order to eliminate parasitic effects. Table 3.1, given below demonstrates the simulation parameters of the circuit elements. Capacitor voltages were displaced from their balanced values in order to be able to observe balancing dynamics.

Table3. 1: Simulation parameters of the circuit elements

Parameter	**Element**	**Unit**	**Value**
Capacitance	C1,C2	uF	400
Capacitance	C3,C4	uF	200
Inductance	L	mH	150
Resistance	R	Ω	6
Frequency	f_s	kHz	20
Internal resistance of transistor	R_{on}	mΩ	1
Snubber resistance of transistor	R_s	MΩ	0.1

Determination of the required output voltage level and consequently switching topology was performed using PWM. In order to achieve PWM, the input modulation signal, either DC or AC, is compared to the signal of magnitude equal to 1, and the switching frequency of the operation.

Limited counter, whose maximum value corresponds to the number of switching subintervals on the PWM period, with the falling edge detector of ramp signal is used to determine the serial number of certain topology in the switching table.

In parallel upper and lower switching levels are determined by manipulations with the modulation index. Then, upper or lower level is chosen based on the comparison of the ramp with the modulation signals. If the modulation signal is higher than a ramp signal, topology from the table corresponding to the upper level is selected and vice versa.

Finally, the output of the control block during each PWM subinterval is an array of 16 binary numbers that correspond to the states of the switches in the converter.

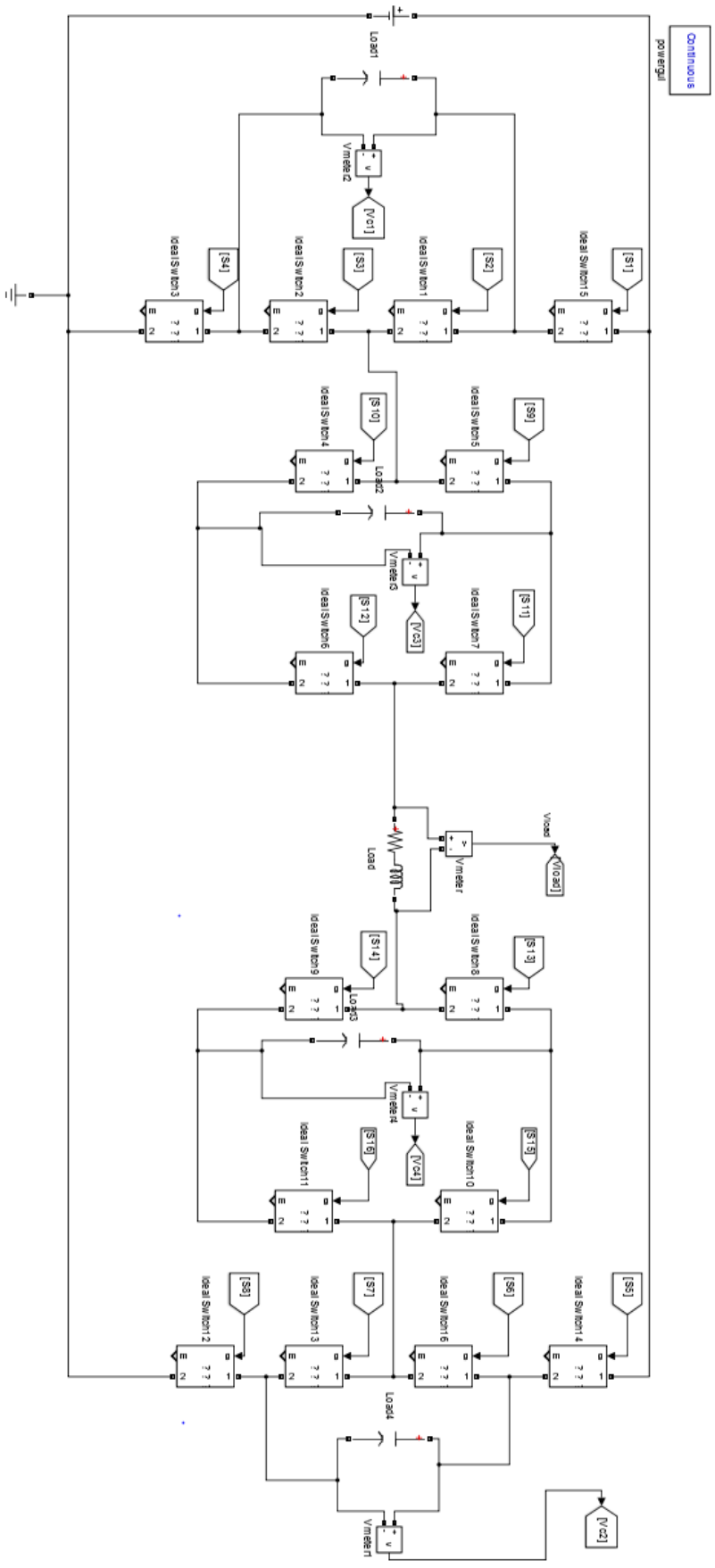
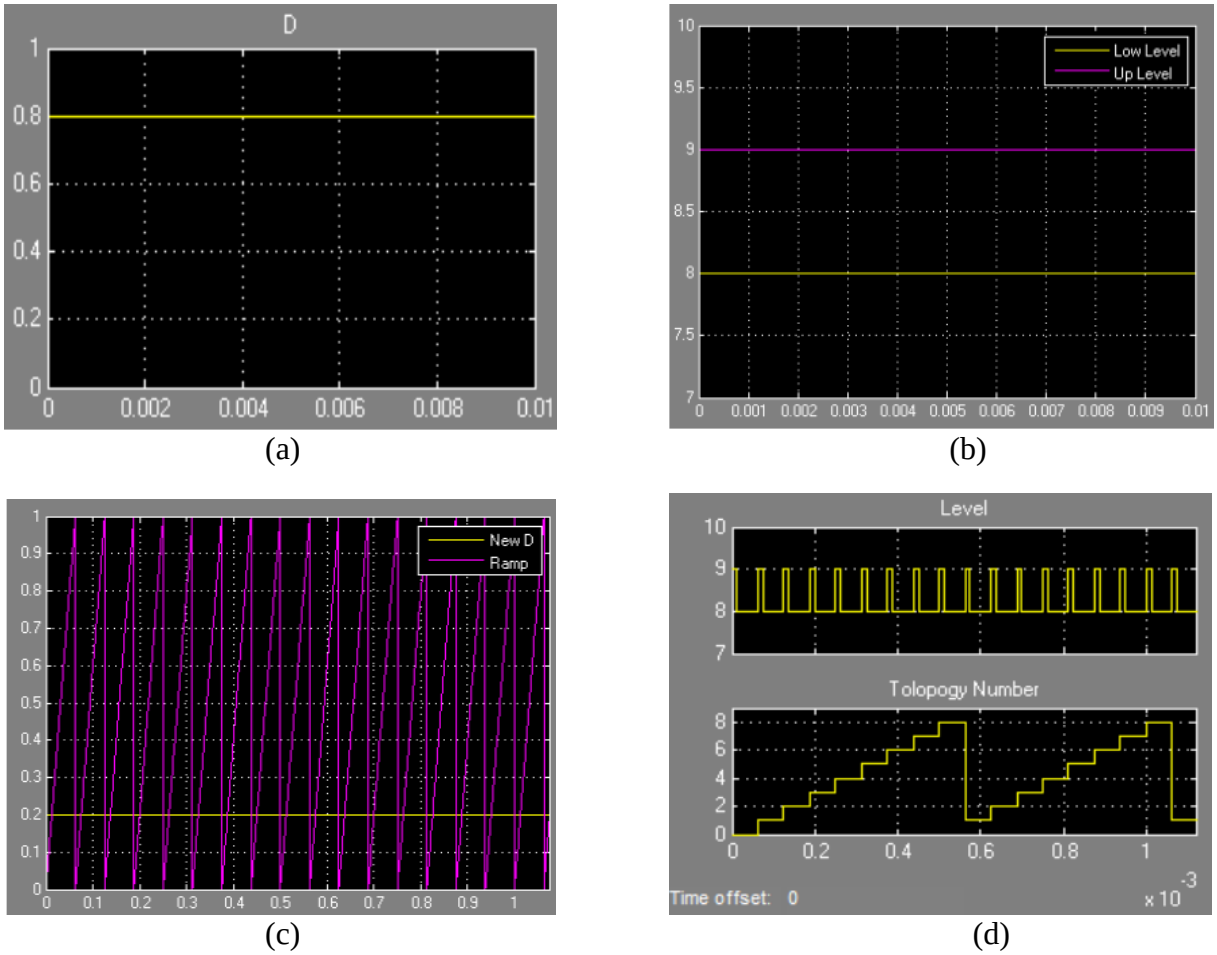


Fig3. 2: Matlab Simulink model

Operation of control block is presented on Fig.3.3, given below. DC modulation signal, with nodulation index D = 0.8 is considered as an example. The output levels are determined to be 8 and 9, that correspond to the modulation index values of 0.75 and 1 respectively. In addition, the modulation signal is modified in order to illustrate where exactly, between determined levels, the output voltage needs to stay. Moreover, the signal is compared to ramp in order to give voltage level and topology number.



(a) (b)

(c) (d)

Fig3. 3: DC mode operation of the PWM control block: (a) input modulation signal; (b) up/low output voltage levels; (c) modified modulation and ramp signals; (d) output voltage level and topology number

4. Results

4.1. Obtained Modulation Strategy

The balancing dynamics of the HFCC converter were analyzed using the Matlab codes described in section 3. This analysis contributed to the identification of the modulation strategy consisting of switching patterns for all voltage levels. Obtained modulation strategies are presented in tables that contain switching patterns for each of the nine modulation levels. In addition, it was found out that for HFCC converter, the most efficient operation is achieved, when sixteen subintervals on the PWM period are used. Table 2, presents switching pattern for modulation index D = 0. The rows in the table correspond to the citcuit topologies and consequently states of the switches in HFCC converter. These circuit topologies - are different layouts of the converter (see Appendix B).

Table4. 1: Switching pattern on a signle PWM period for normalized command D = 0

Switch number / Subinterval	S2	S1	S1’	S2’	S4’	S3’	S3	S4	S9	S10	S11	S12	S13	S14	S15	S16
1	1	0	1	0	1	0	1	0	0	1	1	0	1	0	0	1
2	1	0	1	0	0	0	1	1	1	0	0	1	1	0	0	1
3	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0
4	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	0
5	1	0	1	0	0	1	0	1	0	1	1	0	1	0	0	1
6	1	1	0	0	0	1	0	1	1	0	0	1	1	0	0	1
7	0	1	0	1	0	1	0	1	1	0	0	1	0	1	1	0
8	0	1	0	1	1	1	0	0	0	1	1	0	0	1	1	0
9	0	1	0	1	0	1	0	1	0	1	1	0	1	0	0	1
10	0	1	0	1	0	0	1	1	1	0	0	1	1	0	0	1
11	0	1	0	1	1	0	1	0	1	0	0	1	0	1	1	0
12	0	0	1	1	1	0	1	0	0	1	1	0	0	1	1	0
13	0	1	0	1	1	0	1	0	0	1	1	0	1	0	0	1
14	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1
15	1	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
16	0	0	1	1	1	1	0	0	0	1	1	0	0	1	1	0

Fig. 4.1 – 4.3 present the circuit topologies generated for the modulation index D = 0. All these topologies could be divided into three groups, depending on the voltage level produced by FCC converter separately. For instance, on Fig. 4.1, there are topologies, whose FCC leg produce 1/2 volts and is compensated by H-Bridge capacitors to give 0 V on the load. Moreover, on Fig. 4.2, there are circuit topologies whose FCC leg produce 0 V and consequently, H-Bridge capacitors are used to compensate each other, and therefore there are eight possible topologies instead of four. Futhermore, it could be seen that the total number of possible topologies, that produce modulation index D = 0, is sixteen. That is why, the optimal number of subintervals was considered to be sixteen. In addition, while capacitors are either charged or discgarged, the overall capacitors' voltages and currents in all sixteen topologies are equal to zero. This is the base requirement to achieve natural balancing in converter.

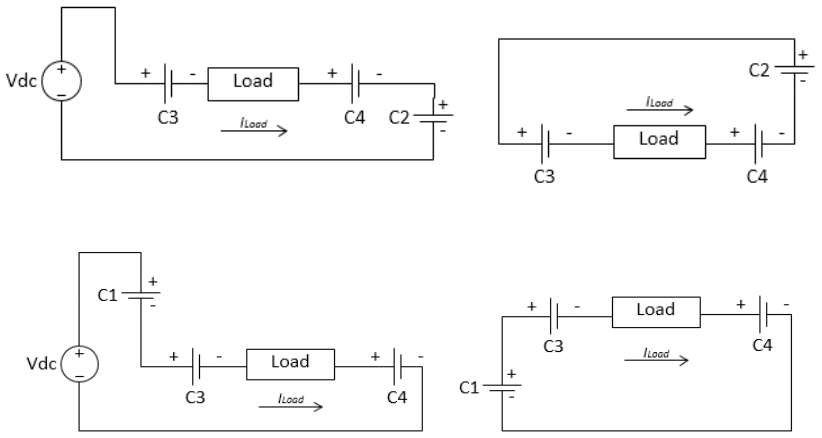


Fig4. 1: Topologies for D=0 (FCC leg 1/2 V and H-Bridge capacitors -1/4 V and -1/4 V)

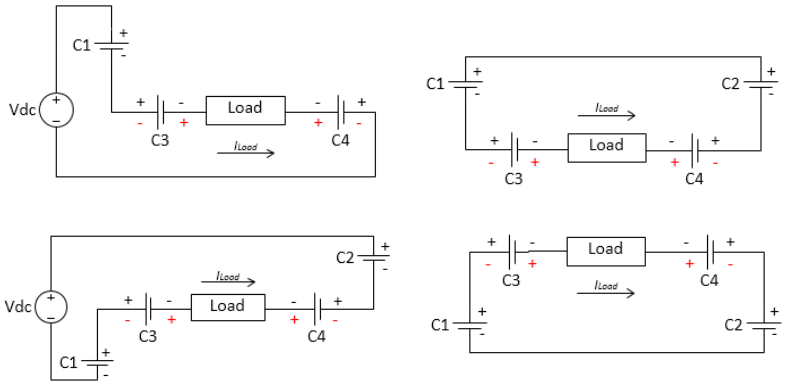


Fig4. 2: Topologies for D=0 (FCC leg 0 V and H-Bridge capacitors -/+1/4 V and +/-1/4 V)

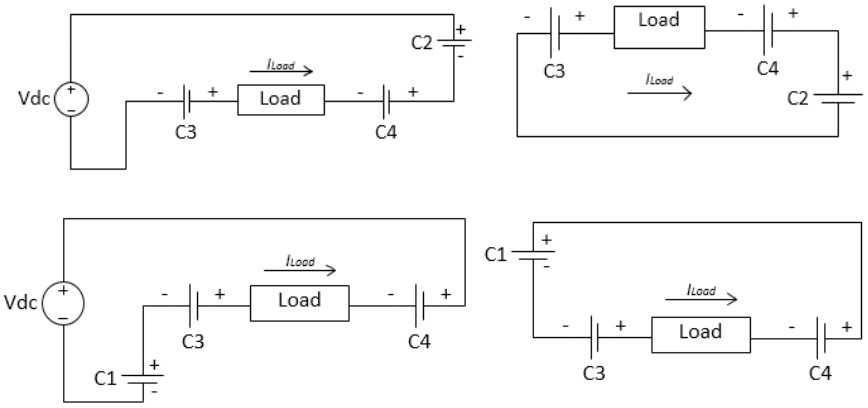


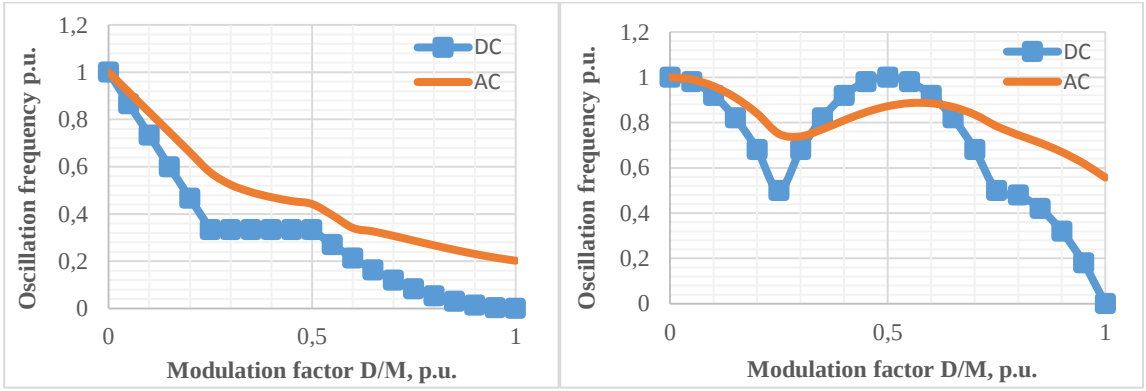
Fig4. 3: Topologies for D=0 (FCC leg -1/2 V and H-Bridge capacitors +1/4 V and +1/4 V)

In order to produce negative modulation, it is required to change the states of the switches of the FCC and H-Bridge converters. Therefore, if for positive voltage levels capacitor was charged, for negative it will be discharged and vice versa. Therefore, in total we get nine possible voltage levels.

4.2. Energy based time domain analysis results

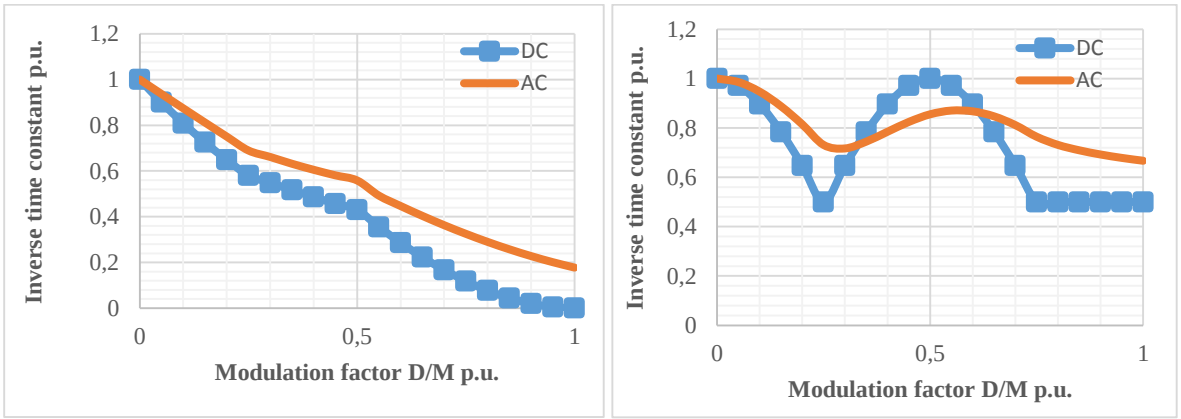
Periodic oscillation frequencies and inverse of periodic time constants for FCC leg and H-Bridge capacitors are presented on Fig. 4.4 and Fig.4.5, respectively. These figures are based on the analytical equations (7-10).

Observations have shown, that FCC capacitors (C1,C2) and H-bridge capacitors (C3,C4) natural balancing dynamics are totally decoupled. This implies that balancing dynamics for each pair could be studied separately. In addition, it was found out that for FCC leg capacitors balancing is aperiodic and for H-Bridge capacitors balancing is periodic (oscillating).



(a) (b)

Fig4. 4: Periodic oscillation frequency for nonnegative modulation indices: (a)FCC capacitors, (b) H-Bridge capacitors



(a) (b)

Fig4. 5: Inverse periodic time constant for nonnegative modulation indices: (a) FCC capacitors, (b) H-Bridge capacitors

Oscillation frequencies and time constants for negative modulation indices are symmetrical to those shown on Figs 4.4, 4.5 due to symmetrical nature of the converter operation and produced switching tables. From the graphs it could be seen that the balancing speed decreases as the modulation indices approach 1 and -1. The fastest balancing of FCC leg capacitors is achieved at modulation index of 0.25 for both DC and AC PWM. In addition, there is no balancing for DC PWM when the modulation index - |D| = 1, and for AC PWM the balancing is the slowest at the same index. Considering the graphs for H-Bridge capacitors, it could be stated that the fastest balancing is also achieved at modulation indices of 0 and 0.25. Moreover, the slowest balancing is achieved for modulation index D = 1. On the other hand, AC PWM has better voltage balancing for modulation region $0.75<|M|<1$ and achieve the best balancing rate for modulation indices around 0. The poor balancing characteristics for the high modulation indices for DC PWM could be explained by the fact, that all the FCC leg and H-Bridge capacitors are disconnected for the modulation index - |D| =1. However, for AC PWM the balancing is better for the high modulation indices, because time when modulation level 1 and -1 are required is small compared to the period of input voltage meaning that capacitors are totally disconnected for the acceptable amount of time.

Equations (7) and (8) present the oscillation frequencies of the FCC leg and H-Bridge capacitors, respectively, and equations (9), (10) present periodic time constants of these capacitors.

$$\omega(D) = \begin{Bmatrix} \frac{T(3-8D)}{32LC} & 0 \le D \le \frac{1}{4} \\ \frac{T}{32LC} & \frac{1}{4} \le D \le \frac{1}{2} \\ \frac{T(1-D)^2}{8LC} & \frac{1}{2} \le D \le 1 \end{Bmatrix} \quad (7)$$

$$\omega(D) = \begin{Bmatrix} \frac{T(1-8D^2)}{32LC} & 0 \le D \le \frac{1}{4} \\ \frac{T(8D-1-8D^2)}{32LC} & \frac{1}{4} \le D \le \frac{3}{4} \\ \frac{T(3D-1-2D^2)}{8LC} & \frac{3}{4} \le D \le 1 \end{Bmatrix} \quad (8)$$

$$T(D) = \begin{Bmatrix} \frac{2048CL^2}{(48D^2-64D+31)T^2R} & 0 \le D \le \frac{1}{4} \\ \frac{1536CL^2}{(16D^3-12D^2-12D+17)T^2R} & \frac{1}{4} \le D \le \frac{1}{2} \\ \frac{192CL^2}{(2D+4)(D-1)^2T^2R} & \frac{1}{2} \le D \le 1 \end{Bmatrix} \quad (9)$$

$$T(D) = \begin{Bmatrix} \frac{768CL^2}{(1-2D)^2(4D+1)T^2R} & 0 \le D \le \frac{1}{4} \\ \frac{192CL^2}{D^2(3-4D)T^2R} & \frac{1}{4} \le D \le \frac{1}{2} \\ \frac{192CL^2}{(4D-1)(D-1)^2T^2R} & \frac{1}{2} \le D \le \frac{3}{4} \\ \frac{1536CL^2}{T^2R} & \frac{3}{4} \le D \le 1 \end{Bmatrix} \quad (10)$$

Calculated oscillation time frequencies and damping time constants resulted in the analytical solutions of voltage balancing dynamics for selected modulation strategy. Equations (11) and (12) present the balancing dynamics of the FCC leg and H-Bridge capacitors, respectively. Obtained equations do not require heavy calculation capabilities. This implies that computations are conducted faster and require less effort.

$$V_1(t) = \frac{V_{DC}}{2} + \left[V_1(0) - \frac{V_{DC}}{2} \right] \exp\left(-t/T_1(D)\right)\cos\omega_1(D)t \pm \left[V_2(0) - \frac{V_{DC}}{2} \right] \exp\left(-t/T_1(D)\right)\sin\omega_1(D)t;$$
$$V_2(t) = \frac{V_{DC}}{2} \mp \left[V_1(0) - \frac{V_{DC}}{2} \right] \exp\left(-t/T_1(D)\right)\sin\omega_1(D)t + \left[V_2(0) - \frac{V_{DC}}{2} \right] \exp\left(-t/T_1(D)\right)\cos\omega_1(D)t.$$

(11)

$$V_3(t) = \frac{V_{DC}}{4} + \left[V_3(0) - \frac{V_{DC}}{4} \right] \exp\left(-t/T_2(D)\right)\cos\omega_2(D)t \pm \left[V_4(0) - \frac{V_{DC}}{4} \right] \exp\left(-t/T_2(D)\right)\sin\omega_2(D)t;$$
$$V_4(t) = \frac{V_{DC}}{4} \mp \left[V_3(0) - \frac{V_{DC}}{4} \right] \exp\left(-t/T_2(D)\right)\sin\omega_2(D)t + \left[V_4(0) - \frac{V_{DC}}{4} \right] \exp\left(-t/T_2(D)\right)\cos\omega_2(D)t.$$

(12)

4.3 Simulation Results

Simulation was performed utilizing the model produced in MATLAB Simulink software. This model gave an opportunity to evaluate obtained switching strategy and voltage balancing dynamics.

Load voltages and currents for both AC and DC PWM simulations are presented on the Fig. 4.6-4.11. In addition, comparison of the expected voltage waveforms, that are produced using balancing dynamics equations, and actual capacitor voltage waveforms produced by modulation strategy simulation, is presented on Fig 4.12 - 4.17.

Simulation of DC PWM has shown, that for any modulation index, output voltage is switched between the nearest converter voltage levels. Average output voltage can be calculating using Ohm's law, assuming negligible effects of the load inductance on the voltage. Therefore, by multiplying average stabilized current by load resistance, which is equal to 6 Ohm, it could be found that for modulation

indices 0.2, 0.4 and 0.8 corresponding average output voltage values are 20,40 and 80 V respectively.

Considering AC PWM simulation, it could be seen from the load voltage and current waveforms, that output voltage is the staircase sinusoidal wave. Number of levels increases as the modulation index is increased. In addition, all nine levels are utilized for modulation index greater than 0.75. Moreover, it could be seen that load current is in phase with the load voltage.

During the simulation initial values of the FCC and H-Bridge capacitors were slightly moved from their balanced values. This results in very high oscillations of load current and voltage at the start of the simulation, that are decreased significantly when capacitors stabilize and their values are balanced.

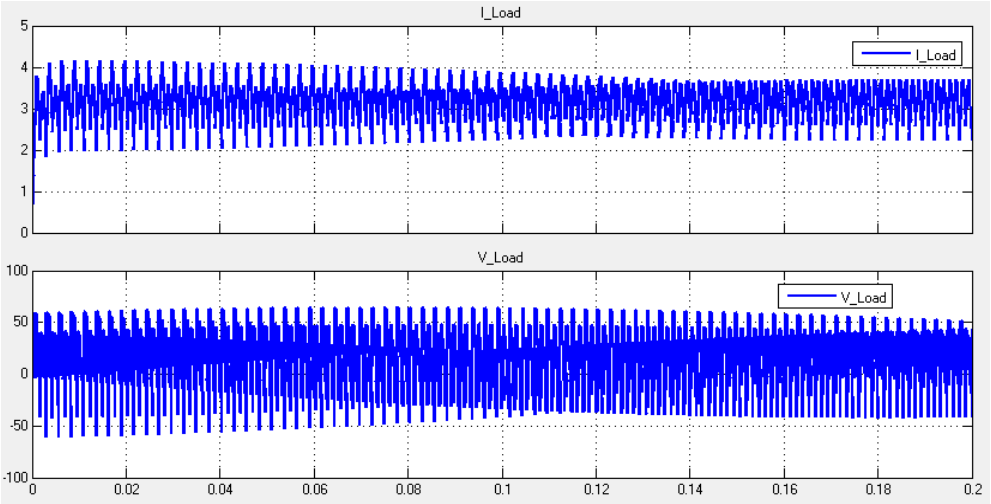


Fig4. 6: Load voltage and current of DC PWM modulation with D=0.2

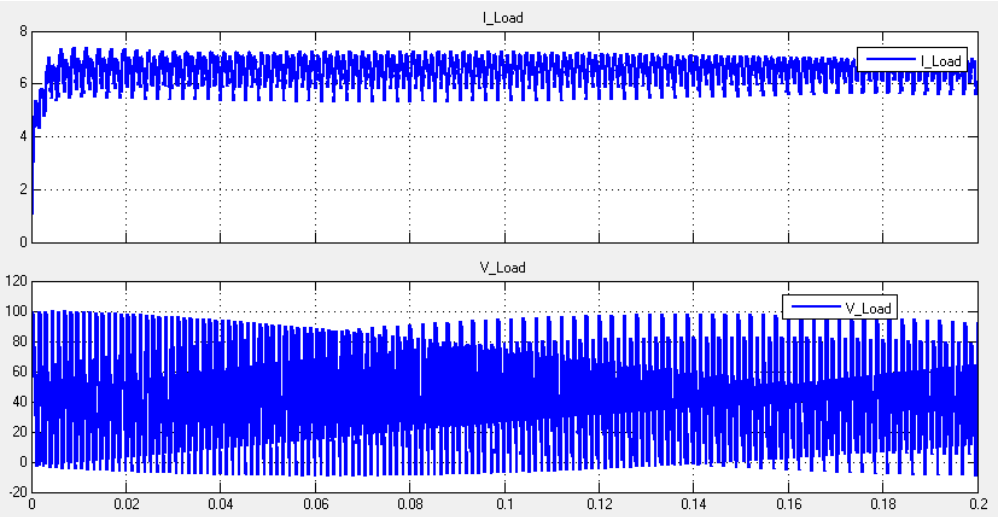


Fig4. 7: Load voltage and current of DC PWM modulation with D=0.4

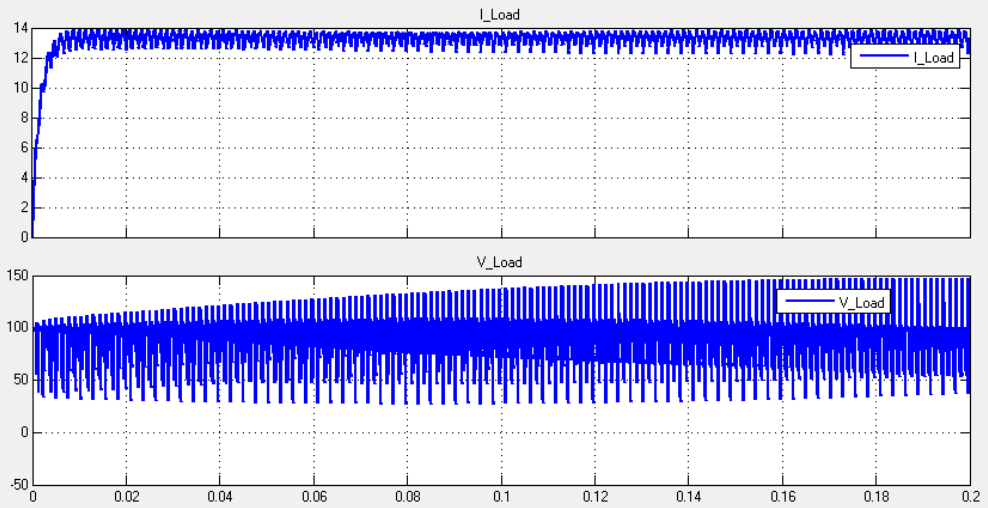


Fig4. 8: Load voltage and current of DC PWM modulation with D=0.8

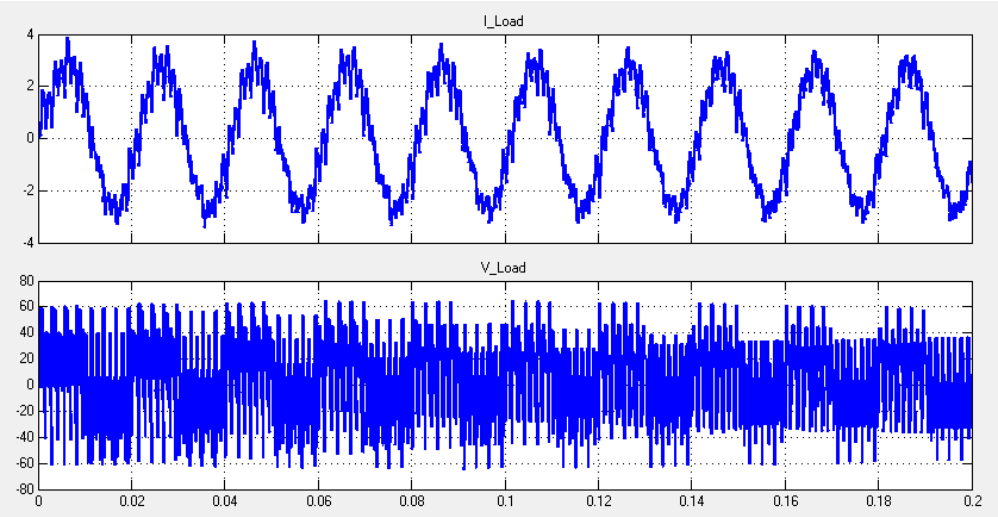


Fig4. 9: Load voltage and current of AC PWM modulation with M=0.2

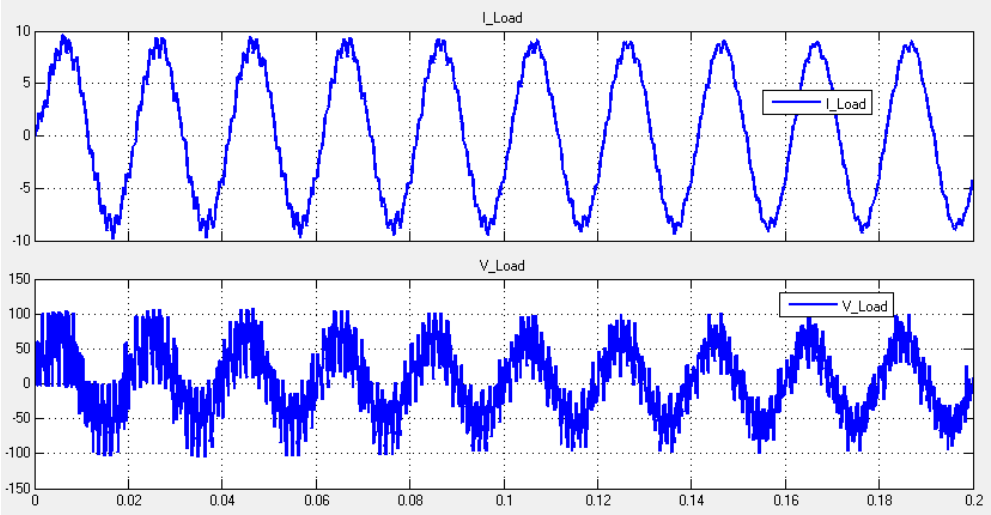


Fig4. 10: Load voltage and current of AC PWM modulation with M=0.6

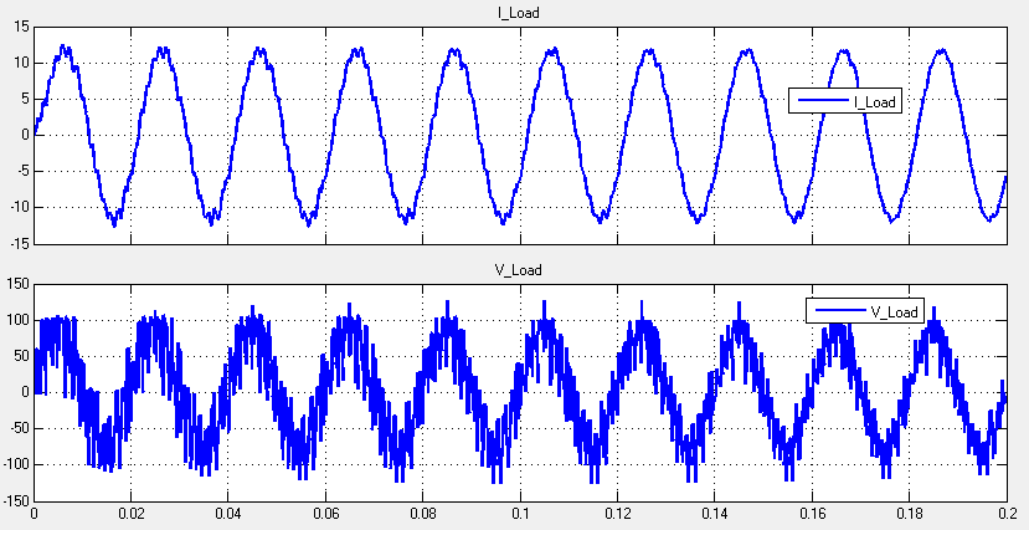
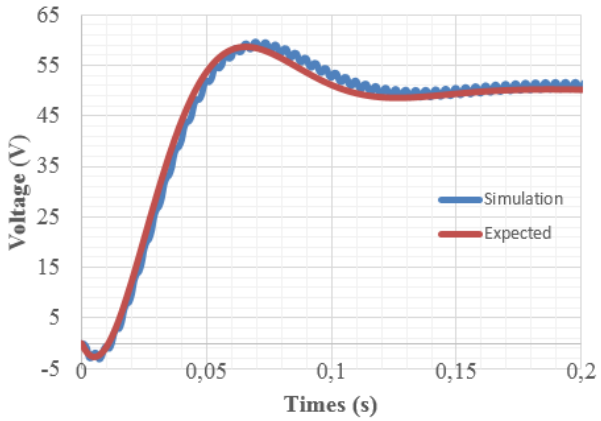
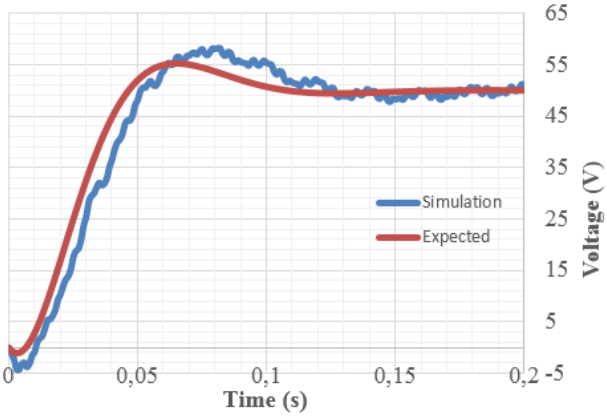


Fig4. 11: Load voltage and current of AC PWM modulation with M=0.8

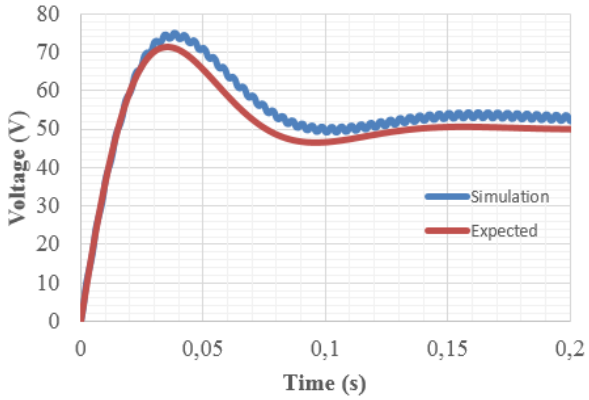
From the comparison given on Fig. 4.12-4.17, it could be seen, that obtained analytical capacitors' voltage waveforms correspond to waveforms obtained by simulation. In addition, it could be seen that FCC leg capacitors stabilize with equal speed in both AC and DC PWM for all modulation indices. Moreover, H-Bridge capacitors stabilize faster with DC PWM for low modulation indices, but for high modulation indices, voltage balancing time is less with AC PWM. Furthermore, the voltage ripples increase when modulation index is increased for both AC and DC PWM. For instance, for modulation index of 0.2 voltage varies no more than by 1 V peak-to-peak, and for modulation index 0.8 the ripples reach 4 V.


Voltage (V)
Times (s)
Simulation
Expected

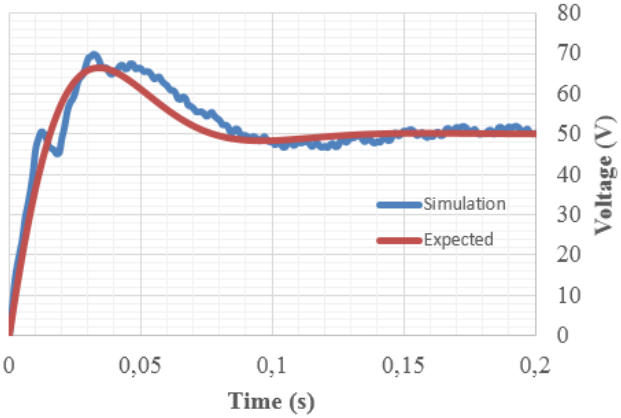
(a)


Voltage (V)
Time (s)
Simulation
Expected

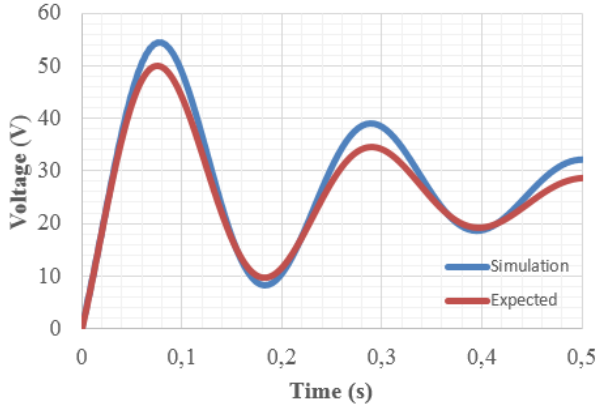
(a)


Voltage (V)
Time (s)
Simulation
Expected

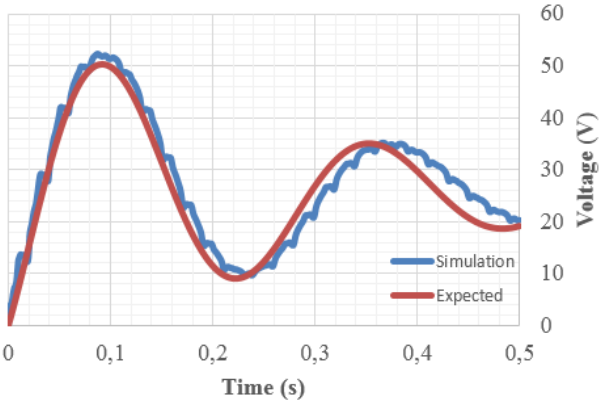
(b)


Voltage (V)
Time (s)
Simulation
Expected

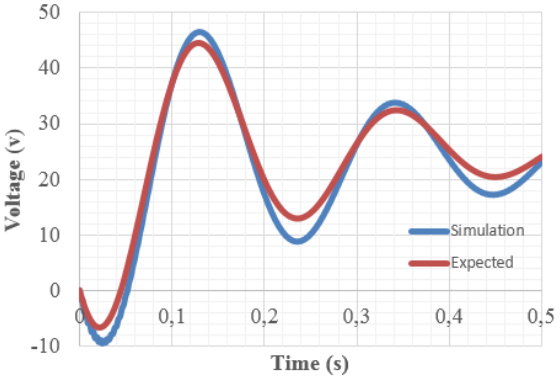
(b)


Voltage (V)
Time (s)
Simulation
Expected

(c)

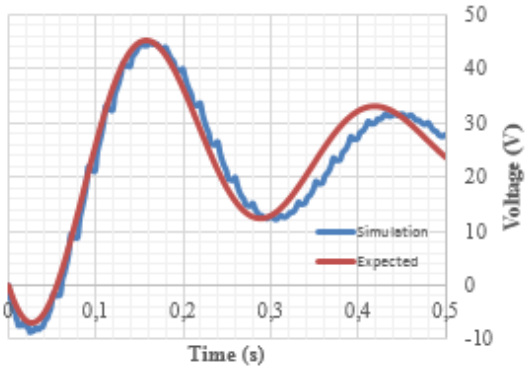

Voltage (V)
Time (s)
Simulation
Expected

(c)



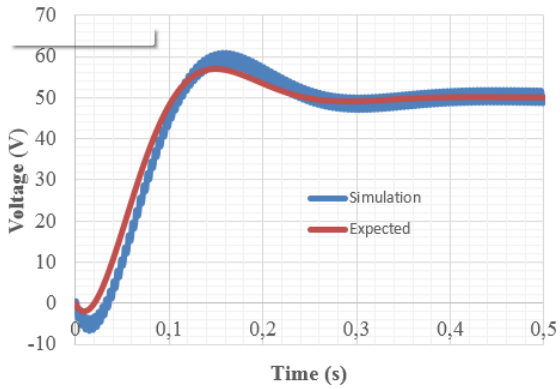
(d)

Fig4. 12: Comparison of accurate (simulation) and average (expected) balancing dynamics for DC PWM with D=0.2 (a)C1 (b) C2 (c) C3 (d) C4

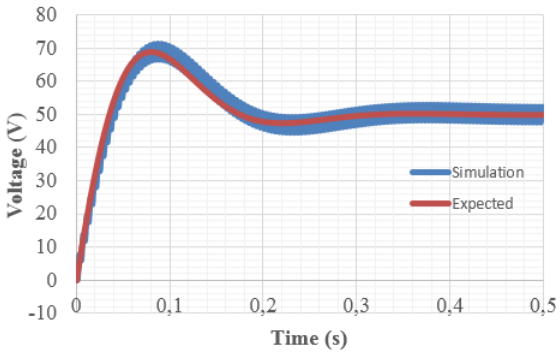


(d)

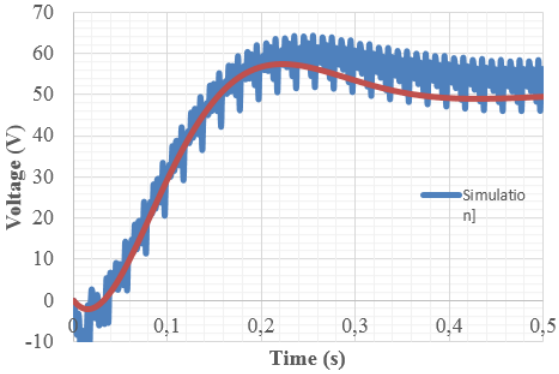
Fig4. 13: Comparison of accurate (simulation) and average (expected) balancing dynamics for AC PWM with D=0.2 (a)C1 (b) C2 (c) C3 (d) C4



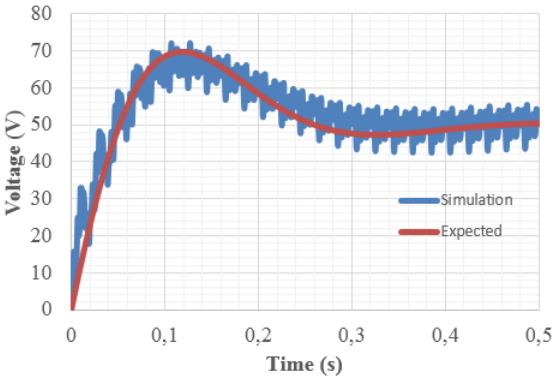
(a)



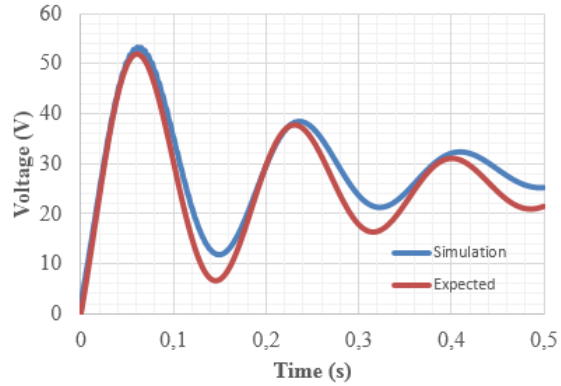
(b)



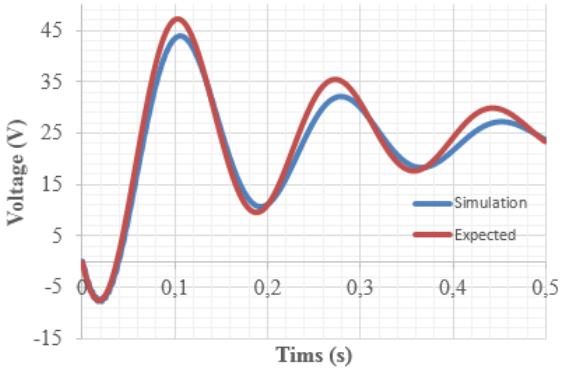
(a)



(b)

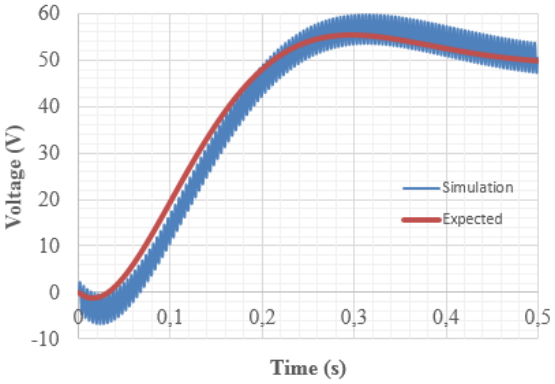


(c)

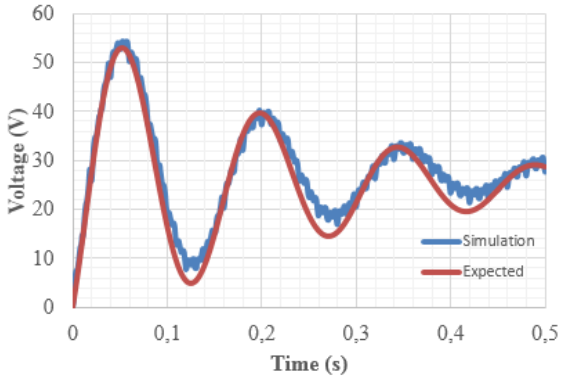


(d)

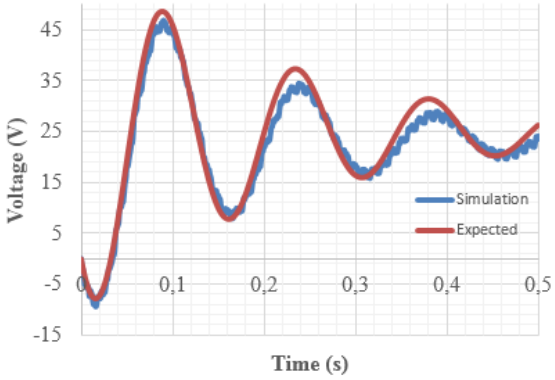
Fig4. 14: Comparison of accurate (simulation) and average (expected) balancing dynamics for DC PWM with D=0.6 (a)C1 (b) C2 (c) C3 (d) C4



(a)

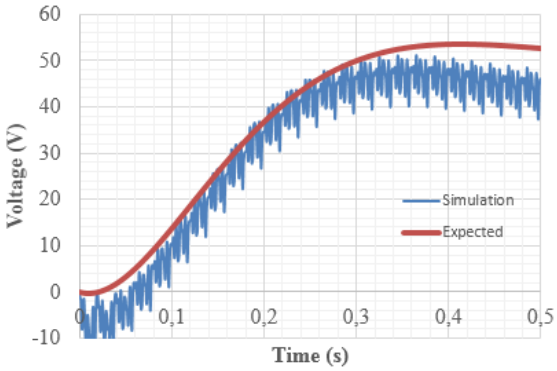


(c)

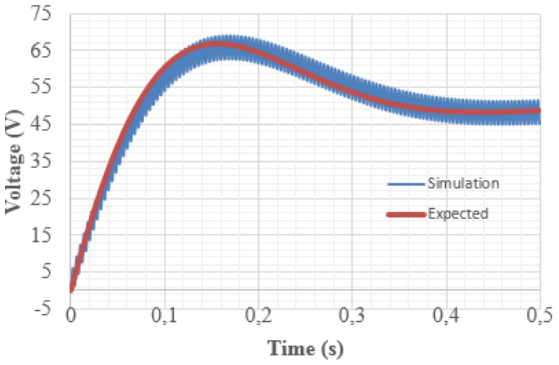


(d)

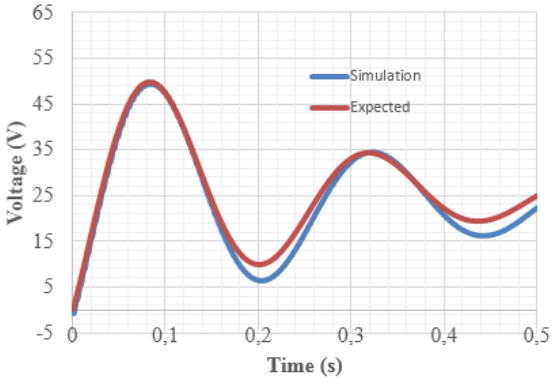
Fig4. 15: Comparison of accurate (simulation) and average (expected) balancing dynamics for AC PWM with D=0.6 (a)C1 (b) C2 (c) C3 (d) C4



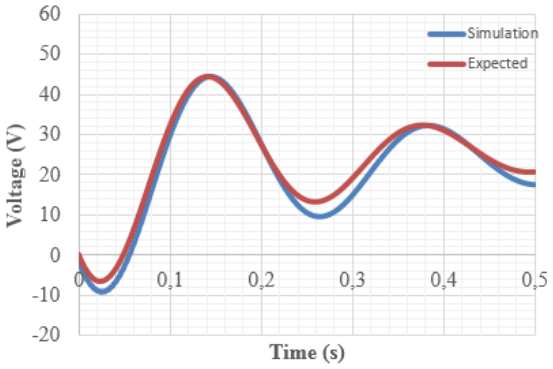
(a)



(b)

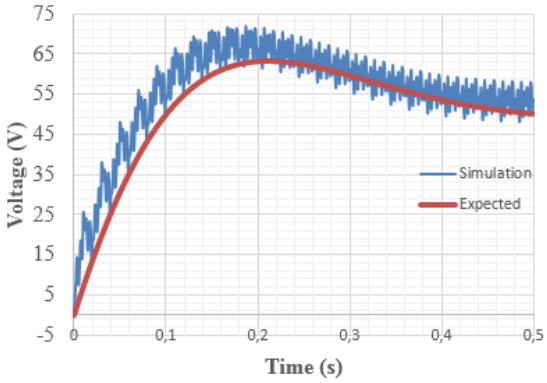


(c).

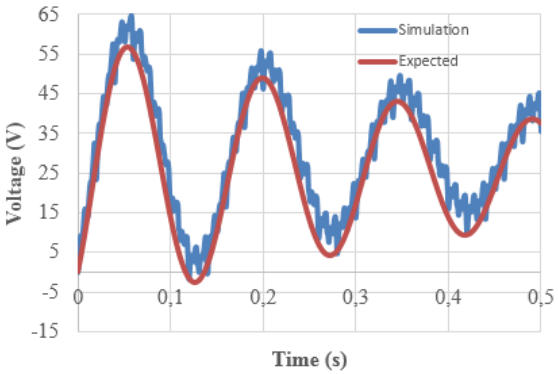


(d)

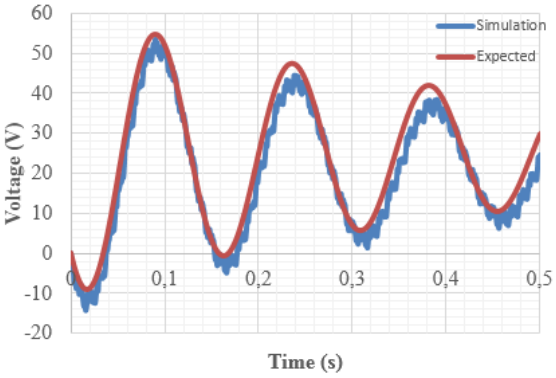
Fig4. 16: Comparison of accurate (simulation) and average (expected) balancing dynamics for DC PWM with D=0.8 (a)C1 (b) C2 (c) C3 (d) C4



(b)



(c)



(d)

Fig4. 17: Comparison of accurate (simulation) and average (expected) balancing dynamics for AC PWM with D=0.8 (a)C1 (b) C2 (c) C3 (d) C4

5. Discussion

The main deliverables of the project including: modulation strategy and balancing dynamics equations were successfully obtained. Presented simulations results have demonstrated that produced modulation strategies could provide a good level of voltage balancing rate of the converter. For instance, for the selected parameters, total balancing time do not exceed 0.3 s, which correspond to the balancing speed that is applicable for majority of the converter applications.

In addition, Matlab codes that define modulation strategy were developed. As it could be seen from the results, the modulation strategy produced by this codes produce balancing of the converter and moreover provide a good balancing speed. Furthermore, manual identification of the modulation strategy is very painstaking work that requires physical intuition, which is significantly reduced with introduction of the Matlab codes.

The main feature of the obtained modulation strategy is the fact that the balancing speed of the converter declines, when the modulation index is increased. In addition, the voltage ripples of the load voltage waveforms also increase with the increasing value of modulation index. The ripples could be decreased by increasing the values of the converters. However, from equations (9) and (10) it is clear that larger capacitances will cause the slower balancing of the load

voltage. Therefore, compromise between voltage ripples and balancing rate should be identified for each particular application.

Moreover, obtained modulation strategy implies that natural voltage balancing is achievable for HFCC multilevel converter. All switching patterns lead to the stabilization of the output voltage on the corresponding voltage level. Furthermore, no closed loop control was used in order to control converter operation and consequently adjust required voltage levels. This is considered to be the main feature of the natural balancing.

In addition, the natural balancing identification on a particular voltage level depends on the number of different topologies that are used to produce the same output voltage level. It is clear that with the small number of redundant switching topologies, as for modulation index 1, natural balancing is the worst. On the other hand, the balancing characteristics of the modulation index - 0.25 are significantly better, as the number of possible topologies is correspondingly larger. Another important factor in the identification of the natural balancing is the number of 'active' capacitors utilized during each PWM subinterval. This implies that if more capacitors exchange their unbalance energy at each time step, obtained balancing characteristics will be better.

Interestingly, FCC leg and H-Bridge capacitors are totally decoupled. This implies that natural balancing in these capacitors could be investigated separately. Consequently, when modulation strategy is developed for similar converter even

with higher number of levels, following modulation strategy could be used for the FCC leg converters.

Finally, identification of the switching strategy by utilizing unbalance energy movement between capacitors has proven its applicability for the multilevel converter types, where redundant topologies are available on voltage levels.

Time-domain energy-based analysis and simulation of the modulation strategy have shown, that obtained analytical equations accurately natural balancing characteristics of FCC and H-Bridge capacitors' voltages. Accuracy of the result with low required computational effort, makes this analysis method more preferable then, for instance, very popular frequency-based harmonic elimination technique described in [26]-[28]. These methods required more computational effort and do not investigate the roots of the voltage unbalance.

Furthermore, obtained modulation strategy for natural balancing could be considered as an alternative for active balancing. For example in terms of reliability, since any fault of the sensing and controlling system could significantly worsen operation of the converter with active balancing, while converter operation with natural balancing does not require these systems. This advantage of natural balancing allows to reduce the overall size and weight of the system, which is considered to be important for power conversion in satellites or aircrafts.

6. Conclusion

It was proven that natural balancing is driven by the dissipation of the unbalance energy. This fact is significant, since it helps to understand the balancing mechanisms of multilevel converters. Consequently, it promotes identification of good quality natural voltage balancing topologies and modulation strategies. In addition, the need in active balancing requirements is reduced. Therefore, converter operation becomes more economically beneficial, as the number of sensing, controlling and decision-making units is reduced. This is especially important for the low power applications, where, for example, sensors and microcontrollers compose the major part of the equipment's total cost.

This paper presents application of time-domain analysis and shows that it is powerful and useful analysis. With the help of the analysis, natural balancing with acceptable balancing rates was investigated for HFCC converter, for which it was not reported previously in literature. The balancing was achieved using modulation strategy presented in the form of tables for both AC and DC PWM. Identification of the modulation strategy was significantly facilitated with the development of the Matlab codes that define all possible topologies and switching patterns. Moreover, obtained modulation strategy could be scaled and adapted to HFCC converter with higher number of voltage levels.

In addition, produced analytical equations that are dedicated to describe voltage balancing dynamics of the converter for the whole range of modulation indices do not require heavy computational effort and therefore, their computation could be carried out online.

In conclusion, it could be stated that obtained modulation strategy has a good balancing dynamics for low modulation indices and the worst characteristics at modulation index equal to 1.

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Appendices

This part contains additional equations, figures and tables that were produced during the development of the following report. They could be found useful for the further understanding of the thesis. It consists of three parts, including: Appendices A, B, C and D.

Appendix A: Tables of the states of switches

Table A. 1: States of the capacitors on a single PWM period for normalized command D =1

Switching pattern / Capacitors	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C3	+	0	-	0	+	0	-	0	+	0	-	0	+	0	-	0
C4	-	0	+	0	-	0	+	0	-	0	+	0	-	0	+	0

Table A. 2: Switching pattern on a signle PWM period for normalized command D = 1

Switch number / Subinterval	S2	S1	S1’	S2’	S4’	S3’	S3	S4	S9	S10	S11	S12	S13	S14	S15	S16
1	1	1	0	0	0	0	1	1	1	0	0	1	0	1	1	0
2	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
3	1	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1
4	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
5	1	1	0	0	0	0	1	1	1	0	0	1	0	1	1	0
6	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
7	1	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1
8	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
9	1	1	0	0	0	0	1	1	1	0	0	1	0	1	1	0
10	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
11	1	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1
12	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
13	1	1	0	0	0	0	1	1	1	0	0	1	0	1	1	0
14	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0
15	1	1	0	0	0	0	1	1	0	1	1	0	1	0	0	1
16	1	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0

Table A. 3: States of the capacitors on a single PWM period for normalized command D=3/4

Switching pattern / Capacitors	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C1	0	+	0	0	0	-	0	0	0	-	0	0	0	+	0	0
C2	0	0	+	0	0	0	+	0	0	0	-	0	0	0	-	0
C3	+	0	-	0	+	0	-	0	+	0	-	0	+	0	-	0
C4	0	-	0	+	0	-	0	+	0	-	0	+	0	-	0	+

Table A. 4: Switching pattern on a signle PWM period for normalized command D = 3/4

Switch number / Subinterval	S2	S1	S1’	S2’	S4’	S3’	S3	S4	S9	S10	S11	S12	S13	S14	S15	S16
1	1	1	0	0	0	0	1	1	1	0	0	1	1	0	1	0
2	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0
3	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0
4	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1
5	1	1	0	0	0	0	1	1	1	0	0	1	1	0	1	0
6	0	1	0	1	0	0	1	1	1	0	1	0	0	1	1	0
7	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0
8	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1
9	1	1	0	0	0	0	1	1	1	0	0	1	1	0	1	0
10	0	1	0	1	0	0	1	1	1	0	1	0	0	1	1	0
11	1	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0
12	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1
13	1	1	0	0	0	0	1	1	1	0	0	1	1	0	1	0
14	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0
15	1	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0
16	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1

Table A. 5: States of the capacitors on a single PWM period for normalized command D=1/2

Switching pattern / Capacitors	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C1	0	+	+	0	0	-	-	0	0	-	-	0	0	+	+	0
C2	0	0	+	+	0	0	+	+	0	0	-	-	0	0	-	-
C3	+	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
C4	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-	+

Table A. 6: Switching pattern on a signle PWM period for normalized command D = 1/2

Switch number / Subinterval	S2	S1	S1’	S2’	S4’	S3’	S3	S4	S9	S10	S11	S12	S13	S14	S15	S16
1	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
2	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1	0
3	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
4	1	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1
5	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
6	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0
7	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
8	1	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1
9	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
10	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0
11	0	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0
12	1	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1
13	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
14	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1	0
15	1	0	1	0	0	1	0	1	0	1	1	0	0	1	1	0
16	1	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1

Table A. 7: States of the capacitors on a single PWM period for normalized command D=1/4

Switching pattern / Capacitors	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C1	0	+	+	0	0	-	-	0	0	-	-	0	0	+	+	0
C2	0	0	+	+	0	0	+	+	0	0	-	-	0	0	-	-
C3	+	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
C4	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-	+

Table A. 8: Switching pattern on a signle PWM period for normalized command D = 1/4

Switch number / Subinterval	S2	S1	S1’	S2’	S4’	S3’	S3	S4	S9	S10	S11	S12	S13	S14	S15	S16
1	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
2	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1	0
3	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
4	1	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1
5	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
6	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0
7	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
8	1	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1
9	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
10	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0
11	0	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0
12	1	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1
13	1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1
14	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1	0
15	1	0	1	0	0	1	0	1	0	1	1	0	0	1	1	0
16	1	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1

Appendix B: Graphs for voltage waveforms

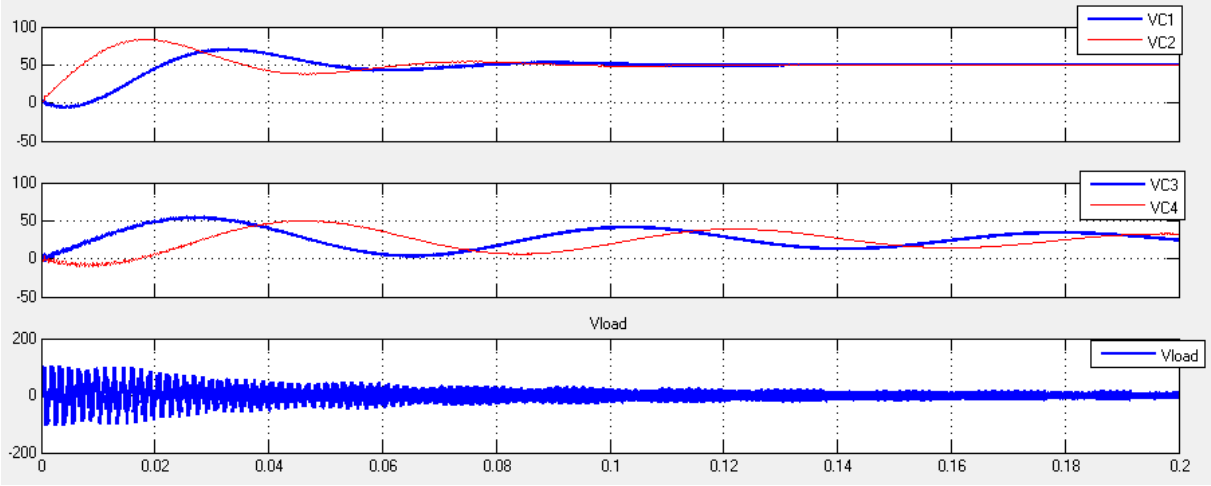

Fig B. 1: Capacitors' and load voltage waveforms for modulation index D =0

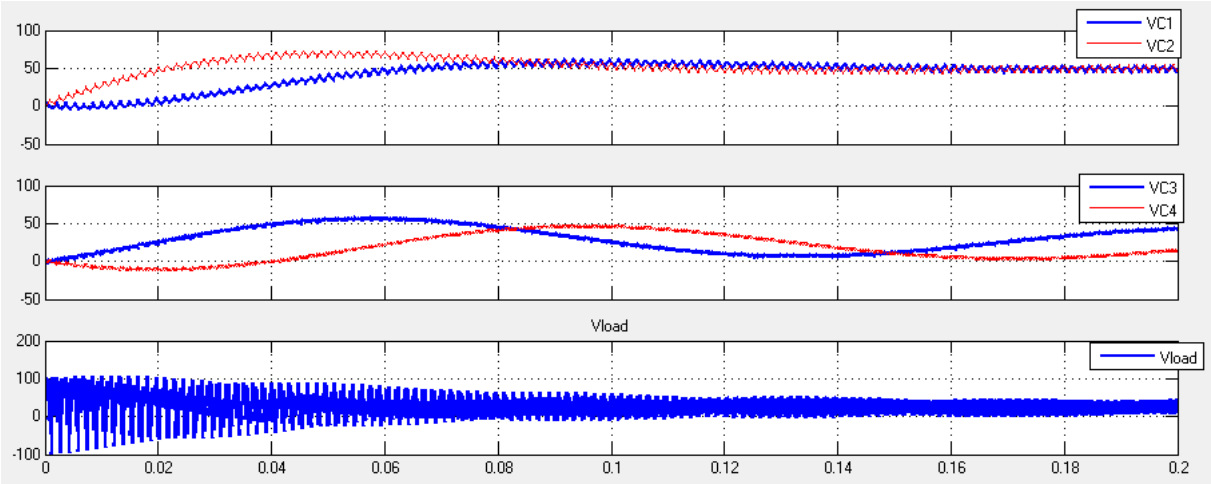

Fig B. 2: Capacitors' and load voltage waveforms for modulation index D =1/4

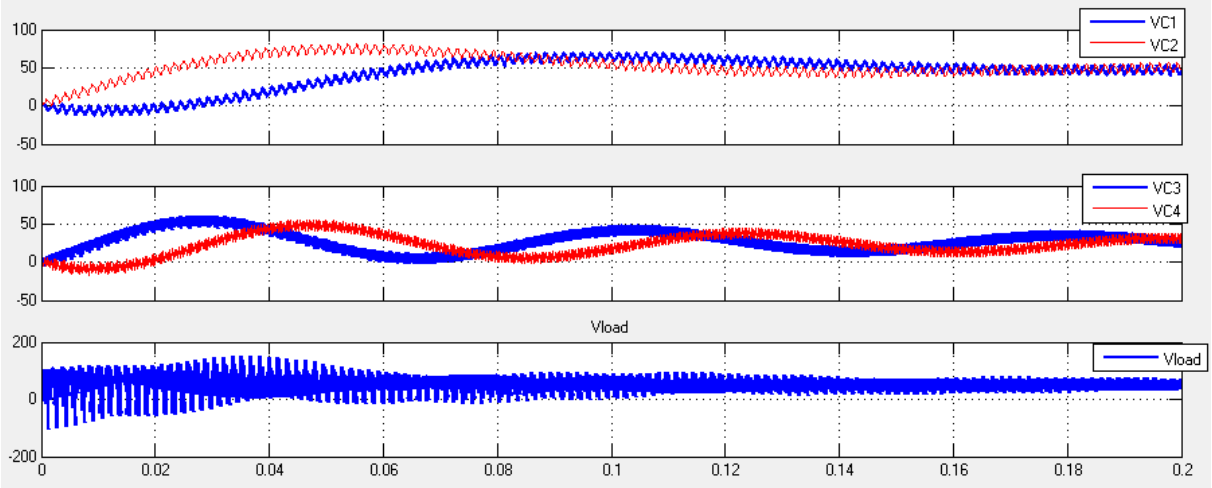

Fig B. 3: Capacitors' and load voltage waveforms for modulation index D =1/2

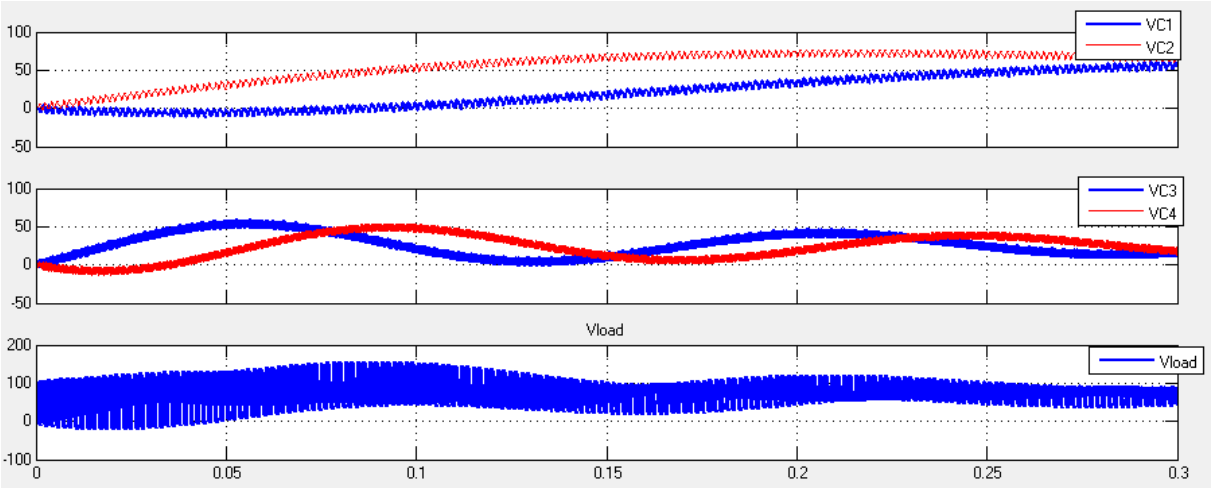

Fig B. 4: Capacitors' and load voltage waveforms for modulation index D =3/4

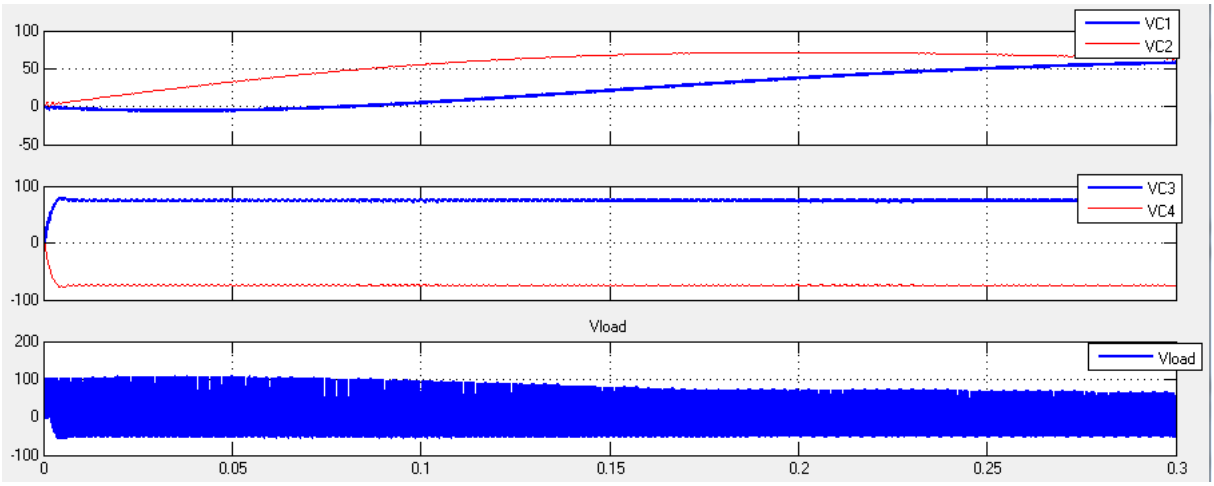

Fig B. 5: Capacitors' and load voltage waveforms for modulation index D =1

Appendix C: Balancing equations for AC PWM

Aperiodic oscillation frequency for AC PWM

$$\omega(M) = \begin{cases} (1-4M^2)\dfrac{T}{32LC} & 0 \le M \le \dfrac{1}{4} \\ \left(sin^{-1}\left(\dfrac{1}{4M}\right) - \dfrac{\pi}{4}(1+4M^2) + M\sqrt{16-\dfrac{1}{M^2}}\right)\dfrac{T}{8\pi LC} & \dfrac{1}{4} \le D \le \dfrac{3}{4} \\ \left(sin^{-1}\left(\dfrac{1}{4M}\right) + 3sin^{-1}\left(\dfrac{3}{4M}\right) - \pi(1+M^2) + \right. & \\ \left. +M\left(\sqrt{16-\dfrac{1}{M^2}} + \sqrt{16-\dfrac{9}{M^2}}\right)\right)\dfrac{T}{8\pi LC} & \dfrac{3}{4} \le D \le 1 \end{cases}$$

(C.1)

Aperiodic time constant for AC PWM

$$T_P(M) = \begin{cases} \dfrac{96\pi CL^2}{\left[\frac{\pi}{8} - \frac{3\pi}{4}M^2 + \frac{8}{3}M^3\right]T^2R} & 0 \le M \le \frac{1}{4} \\ \dfrac{768CL^2}{\left[\frac{1}{4}A(1-12M^2) + \frac{M}{3}D\left(\frac{7}{16} - 4M^2\right) + \frac{3\pi}{4}M^2 + \frac{8}{3}M^3\right]T^2R} & \frac{1}{4} \le D \le \frac{1}{2} \\ \dfrac{96\pi CL^2}{\left[\begin{array}{c}\frac{1}{4}A(1-12M^2) + B(1+6M^2) + \\ +\frac{M}{3}D\left(\frac{7}{16} - 4M^2\right) + \frac{M}{6}F\,(11-16M^2) \\ -\frac{9\pi}{4}M^2 + \frac{8}{3}M^3 - \frac{\pi}{2}\end{array}\right]T^2R} & \frac{1}{2} \le D \le \frac{3}{4} \\ \dfrac{96\pi CL^2}{\left[\begin{array}{c}\frac{\pi}{16} + \frac{1}{4}A(1-12M^2) + B(1+6M^2) - \frac{9}{8}C(1+4M^2) + D\frac{M}{3}\left(\frac{7}{16} - 16M^2\right) - \\ -E\frac{M}{4}\left(\frac{27}{8} - \frac{8M^2}{3}\right) + F\frac{M}{6}(11+16M^2)\end{array}\right]T^2R} & \frac{3}{4} \le D \le 1 \end{cases}$$

(C.2)

Periodic oscillation frequency for AC PWM

$$w(M) = \begin{cases} \left(\frac{3\pi}{2} - 8M\right)\frac{T}{32LC} & 0 \le M \le \frac{1}{4} \\ \left(\frac{\pi}{2} + 2sin^{-1}\left(\frac{1}{4M}\right) + 2M\left(\sqrt{16 - \frac{1}{M^2}} - \frac{1}{4}\right)\right)\frac{T}{32LC} & \frac{1}{4} \le D \le \frac{3}{4} \\ \left(\begin{array}{c}2\pi - 4sin^{-1}\left(\frac{1}{2M}\right) + 2sin^{-1}\left(\frac{1}{4M}\right) + 8M\left(\frac{\sqrt{16 - \frac{1}{M^2}}}{4} - 1\right) + \\ +\pi M^2 - 7M\left(\frac{\sqrt{4 - \frac{1}{M^2}}}{2}\right) - 2M^2 sin^{-1}\left(\frac{1}{2M}\right) + \sin\left(\frac{1}{2M}\right)\end{array}\right)\frac{T}{32LC} & \frac{3}{4} \le D \le 1 \end{cases}$$

(C.3)

Periodic time constant for AC PWM

$$T_P(M) = \begin{cases} \dfrac{2048CL^2}{\left[2\pi M^2 - 64M + 32\dfrac{\pi}{2}\right]T^2R} & 0 \le M \le \dfrac{1}{4} \\ \dfrac{2048CL^2}{\left[\dfrac{34\pi}{3} - 64M + \dfrac{25sin^{-1}\left(\frac{1}{4M}\right)}{3} - 4\pi M^2 + 32M^2 sin^{-1}\left(\frac{1}{4M}\right) + \right.} & \dfrac{1}{4} \le D \le \dfrac{1}{2} \\ \left. + \dfrac{91M\sqrt{\dfrac{16M^2-1}{M^2}}}{9} + \dfrac{32M^3\sqrt{\dfrac{16M^2-1}{M^2}}}{9}\right]T^2R & \\ \dfrac{48CL^2}{\left[\dfrac{64\pi}{3} - 64M - 20sin^{-1}\left(\frac{1}{2M}\right) + \dfrac{25sin^{-1}\left(\frac{1}{4M}\right)}{3} - 8M^2 sin^{-1}\left(\frac{1}{2M}\right) + \right.} & \dfrac{1}{2} \le D \le 1 \\ \left. + 32sin^{-1}\left(\frac{1}{4M}\right) - 22M\sqrt{\dfrac{4M^2-1}{M^2}} + \dfrac{91M\sqrt{\dfrac{16M^2-1}{M^2}}}{9} + \right. & \\ \left. + \dfrac{32M^3\sqrt{\dfrac{16M^2-1}{M^2}}}{9}\right]T^2R & \end{cases}$$

(C.4)

Appendix D: Matlab codes

General part: The general part is identical for all voltage levels, so only variable 'Comb#' should be changed throughout the code to get particular voltage level. Therefore, we have

```
FCC_leg = [-2 0 2]; % FCC leg
H_Bridge = [-1 0 1]; % H-Bridge
% combines the vectors (81 combinations possible)
Combs = combvec(FCC_leg,FCC_leg,H_Bridge,H_Bridge);
% combine the values of FCC and H-Bridge capacitors
Load_V = sum(Combs); % sum all the columns
% Compares the sums of the columnqs of cmbs
Comb0 = Combs(:,Load_V == 0); % voltage on the load = 0
Comb1 = Combs(:,Load_V == 1);% voltage on the load = 1/4
Comb2 = Combs(:,Load_V == 2);% voltage on the load = 1/2
Comb3 = Combs(:,Load_V == 3);% voltage on the load = 3/2
Comb4 = Combs(:,Load_V == 4);% voltage on the load = 1
% defines how many certain combinations of H-brige capactitors
are there

min_min = Comb0(:,Comb0(3,:) == -1 & Comb0(4,:) == -1);
% when states of C3 and C4 are minus and minus, respectively
plus_min = Comb0(:,Comb0(3,:) ==  1 & Comb0(4,:) == -1);
```

```
% when states of C3 and C4 are plus and minus, respectively
plus_plus = Comb0(:,Comb0(3,:) ==  1 & Comb0(4,:) ==  1);
% when states of C3 and C4 are plus and plus, respectively
min_plus = Comb0(:,Comb0(3,:) == -1 & Comb0(4,:) ==  1);
% when states of C3 and C4 are minus and plus, respectively
% size(xx,2)- calculates the number of columns
% combvec - makes all possible combinatios of the matrix
% combvec(1:size(mm,2),1:size(pm,2)) =
% 1     2     1     2     1     2
% 1     1     2     2     3     3
% therefore comb_new is the combination of 8 matrices
comb_new=combvec(1:size(min_min,2),1:size(plus_min,2),1:size(p
lus_plus,2),1:size(min_plus,2),...
1:size(min_min,2),1:size(plus_min,2),1:size(plus_plus,2),1:siz
e(min_plus,2));
% create new matrices length of a- number of 4x8 matrices
New_set  = zeros(4,8,length(comb_new(1,:)));
Topology{1} = zeros(4,8,length(comb_new(1,:)));
% initialize new variable-c
c = 0;
% creates a 'for' loop
% Here it defines whether the sum of the H-Bridge converters
voltages is
% zero
for ii = 1:length(comb_new(1,:))
    New_set(:,:,ii) = [min_min(:,comb_new(1,ii)),
plus_min(:,comb_new(2,ii)), plus_plus(:,comb_new(3,ii)),
min_plus(:,comb_new(4,ii)),...
                       min_min(:,comb_new(5,ii)),
plus_min(:,comb_new(6,ii)), plus_plus(:,comb_new(7,ii)),
min_plus(:,comb_new(8,ii))]; % takes the raw of mm-mp
according to the number in "q"
    if sum(New_set(3,:,ii)) == 0 && sum(New_set(4,:,ii)) == 0
% if the sum of third and fourth raw are equal to 0 then c
rises
        c = c + 1;
        Topology{1}(:,:,c) = New_set(:,:,ii);
    end
end

Topology{1} = Topology{1}(:,:,1:c);
clear temp
c = 0; % constant
for ii = 1:length(Topology{1}(1,1,:))
    s1 = Topology{1}(1,:,ii);
    s2 = Topology{1}(2,:,ii);
    for jj = 1:length(s1) % from 1 to 8
        if all(s1==circshift(s2,[0,jj])) ||
all(s1==circshift(fliplr(s2),[0,jj]))
            c = c + 1;
            temp(c) = ii;
```

```
            break
        end
    end
end
Topology{1} = Topology{1}(:,:,temp);
```

'Number_of_Switching' function

```
function N = Number_of_Switching(L1,L2) % number of switchings
function
c = [zeros(size(L1)),zeros(size(L1)),zeros(size(L1,1),1)]; %
creates the matrix c = 4x17
c(:,1:2:(size(c,2)-2)) = sign(L1); % fils the signs of the
level into the odd number slots
c(:,2:2:(size(c,2)-1)) = sign(L2); % fils the signs of the
level into the even number slots
c(:,     size(c,2)   ) = sign(L1(:,1)); % takes the sign of
the first column into the 17th
N = sum(sum(abs(diff(c,1,2)))); % calculates the number of the
sign changes (error as it calculate the diff of 1 and -1 as 2
switchings)
```

Secondary part of the code, is dedicated to select topologies with least number of switching and make 16 topologies out of 8.

```
NS00 = NaN(size(Topology{1},3),1); % Not a Number (NaN)
for ii = 1:size(Topology{1},3) % from 1 to the number of
combinations (r,c,N=40)== 1:40
    NS00(ii) = NumSw(Topology{1}(:,:,ii),Topology{1}(:,:,ii));
% NS00 == function NumSw (which calulates the number of
switchings)
end
M = min(NS00(:)); % finds the minimum value in the array
[L0w0] = find(NS00 == M); % finds what elements are equal to M
(minimal value of switchings)
for k = 1:length(L0w0) % k from 1 to the length of L0w0
    Output00{k}(:,1:8) = Topology{1}(:,:,L0w0(k));
    Output00{k}(:,9:16) = Topology{1}(:,:,L0w0(k));
end
celldisp(Output00)
```