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APPLIED RESEARCH

Realization of Arithmetic Logic Units Using Electro-Optic Microring Resonators in Photonic Circuits

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ABSTRACT This work presents a new approach to designing Arithmetic Logic Units (ALUs) using electro-optic microring resonators. The methodology covers the demonstration of full and half addition and subtraction, parity checking, and dynamic logic gates functionalities at the data speed of 10 Gbps. In this work, integrated electro-optic circuits have been meticulously designed to have minimum footprints using microring resonators (MRRs) with low losses, thus, ensuring efficient and scalable optical computing system. A unique design for electro-optic full adder/subtractor and three input odd-even parity checkers were implemented and validated successfully within the Lumerical simulation environment. Simulation results demonstrate the successful alignment of optical outputs with their respective truth tables, confirming the reliability and accuracy of the designed circuits. These advancements represent significant progress in the field of optical computing, offering notable improvements in computational speed, efficiency, and scalability. This research contributes to the ongoing exploration and development in optical computing, with the potential to revolutionize computational efficiency and performance in various applications.

INDEX TERMS Arithmetic logic units (ALUs), electro-optic microring resonators, photonic circuits, optical computing, Lumerical simulation, addition, subtraction, parity checkers, dynamic logic gates.

I. INTRODUCTION

In the realm of computing, the quest for faster, more efficient, and scalable processing units has been a driving force behind technological advancements. Traditional electronic Arithmetic Logic Units (ALUs) have long served as the backbone of digital computation, performing essential operations such as addition, subtraction, and logical functions. However, the inherent limitations of electronic circuits, including heat dissipation and speed constraints, have spurred researchers to explore alternative paradigms such as optical computing [1].

The motivation for designing optical ALUs stems from the unique advantages offered by optics, including high-speed data transmission, low power consumption, and potential for parallel processing [2]. At the heart of optical ALUs, electro-optic micro ring resonators (MRR) have garnered significant interest due to their compact size, low energy consumption, and compatibility with integrated photonic circuits [3], [4].

In the optical ALU domain, numerous research efforts have contributed significantly to the advancement of optical computing. Notable studies have focused on electro-optic micro ring resonators and their applications in constructing essential components of arithmetic logic circuits, including logic gates, comparators, and half adders. The use of modulated

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micro ring resonators in constructing logic gates was explored in [5] and [6], where the logical resonance shifts in modulated MRRs resulted in intensity changes. The combination of several such MRRs enables the emulation of logic gates based on the output intensity of the structure. Apart from optical logic gates, optical comparators [7], and half adder [8], full adder [9], and subtractors [10], [11], have been developed.

The previous work from our team [8] focuses on designing half adder, and this works aims to create the design for complex ALU circuits. The main focus is designing a ALU with Full adder, subtractor, and parity checkers operations and with reduced footprint, as well as optimized operation time.

II. BACKGROUND WORK

A. LOGICAL FUNCTIONS

The aim of the proposed circuit is to develop logical circuits that utilize combinations of multiple logic gates, including half-adders, full adders, half-subtractors, full subtractors, parity checkers, and multipurpose dynamic logic gates. These circuits use common logic gates such as XOR ($\oplus$), AND ($A{\cdot}B$), and NOT (A'). Their functions are implemented using traditional logic gate circuits as shown in the accompanying tables. The descriptions of these circuits are provided below:

1. **Half Adder**: Adds two single-bit binary numbers, producing a sum and a carry output [12].
2. **Half Subtractor**: Subtracts two single-bit binary numbers, producing a difference and a borrow output [12].
3. **Logic gates**. Includes OR/NOR, XOR/XNOR, AND/NAND gates.
4. **Full Adder**: Adds two input bits (A, B), taking (carried input C) into account producing a sum and a carry output [13].
5. **Full Subtractor**: Subtracts two input bits (A, B) and taking (borrowed input C) into account, producing a difference and a borrow output.
6. **Parity checker:** A parity bit is an extra binary bit added to a binary string code. Even parity adjusts to the total number of 1s, with the parity bit becoming 1 for an even number of 1s, otherwise 0 [14].

B. FUSION & SIMILARTIES IN THE LOGICAL FUNCTIONS

To achieve an integrated optical circuit, our design focuses on two primary functional components: address control unit and logic units. For the address control, we implemented a 2:4 decoder with inputs D1, D2, and X for logic switching. These inputs dictate which logic outputs are activated, as detailed in Table 1. The 2:4 decoder directs signals towards four different logic sections: Half Adder/Half Subtractor, Full Adder/Full Subtractor, OR-NOR/XOR-XNOR, and AND-NAND circuits. And X switch is instrumental within the section. In the design, it switches half adder to half subtractor, full adder to full subtractor, and or-nor to xor-xnor by using the X switching function. The control of the output functions including the X switch signal is shown in Table 1.

The corresponding truth tables for these circuits with respect to inputs A, B, and C are presented in Table 2. Table shows the output value corresponding to inputs A, B, C.

To optimize the design of these logic elements and minimize the overall complexity of the combined circuit, we leveraged the operational similarities between certain logic units. For instance, although half adders and half subtractors perform different operations, their 'sum' and 'difference' outputs are governed by identical logic of $A \oplus B$. This allows for the unification of these two circuits on a common output port, using a shared 'sum/difference' output, as shown in Table 2.

In developing combined OR/NOR and XOR/XNOR logic units, we designed a circuit that seamlessly transitions between these functions via a command from the X input, ensuring that the design remains simple and efficient (Table 1). The inclusion of AND/NAND logic circuits (Table 2), completes our design for the optical logic gates.

For the arithmetic functions, the full adder and full subtractor logic, we observed that both share common logic for their sum and difference outputs (Table 2). The carry logic of a full adder is defined as $\text{Carry} = A{\cdot}(B + C) + B{\cdot}C$, while the borrow logic for a full subtractor is expressed as $\text{Borrow} = A'{\cdot}(B + C) + B{\cdot}C$. The primary difference between these two lies in the use of A and A'. By introducing the X variable, similar to the logic gate circuit example, we can manipulate the value of A, further streamlining the design. Hence, by introducing X switch function together with the address bits, D1 and D2, forms the address control unit which decides the functions to be carried out between the input bits. This completes the basic implementation of optical ALU with core logical and arithmetic functions.

TABLE 1. Control addresses.

Inputs			Selected Outputs
X	D1	D2	
0	0	0	Full adder
0	0	1	Half Adder
0	1	0	OR, NOR
0	1	1	AND, NAND
1	0	0	Full Subtractor
1	0	1	Half Subtractor
1	1	0	XOR, XNOR
1	1	1	AND, NAND

C. BACKGROUND OF OPTICAL HALF ADDERS AND XOR LOGICS

The implementation of a half adder using MRRs is demonstrated in [8], utilizing optical signals as outputs (Fig. 1). This structure consists of sum and carry output channels, and A and B modulation voltages that modulate three MRRs. As single-wavelength light travels through the waveguides and MRRs, the modulation of these MRRs, whose resonance matches the wavelength of the light source, determines the

TABLE 2. Dynamic OR/NOR to XOR/XNOR logic.

Inputs / Outputs	A :	0	0	0	0	1	1	1	1
	B :	0	0	1	1	0	0	1	1
	C :	0	1	0	1	0	1	0	1
O1: Half adder Sum, H. Subtractor Difference		0	0	1	1	1	1	0	0
O2: Half Adder Carry		0	0	0	0	0	0	1	1
O2: Half Subtr. Borrow		0	0	1	1	0	0	0	0
O3: Full Adder Sum, Full Subtr. Diff		0	1	1	0	1	0	0	1
O4: Full Adder Carry		0	0	0	1	0	1	1	1
O4: Full Subtr. Borrow		0	1	1	1	0	0	0	1
O5: NOR		1	1	0	0	0	0	0	0
O5: XNOR		1	1	0	0	0	0	1	1
O6: OR		0	0	1	1	1	1	1	1
O6: XOR		0	0	1	1	1	1	0	0
O7: NAND		1	1	1	1	1	1	1	1
O8: AND		0	0	0	0	0	0	1	1

path of the light source by resonance shift. This configuration enables the construction of the half adder logic. In the optical half adder model (Fig. 1), the modulated resonance of A and B MRRs matches the wavelength of the propagating optical signal. Whenever they receive a modulation signal, the states of the 'Sum' and 'Carry' outputs change, creating the half adder logic. In addition to these designs, the design of half and full subtractors using all-optical MRRs based on polarization switches was introduced in [15]. Similarly, half adders and full adders were also designed using the same principle [16].

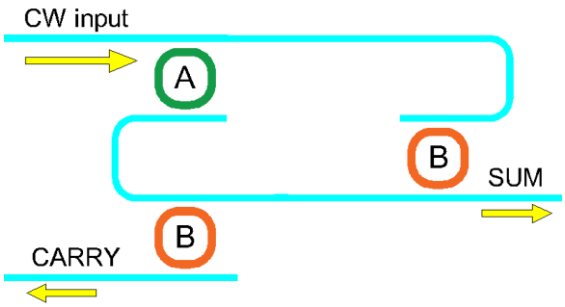

FIGURE 1. Optical half adder design (implemented from Alipbayeva et al. [8]).

Another significant optical logic circuit is the AND/NAND logic gate developed by Azhigulov et al. [6], as shown in Fig. 2. This circuit demonstrates light traveling in modulated MRRs functioning as AND/NAND logic gates. This circuit offers a simplistic form of an AND/NAND optical logic gate and ensures its integration into more complicated circuits.

III. PROPOSED OPTICAL ALU DESIGNS

The design of the proposed ALU is shown in Fig.3. The architecture uses a 2:4 decoder to route optical signals

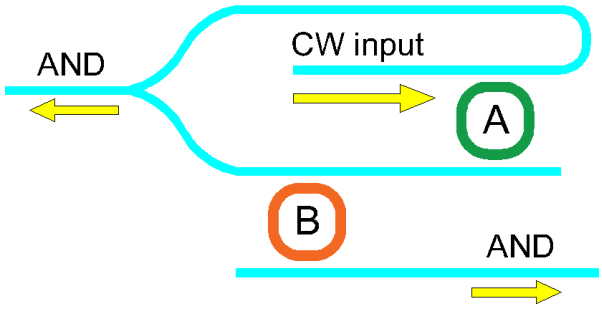

FIGURE 2. Optical XOR/XNOR logic gate design by Azhigulov et al. [6].

based on the address Bits D1 and D2: **01** for the half adder/subtractor, **00** for the full adder/subtractor, **10** for NOR/OR and XOR/XNOR, and **11** for AND/NAND gates. The decoder is positioned on the left side of the model, directing light into one of these four paths. The right side contains the corresponding logic circuits, each accepting inputs A, B, and C, with an additional input X for in-circuit switching to control specific operations. The X switch utilizes the use of similar outputs of different functions and only switching the dissimilar output functions while carrying out the arithmetic and logic functions.

A. HALF ADDER/SUBTRACTOR DESIGN (ADDRESS 01)

The design of the half adder-subtractor is obtained by modifying the design of the half adder in Fig. 1. Here 'Sum'' and 'Difference' has same logic (A XOR B), and hence the same output channel, O1. Moreover, Half Adder Carry has logic of A·B, and Half Subtractor Borrow has logic of A'·B.

Here, additional waveguides were added to create the borrow part for the half subtractor. The half subtractor's borrow part follows the logic of A' B, meaning it does not need to couple to A but to B. To create this logic, we added a waveguide splitter after the through port of A. The arm of the splitter coupled to right side B MRR. Since it couples to the opposite side of the 'carry', the output goes to the opposite side of the lower waveguide when coupled to B without interfering with the 'carry' output. As for the 'difference', the sum and difference outputs in half adders and half subtractors follow the same logic of A⊕B.

B. FULL ADDER/SUBTRACTOR DESIGN (ADDRESS 00)

In the path of full adder, full subtractor, the output of sum, and difference follow the same logic of C⊕(A⊕B). This can also function as 3 input even parity. This section is located in 00 address, and of it at top side. Here, the circuit need to give 0,1,1,0 at different values of B, C when A = 0, and 1,0,0,1 when A =1. In order to create circuit, that gives 1 output, when either B or C is 1, but 0 when both are positive or 0 (A = 0 situation), we used specific circuit that carries light from drop port of C [C =1] to the coupling section of B. If B = 0, light take direction to output without coupling B, after passing waveguide crossing. If C = 0, B = 1, light does

not couple C MRR, and B MRR sends light signals directly to the output. In the case of A = 1, light enters from left side of B, and C system, as opposed to previous right side. As a result, it performs reverse logic.

As for Full Adder Carry output, the lower left of 00 section produce 1 output if A = 1, and either or both of B and C is 1. And right side produce one if B = C = 1. This completes logic of Full Adder Carry. And X MRR swaps light going to optical input of A MRR to its add-drop input, effectively switching logic of A to A'. Thus turning Full Adder Carry to Full Subtractor Borrow.

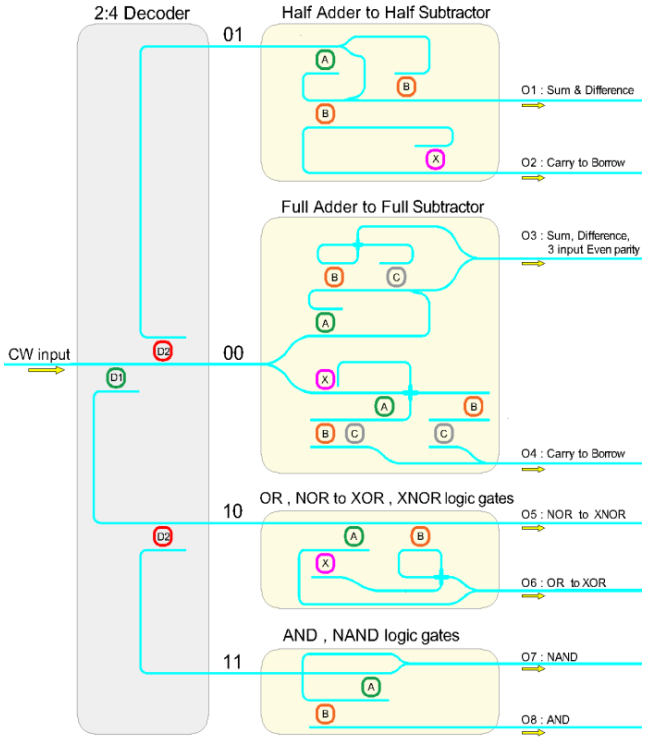

FIGURE 3. Proposed design involving half adder/subtractor, full adder/subtractor, and logic gates.

C. LOGIC GATES (ADDRESS 10, 11)

The basis of OR, NOR to XOR, XNOR logic gate is obtained from design of OR, NOR optical circuit consisting of two A, B input MRRs laid between two parallel waveguides [17]. This was modified by adding X input MRR. If X = 0, it acts as OR, NOR logic gate, directing light to OR output if either of A, B is 1. When X = 1, and A = B = 1, it directs light XNOR channel (previously NOR), instead of XOR (previously OR), changing OR, NOR logic circuit to XOR, XNOR circuit. Apart from them, AND-NAND section is obtained from employing design in Azhigulov et al. [6] (Fig. 2).

IV. RESULTS

To optimize the modulation depth and achieve a high extinction ratio in the add-drop MRR, an optical microring resonator (MRR) based on silicon (Si) was designed with carefully chosen parameters. The device features a p-i-n doped modulation region for efficient electro-optic modulation and is based on the analysis of MRR designs in Nurgali et al., 2024 [18]. These design parameters ensure a balance between high extinction ratio and high-speed operation and are utilized in both spectral and time-domain simulations. A detailed summary of the design parameters used for model's Lumerical simulation is provided in Table 3.

TABLE 3. Parameters of MRR used in simulation.

Parameters of MRRs	Values
Waveguide width, ridge height, slab height.	0.5 um, 0.16 um, 0.08 um.
Ring radius, coupling length, coupling gap.	7 um, 1 um, 0.2 um.
Waveguide doping type	p-i-n
Input-to-Ring Coupling Ratio	0.145
Ring-to-Drop Coupling Ratio	0.145
Resonant wavelength	1549.1 nm
Extinction Ratio (Through Port)	10.71dB
Extinction Ratio (Drop Port)	0.061dB
Resonance Width (Drop Port)	0.7 nm
Resonance shift	2.2 nm

The resonance shift under modulation is displayed in Fig. 4. The propagating light wavelength is chosen at the resonance peak of V = 0.7 a.u modulation, which is below the p-i-n junction threshold. At this state, the signal can travel through the MRR cavity without significant intensity loss. Another state, V = 1.3 a.u, is chosen to shift the resonance filter of the MRR so that it does not couple the propagating light into the ring cavity. Fig. 4a and 4b show the deep resonance depth at V = 0.7 a.u, corresponding to the add-drop and add-through ports. We selected the laser wavelength at this point to achieve higher yield.

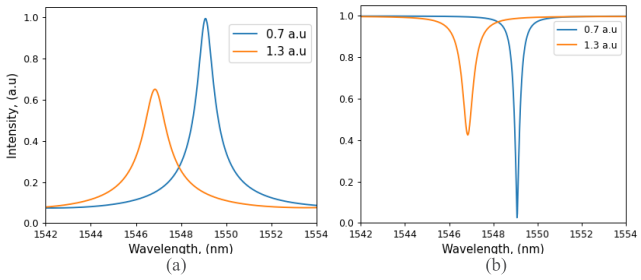

FIGURE 4. Optical spectrum of resonance shifts of modulated MRR: (a) drop port, (b) through port.

In the time-domain simulation, the proposed model was implemented in Lumerical Interconnect, based on the schematic shown in Fig. 3. A uniform optical signal with a wavelength of 1549.1 nm was chosen, which corresponds to the peak of the V = 0.7 a.u modulation state in Fig. 4. This wavelength was selected to maximize the light coupled into the drop port of the MRR, with the modulation voltage of V = 0.7 a.u set as the '1' state. In this configuration, a modulation voltage of V = 1.3 a.u (1.3 a.u - 0 a.u) represents the '0' state, while V = 0.7 a.u (1.3 a.u - 0.6 a.u)

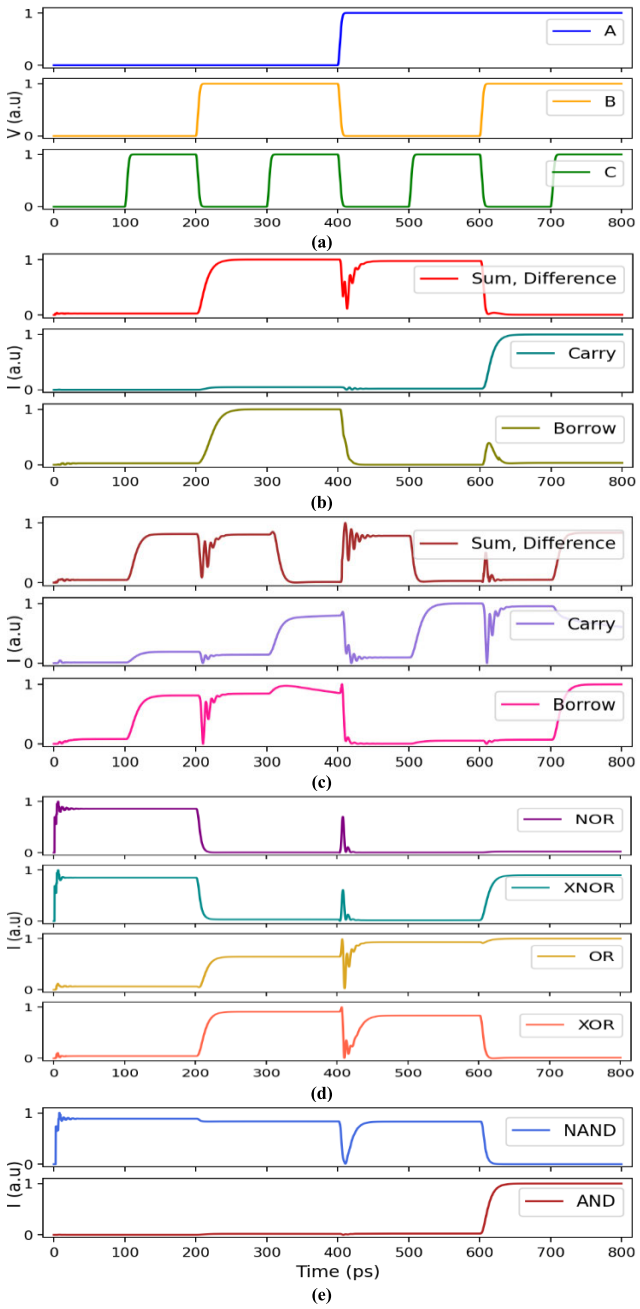

FIGURE 5. Time domain results model in Lumerical according to table 2: a) A, B, C inputs, b) Sum/difference, carry, borrow outputs of half adder and half subtractor, c) Sum/difference, carry, borrow outputs of full adder and full subtractor d) dynamic NOR/XNOR and OR/XOR results, e)NAND/AND results.

represents the '1' state. The waveguide lengths and proportions were adjusted to match the model. The simulation was performed at a bitrate of 10 Gbps, with the results shown in Fig. 5, which displays normalized outputs. The simulation used 8-bit sequences (A, B, and C) representing all possible combinations of the three inputs: 00001111, 00110011, and 01010101, matching the input-output truth table for the logic units in Table 2. With a 10 Gbps bitrate, the sequence window was 800 ps. The figure shows the logic outputs for: (a) inputs, (b) half adder to half subtractor, (c) full adder to full subtractor, (d) OR-NOR to XOR-XNOR, and (e) AND-NAND sections. The desired logic unit was selected through addressing modulation, as outlined in Table 1. The obtained results align with the truth tables, confirming the accuracy and effectiveness of the design.

V. PERFORMANCE ANALYSIS

A. LOSS ANALYSIS

The losses in the proposed integrated optical circuit design can be attributed to four primary components: microring resonators (MRRs), straight and bending waveguides, Y-junctions, and waveguide crossings.

Losses associated with MRRs arise from two scenarios: first, when the wavelength of the light propagating through the waveguide is not in resonance with the MRR, and second, when the wavelength is in resonance, resulting in coupling to a second waveguide via the MRR cavity. In the former case, even though the wavelength is not resonant, a portion of the light is still coupled to the MRR, leading to a decrease in the overall intensity of the propagating light. The extent of these losses depends on the resonance width and the deviation of the signal's wavelength from the resonance, as depicted in the resonance spectrum of the MRR in Fig. 4. Each resonance peak exhibits an off-resonance insertion value, even at neighboring resonant wavelengths. Although reducing the resonance width by decreasing the coupling coefficient can minimize these losses, it also results in longer rise and fall times, thereby slowing the MRR's response speed [18].

In the latter case, where the wavelength is in resonance with the MRR, the majority of the light couples to the MRR. However, bending losses occur, which increase as the radius decreases and the waveguide width narrows [18]. Additionally, in doped electro-optic modulated MRRs, increasing the modulation voltage raises the number of charge carriers in the cavity waveguide. This increase in charge carriers elevates the imaginary part of the refractive index, thereby accumulating losses in the ring cavity [19]. To mitigate these losses, we selected the wavelength of the propagating signal at a lower modulation state (v = 0.7 a.u.), as illustrated in Fig. 4. This approach significantly reduced cavity losses in the design.

In the simulation of MRRs, light passing through the MRR cavity retains 98.6% of its input intensity (0.061 dB loss), while light propagating through the waveguide in a non-resonant condition retains 95.5% (0.195 dB loss). Although these loss values are minimal individually, they accumulate significantly in complex designs with multiple integrated MRRs. Figure 6 illustrates the intensity outputs from single MRRs (Fig. 6a), from a waveguide with a non-resonant wavelength coupled to multiple MRRs (Fig. 6b), and from the signal coupled to the cavity of multiple MRRs (Fig. 6c). The respective placements of MRRs in these simulations are shown in the top and bottom sections of Figure 6d. While a single MRR incurs minimal loss

or distortion, the overall intensity drop at a wavelength coupled to multiple non-resonant MRRs is attributed to coupling losses, and signal distortion at the optical signal coupled to the cavity of multiple MRRs is due to delays in the MRRs.

In addition to MRR-related losses, optical losses also occur in bent and straight waveguides, as well as in waveguide splitters and combiners. In Lumerical MODE simulation, the losses in a straight waveguide were measured at 10^{-4} dB/cm, while in bent waveguides, they were 22 dB/cm for a 4 μm bend and 3.13 dB/cm for a 5 μm bend radius with waveguide parameters used in simulation. This implies that the input signal retains 96% and 99.7% of its intensity after passing through five bent waveguides with 4 μm and 5 μm bends, respectively, while no significant loss occurs in straight waveguides within the design limits.

Regarding Y-junctions, Alam et al. reported an excess loss of 0.52 dB for a Y splitter [20]. In contrast, Yi et al. demonstrated a power splitter with low excess losses of 0.21 dB for the 1500–1600 nm range [21]. As for the Lumerical MODE simulation with the model's ridge waveguide Y-branch, the insertion loss was observed to be 3 dB. Additionally, each output branch of the Y-splitter consistently receives less than half of the incoming signal, leading to discrepancies in signal intensities between the circuit branches.

At waveguide crossings, power losses can occur due to mode mismatch or scattering at the intersection points. Zhang et al. reported insertion losses varying from 0.13 to 0.27 dB in fabricated wafers, while Lu et al. and Kim et al. showed insertion losses of 0.086 dB and 0.078 dB, respectively [22], [23], [24]. In the simulation, with the model's parameters, the estimated insertion loss for the crossing was 0.04dB.

To maintain uniform intensity levels across output channels, it is crucial to account for the losses incurred by waveguide splitters, MRRs, and crossings. In the case of the half-adder sum and half-subtractor difference, both [A = 0, B = 1] and [A = 1, B = 0] logic paths involve splitters, resulting in equal normalized outputs. Other output channels also feature input paths with a similar number of splitters and MRRs, ensuring consistency in signal processing.

B. DELAY ANALYSIS

In Lumerical simulations, we estimated the delay for signals traversing waveguides and MRRs. Silicon waveguides exhibit a short and uniform delay of 1.16 ps per 100 μm at a refractive index of 3.48, which is negligible compared to the 100 ps required for each bit. However, MRRs introduce more significant delays by storing signals in their cavities and releasing them, causing distortion at the start and end of signals.

The distortions in the signal attributed to multiple MRRs arise from the optical signal making multiple rotations before exiting the ring cavity. MRRs can store and discharge the optical signal, causing the output to initially have reduced intensity and then exhibit a gradual decline once the signal ends. This results in a rectangular input signal having rise

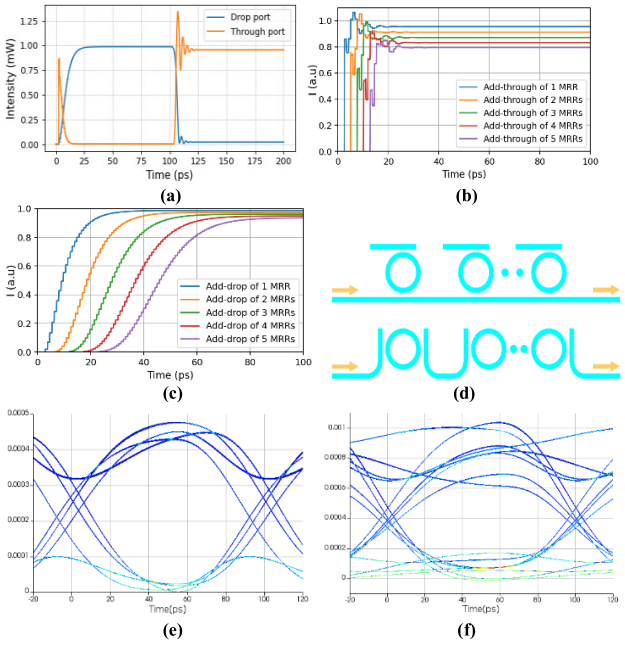

FIGURE 6. Delay simulation of the MRR in the proposed design. (a) Step response of the MRR. (b) Delay and intensity reduction of non-resonant optical signal through coupling region of the MRRs. (c) Delay of resonant optical signal coupled to MRRs. (d) MRRs placements for deriving series delays and loss. (f) Eye diagram of Sum/Difference of full adder/subtractor [O3]. (d) Eye diagram of Carry/Borrow of full adder/subtractor[O4].

and fall edges at the output. As shown in Figure 6c, the rise time of the signal becomes longer as the number of MRRs increases. The rise time, defined as the time for the signal to reach 90% of its saturation level, increases from 20 ps for a single add-drop MRR to 30 ps and 40 ps for the second and third MRRs, respectively. At a 10 Gbps operation speed, using more than four add-drop MRRs in a single path can lead to significant signal degradation.

The step response of a single modulated MRR is shown in Fig. 6a, while the cumulative delays in more complex paths are displayed with eye diagrams in Figs. 6e and 6f. These diagrams correspond to the Sum/Difference (O3) and Carry/Borrow (O4) outputs of a full adder/subtractor, which involve multiple MRRs in their light paths. Fortunately, the output remains clear, as no positive intensity amplitude falls below 50% of the highest value, ensuring reliable performance despite the distortion.

In the proposed design, elementary circuits such as the half adder and subtractor utilize two MRRs within a single optical path, ensuring minimal signal losses and efficient propagation. More complex circuits, including the full adder and subtractor, incorporate three MRRs, which result in increased losses and delays. Additionally, waveguide splitters and crossings further influence the output intensities. Despite these variations, the analysis confirms the design's capability to generate distinct logic outputs while maintaining the desired levels of complexity and operational speed. The additional parameters of the PIC components used in simulation, including delays and optical losses, are detailed in Table 4.

TABLE 4. Loss and delay values of implemented PIC parts in the simulation.

Elements	Optical Loss (dB)	Delay (ps)
Straight waveguide 100 um	10^{-6}	1.33
Bent waveguide r = 4um, 180°	0.028	0.167
Bent waveguide r = 5um, 180°	0.005	0.209
MRR, through port, r = 7um, k = 0.145	0.195	10 (ripple)
MRR, drop port, r = 7um, k = 0.145	0.061	20 (rise time)
Y waveguide	3	varies
Waveguide crossing	0.04	varies

VI. CONCLUSION

Our work demonstrates the feasibility of designing complex Arithmetic Logic Unit (ALU) circuits using electro-optic microring resonators. We successfully developed and simulated parity checker, half adders, full adders, and subtractors. Despite the complexity of these designs, the output signals exhibited uniform 0 and 1 amplitudes with minimal distortion. The simulations, conducted at a high speed of 10 Gbps, revealed no significant distortion, highlighting the reliability of this approach. Consequently, this study concludes that it is entirely possible to integrate these circuits into a single board, paving the way for the development of sophisticated integrated circuits using electro-optic microring resonator technology.

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