IET Power Electronics

Rapid Communication

Analytical current THD evaluation for three-phase voltage source inverters

ISSN 1755-4535
Received on 22nd October 2019
Revised 27th November 2019
Accepted on 13th December 2019
E-First on 2nd January 2020
doi: 10.1049/iet-pel.2019.1257
www.ietdl.org

Zhansen Akhmetov[1] ✉, Alex Ruderman[1]

[1]Department of Electrical and Computer Engineering, School of Engineering and Digital Sciences, Nazarbayev University, Nur-Sultan, Kazakhstan

✉ *E-mail: zhansen.akhmetov@nu.edu.kz*

Abstract: This study addresses the calculation of current total harmonic distortion (THD) for three-phase (3P) pulse-width modulation (PWM) inverters. First, it demonstrates how an analytical approach to PWM current ripple normalised mean square (NMS) calculation introduced in the late 1980s for a two-level (2L) inverter can be used for current THD evaluation. Second, it is shown how to evaluate current THD for a three-level (3L) 3P inverter using the current ripple NMS concept. Though considered is a 3P cascaded inverter with one H-bridge per phase, the results are applicable to popular 3L neutral point clamped (T-type) and flying capacitor inverters.

1 Introduction

Over the past 10–15 years, the power electronics community has shown significant interest in current total harmonic distortion (THD) analysis. Most papers end up with numerical THD evaluation by built-in simulation tools based on fast Fourier transform. The frequency domain analytical approach that involves a double Fourier series does not deliver simple THD expressions [1].

Simple closed-form voltage THD formulas for an arbitrary inverter level count [2] are obtained in time domain assuming the large ratio of switching-to-fundamental frequencies. Such asymptotic formulas are quite accurate for (apparent) switching to fundamental frequency ratios >25–30.

2L SP and 3P pulse-width modulation (PWM) inverter current THD may be evaluated based on harmonic distortion factor time domain analysis [1]. It originates from the 1988 paper [3] that assumed a purely inductive load for current ripple calculation purpose (frequency weighted THD approximation equivalent [1]) and a steady-state PWM current ripple on a PWM period.

In [3], the researchers focused mostly on additional PWM induced loss and had no interest in current THD. In [1], there are hints about current THD calculation for 3P RL-loads (induction motor loads) but it does not present explicit formulas.

The above approach is generalised in [4] for an SP multilevel voltage source PWM inverter with an arbitrary level count. For a 3P PWM inverter, current THD is increased due to a line-to-line voltages zero-sequence that results in a non-uniform line-to-line voltage pulses' time distribution. As the zero sequence depends on the modulation strategy, current THD will be different for different strategies [1, 3].

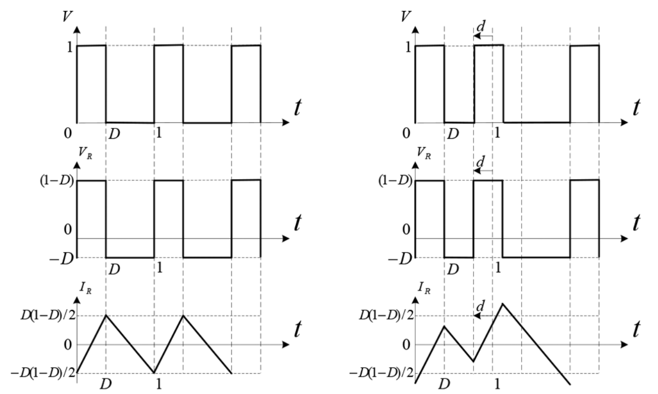

Fig. 1 *Normalised voltage, voltage and current ripples on a PWM period*
(a) SP, **(b)** 3P inverter with normalised offset

2 Current THD for a 2L 3P inverter

Voltage pulses of a 2L SP inverter have apparent switching frequency (2 × PWM carrier one) and are evenly distributed. PWM current ripple is derived from the voltage ripple (Fig. 1*a*) assuming pure inductive load and its normalised mean square (NMS) on a PWM period equals [4]

$$\mathrm{NMS}_2^{\mathrm{DC}}(D)_{1\mathrm{p}} = D^2\left(1 - 2D + D^2\right)/12. \qquad (1)$$

For a 3P inverter, two line-to-line voltage pulses are unevenly spread on a PWM period with a normalised offset d (Fig. 1*b*) and then current (ripple) NMS becomes

$$\mathrm{NMS}_2^{\mathrm{DC}}(D,d)_{3\mathrm{p}} = D^2\left(1 - 2D + D^2 + 3d^2\right)/12. \qquad (2)$$

For a 2L SP PWM inverter, the two references

$$V_a = m\sin\tau;\ V_b = -m\sin\tau, \qquad (3)$$

where modulation index $0 < m < 1$; $\tau = \omega t$ is the electrical angle (time). 'Differential mode' (duty cycle) and 'common mode' (offset) commands equal

$$\begin{aligned} D(\tau) &= (V_a - V_b)/2 = m\sin\tau;\\ d(\tau) &= (V_a + V_b)/2 = 0. \end{aligned} \qquad (4)$$

For a 3P inverter with sine-triangle PWM (STPWM), to obtain the same line-to-line AB voltage reference $D(\tau)$ (4), the required PWM phase A, B voltage commands (references) scanned by triangular carrier become (Fig. 2)

$$V_a = \frac{2}{\sqrt{3}}m\sin(\tau - \pi/6);\ V_b = \frac{2}{\sqrt{3}}m\sin(\tau - 5\pi/6) \qquad (5)$$

and the normalised 'common mode' voltage –

© The Institution of Engineering and Technology 2020

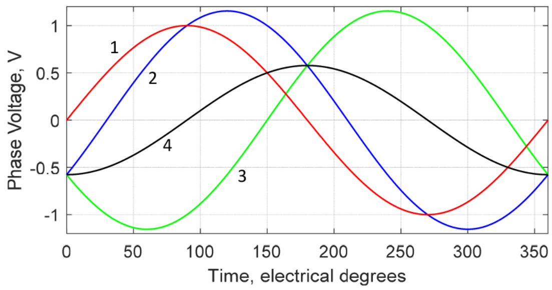

Fig. 2 *3P PWM voltages for STPWM: 1 – line-to-line AB voltage (differential mode D); 2 – leg A command; 3 – leg B command; 4 – line-to-line 'common mode' voltage (offset d)*

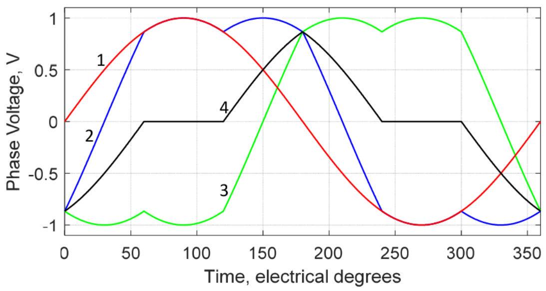

Fig. 3 *3P PWM voltages for SVPWM: 1 – line-to-line AB voltage (differential mode D); 2 – leg A command; 3 – leg B command; 4 – line-to-line 'common mode' voltage (offset d)*

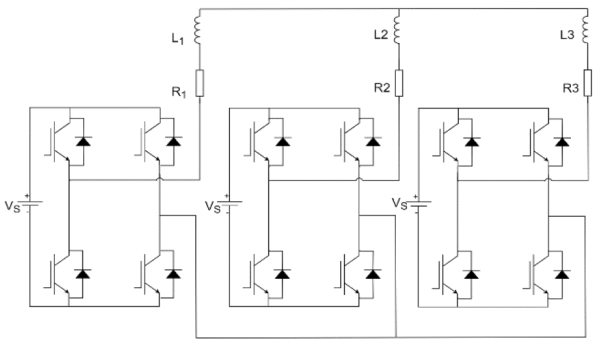

Fig. 4 *3P CHB inverter with one H-bridge per phase*

$$d(\tau) = (V_a + V_b)/2 = -m\cos\tau/\sqrt{3}. \qquad (6)$$

Current NMS for AC PWM by averaging that for DC PWM (1), (2) on (a quarter of) a fundamental period becomes

$$\mathrm{NMS}^{\mathrm{AC}}(m) = \frac{2}{\pi}\int_0^{\pi/2} \mathrm{NMS}_2^{\mathrm{DC}}(D(\tau), d(\tau))\mathrm{d}\tau. \qquad (7)$$

For a 2L SP inverter

$$\mathrm{NMS}_2^{\mathrm{AC}}(m)_{1\mathrm{p}} = \frac{1}{24}m^2 - \frac{2}{9\pi}m^3 + \frac{1}{32}m^4. \qquad (8)$$

For a 2L 3P inverter, the contribution of $3D^2d^2$ term in (2) amounts to $m^4/8$ that added to (8) gives

$$\mathrm{NMS}^{\mathrm{AC}}(m)_{3\mathrm{p}} = \frac{1}{24}m^2 - \frac{2}{9\pi}m^3 + \frac{1}{24}m^4;\ 0 < m < 0.866. \qquad (9)$$

The limitation $m < 0.866$ originates from the fact that STPWM does not make full use of the DC bus voltage dynamic range due to premature phase voltage command saturation [1]. The difference is in m^4 coefficient only as it will be for any other possible modulation strategy by a reasonable zero sequence insertion.

Next, consider a sinusoidal 3P PWM with zero sequence voltage command injection equivalent to space vector PWM (SVPWM) (Fig. 3) [1]

$$v_0 = -[\max(V_A, V_B, V_C) + \min(V_A, V_B, V_C)]/2. \qquad (10)$$

From (5) and (10) (Fig. 3), the offset becomes

$$d(\tau) = \frac{V_a' + V_b'}{2} = \begin{cases} -m\cos(\tau + \pi/6),\ 0 < \tau \le \pi/3; \\ 0,\ \pi/3 < \tau \le \pi/2. \end{cases} \qquad (11)$$

From (2), (7), and (11), SVPWM current NMS becomes

$$\mathrm{NMS}^{\mathrm{AC}}(m)_{3\mathrm{p}} = \frac{1}{24}m^2 - \frac{2}{9\pi}m^3 + \left(\frac{1}{16} - \frac{3\sqrt{3}}{64\pi}\right)m^4. \qquad (12)$$

For inductance dominated RL-load, current THD using (8), (9), and (12) can be calculated similarly to [4] as

$$\mathrm{THD},\% = \frac{\sqrt{2\mathrm{NMS}^{\mathrm{AC}}(m)}}{m}\frac{w}{2f_s}\sqrt{1 + \left(\frac{R}{wL}\right)^2} \times 100, \qquad (13)$$

where f_s is the switching frequency and w is the fundamental angular frequency.

By substituting (8), (9), (12) in (13), one can get simple specific current THD formulas for a 2L SP inverter and a 3P inverter with STPWM and SVPWM.

While 3P NMS formulas (8) and (12) are derived for line-to-line voltage or delta-connected balanced load, THD formula (13) is valid for the star-connected load as well though frequency spectra are different (no triple harmonics for star) [1]. This is due to fundamental delta-star equivalence [2].

For a grid-tied 3P inverter, similar to [4]

$$\mathrm{THD},\% = \frac{V_{\mathrm{dc}}\sqrt{2\mathrm{NMS}^{\mathrm{AC}}(m)}}{2\sqrt{3}ILf_s} \times 100, \qquad (14)$$

where V_{dc} is the DC bus voltage, I is the fundamental current magnitude, and L is the coupling inductance.

Modulation index m is found from a related phasor diagram. For unity power factor, with good accuracy [4]

$$m = m_g = V_g/V_{\mathrm{dc}}, \qquad (15)$$

where V_g is the line-to-line grid voltage magnitude.

3 Current THD for a 3L 3P inverter

For a given three(multi)-level 3P inverter and PWM strategy, current THD calculation challenge is to characterise line-to-line voltage ripple pulses in terms of width $D(\tau)$ and offset $d(\tau)$ similar to (4), (6), and (11) for 2L (Fig. 1) to further calculate by (7) current NMS to be substituted in (13) or (14).

Consider a 3L 3P cascaded H-bridge (CHB) inverter (Fig. 4) with carrier-based level shifted (LS) PWM and voltage references (5). For a 3L 3P inverter, for $0 \le D < 0.5$

$$\mathrm{NMS}_3^{\mathrm{DC}}(D, d) = \mathrm{NMS}_2^{\mathrm{DC}}(2D, 2d)_{3\mathrm{p}}/4, \qquad (16)$$

where $\mathrm{NMS}_2^{\mathrm{DC}}$ is given by (2).

The required phases A and B normalised PWM voltage commands (references) are equal to (5).

From PWM current ripple calculation perspective, there are three different cases on a quarter of a fundamental period $0 < \tau < \pi/2$.

Case 1: Both reference signals are negative (more generally, have the same sign), $0 < V_a < -1; 0 < V_b < -1$ (Fig. 5*a*). The time range of reference voltages for this case is $0 < \tau < \pi/6$. From

© The Institution of Engineering and Technology 2020

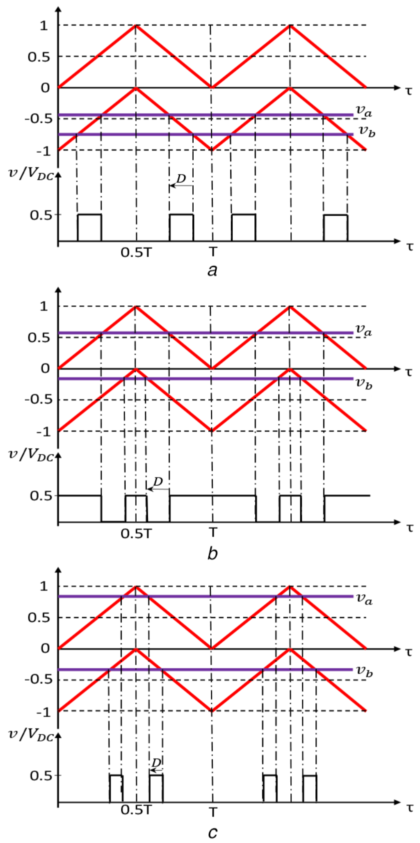

Fig. 5 *Modulation signal and voltage pulses for*
(a) Case 1, ***(b)*** Case 2, ***(c)*** Case 3

Fig. 5*a*, line-to-line voltage normalised pulse width and offset (Fig. 1*b*) are found as

$$\begin{aligned} D(\tau) &= (V_a - V_b)/2 = m\sin\tau; \\ d(\tau) &= 0.5 - (V_a + V_b)/2 = 0.5 - (m/\sqrt{3})\cos\tau\,. \end{aligned} \quad (17)$$

Case 2: The references have opposite signs and their difference absolute value is less than unity ($V_a > 0; V_b < 0; V_a - V_b < 1$) (Fig. 5*b*). For this case, the reference signals range is $\pi/6 < \tau < a\sin(1/(2m)), m > 1/2$.From Fig. 5*b*, for case 2 line-to-line voltage normalised pulse width and offset become

$$\begin{aligned} D(\tau) &= 0.5 - (V_a - V_b)/2 = 0.5 - m\sin\tau; \\ d(\tau) &= 0.5 - [0.5 - (V_a + V_b)/2] = (m/\sqrt{3})\cos\tau\,. \end{aligned} \quad (18)$$

Case 3: The references have opposite signs and the absolute value of their difference is more than unity ($V_a > 0; V_b < 0; V_a - V_b > 1$) (Fig. 5*c*). The range of reference signals for this case is $a\sin(1/(2m)) < \tau < \pi/2, m > 1/2$. From Fig. 5*c*, for case 2

$$\begin{aligned} D(\tau) &= (V_a - V_b)/2 - 0.5 = m\sin\tau - 0.5; \\ d(\tau) &= 0.5 - [0.5 - (V_a + V_b)/2] = (m/\sqrt{3})\cos\tau\,. \end{aligned} \quad (19)$$

For an STPWM, the relationship between reference sine signal magnitude A and modulation index $0 < m < 0.866$ is $A = 2m/\sqrt{3}$ (over-modulation not considered).

Current ripple NMS calculations for AC PWM are different for $0 < m < 0.5$ and $0.5 < m < 0.866$.

For $0 < m < 0.5$, DC PWM NMS is found from (16) for $D < 0.5$ and AC PWM NMS integral (7) is split into two for $0 < \tau < \pi/6$ (case 1) and $\pi/6 < \tau < \pi/2$ (case 2)

$$\mathrm{NMS}^{\mathrm{AC}}(m)_{3\mathrm{p}} = \frac{6m^4\pi - (16 + 4\sqrt{3})m^3 + (4\pi - 3\sqrt{3})m^2}{36\,\pi}. \quad (20)$$

For $0.5 < m < 0.866$, DC PWM NMS is found from (16) for $D < 0.5$ and AC PWM NMS integral (7) is split into three according to cases 1–3 (17)–(19)

$$\begin{aligned} \mathrm{NMS}^{\mathrm{AC}}(m)_{3\mathrm{p}} = \frac{1}{36\pi}\Big[&6m^4\pi - (16 + 4\sqrt{3})m^3 \\ &+ (22\pi - 3\sqrt{3})m^2 - (22m + 32m^3)\sqrt{1 - \frac{1}{4m^2}} \\ &+ 3\pi + 6(m^2 + 2m^4)\operatorname{acsc}(2m) \\ &- 6(1 + 7m^2 + 2m^4)\operatorname{asin}\left(\frac{1}{2m}\right)\Big]. \end{aligned} \quad (21)$$

Next, consider SVPWM with voltage references of (5) modified by zero sequences (10)

$$\begin{aligned} V'_a &= (2/\sqrt{3})m\sin(\tau - \pi/6) + v_0; \\ V'_b &= (2/\sqrt{3})m\sin(\tau - 5\pi/6) + v_0\,. \end{aligned} \quad (22)$$

While the pulse width $D(\tau)$ is the same as for LS STPWM in (16)–(18), the offset $d(\tau)$ is different.

Case 1: In the range of $0 < \tau \le \pi/6$

$$d(\tau) = 0.5 - \left(1 + \frac{V'_a + V'_b}{2}\right) = -0.5 + m\cos(\tau + \pi/6)\,. \quad (23)$$

Cases 2 and 3: In the range of $\pi/6 < \tau < \pi/2$

$$\begin{aligned} d(\tau) &= -m\cos(\tau + \pi/6), \ \pi/6 < \tau \le \pi/3; \\ d(\tau) &= 0, \ \pi/3 < \tau \le \pi/2. \end{aligned} \quad (24)$$

For SVPWM with $0 < m < 0.5$, DC PWM NMS is found from (16) for $D < 0.5$ and AC PWM NMS by (7) becomes

$$\mathrm{NMS}^{\mathrm{AC}}(m) = \frac{(36\pi - 27\sqrt{3})m^4 + (128 - 120\sqrt{3})m^3 - (18\sqrt{3} + 18\pi)m^2}{144\pi}. \quad (25)$$

For SVPWM with $0.5 < m < 1$

$$\begin{aligned} \mathrm{NMS}^{\mathrm{AC}}(m) = \frac{1}{2\pi}\Bigg\{&\left[\frac{\pi}{2} - \frac{3\sqrt{3}}{8}\right]m^4 \\ &+ \left[\frac{16}{9} - \frac{5\sqrt{3}}{3} - \frac{16}{9}\sqrt{1 - \frac{1}{4m^2}}\right]m^3 \\ &+ \left[\frac{5\pi}{4} - \frac{\sqrt{3}}{4} - 2\operatorname{asin}\left(\frac{1}{2m}\right)\right]m^2 \\ &- 11m\sqrt{1 - \frac{1}{4m^2}}/9 - \frac{\operatorname{asin}(1/2m)}{3} + \frac{\pi}{6}\Bigg\}. \end{aligned} \quad (26)$$

SVPWM is better than LS STPWM because zero sequence introduction makes line-to-line voltage pulses distribution more even. This is demonstrated by normalised current ripple root mean square (RMS; $\sqrt{\mathrm{NMS}^{\mathrm{AC}}(m)}$) graphs (Fig. 6). Current ripple RMS is practically proportional to grid-tied current THD for $0.6 < m < 0.9$ by formula (14).

Fig. 7 compares normalised current THD

$$\mathrm{THD}_n, \% = \frac{\sqrt{2\mathrm{NMS}^{\mathrm{AC}}(m)}}{m} \times 100. \quad (27)$$

for different PWM strategies and level counts.

© The Institution of Engineering and Technology 2020

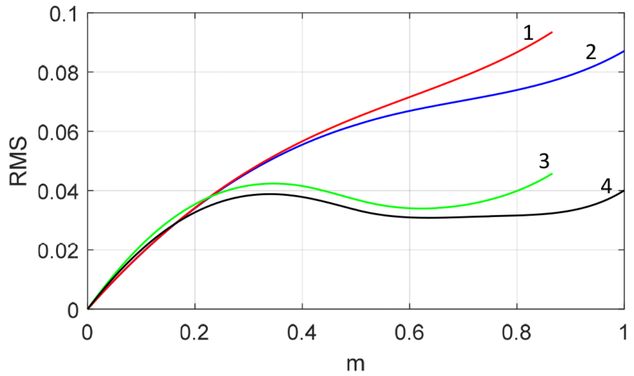

Fig. 6 *Normalised current RMS for: 1 – 2L 3P STPWM; 2 – 2L 3P SVPWM; 3 – 3L 3P LS STPWM; 4 – 3L 3P SVPWM*

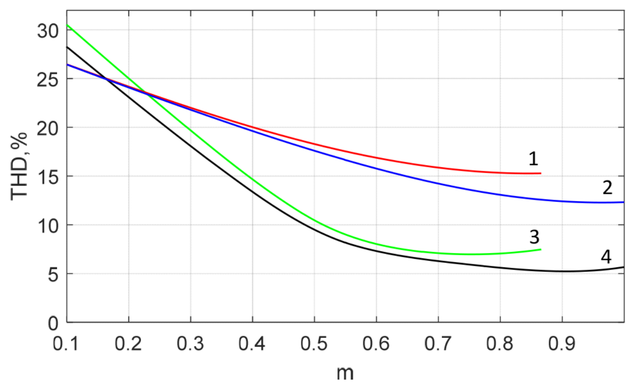

Fig. 7 *Normalised current THD for: 1 – 2L 3P STPWM; 2 – 2L 3P SVPWM; 3 – 3L 3P LS STPWM; 4 – 3L 3P SVPWM*

4 Verification by simulation

Theoretical results were verified by MATLAB/Simulink simulations for a 3P 3L neutral point clamped (T-type) grid-tied inverter with LS SVPWM and the following parameter values: $V_{\mathrm{dc}} = 400\,V$; $V_{\mathrm{g}} = 311\,\mathrm{V}$; $f = 50\,\mathrm{Hz}$; $f_{\mathrm{s}} = 2.5\,\mathrm{kHz}$; $L = 10\,\mathrm{mH}$; $R = 1\,\Omega$; $I = 10\,\mathrm{A}$; and $m = 0.832$ (unity power factor). For very large DC bus capacitances (no neutral point voltage ripple) current THD by (14) equals 2.08%, from simulation – 2.12%. For $C = 0.2\,\mathrm{mF}$, neutral point peak-to-peak voltage ripple amounts to 5% and simulated current THD increases to 2.13%; for $C = 0.1$ and 0.05 mF, voltage ripple becomes 10 and 20% and current THD – 2.18 and 2.45%, respectively.

Grid and inverter line-to-line AB voltages are shown in Fig. 8*a*, phase A grid voltage and current – in Fig. 8*b*.

5 Conclusion

This study first demonstrated how current THD of a 2L 3P inverter can be assessed using harmonic distortion or loss, factor (current ripple NMS) time domain analysis [1, 3]. Next, the time domain averaging approach was applied to a 3L CHB inverter with one H-bridge per phase and two modulation strategies – LS STPWM and SVPWM.

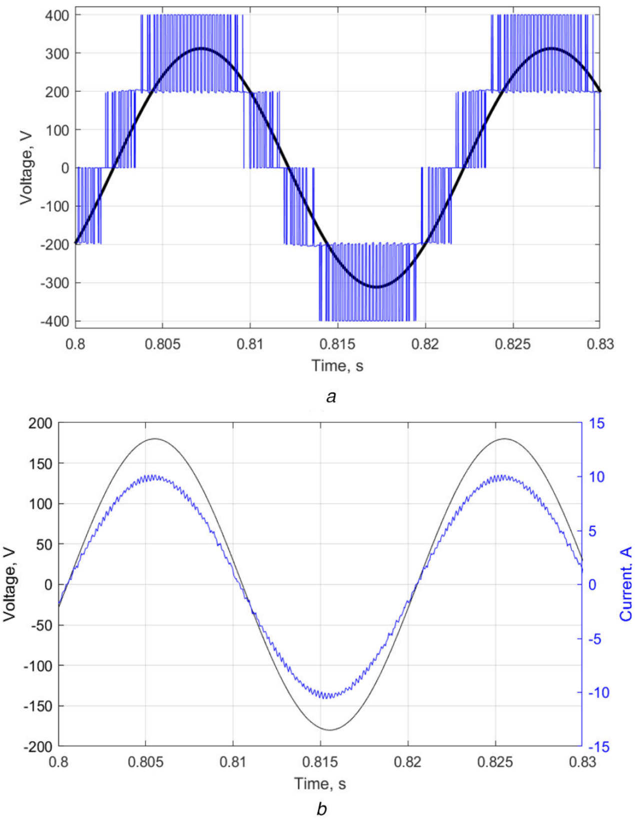

Fig. 8 *3P 3L grid-tied NPC inverter with LS SVPWM*
(a) Grid and inverter line-to-line AB voltages, ***(b)*** Phase A grid voltage and current

As verified by simulations, the asymptotic current THD formulas are quite accurate for PWM-to-fundamental frequency ratios >25–30. Theoretical THD values are always lower because of (a) small resistance impact on current ripple; (b) asymptotic assumption; (c) real life close-loop rejection of disturbances. Thus, the asymptotic formulas can be considered as lower bound estimates.

For neutral point clamped (T-type) and flying capacitor 3L 3P inverters, current THD formulas accuracy may deteriorate due to neutral point/flying capacitor voltage ripples caused low-frequency sub-harmonics.

6 References

[1] Holmes, D.G., Lipo, T.A.: '*Pulse width modulation for power converters*' (IEEE Press, Piscataway, NJ, 2003)

[2] Ruderman, A., Reznikov, B., Busquets-Monge, S.: 'Asymptotic time domain evaluation of a multilevel multiphase PWM converter voltage quality', *IEEE Trans. Ind. Electron.*, 2013, **60**, (5), pp. 1999–2009

[3] van der Broeck, H.W., Skudelny, H.-C., Stanke, G.W.: 'Analysis and realization of a pulsewidth modulator based on state space vectors', *IEEE Trans. Ind. Appl.*, 1988, **24**, (1), pp. 142–150

[4] Reznikov, B., Srndovic, M., Familiant, Y., *et al.*: 'Simple time averaging current quality evaluation of a single-phase multilevel PWM inverter', *IEEE Trans. Ind. Electron.*, 2016, **24**, (1), pp. 142–150

© The Institution of Engineering and Technology 2020