

**MOVING OBJECT DETECTION WITH MEMRISTIVE CROSSBAR  
ARRAYS**

**Sultan Duisenbay, Bachelor of Engineering**

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**School of Engineering  
Department of Electrical and Electronic Engineering  
Nazarbayev University**

53 Kabanbay batyr Avenue,  
Astana, Kazakhstan, 010000

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# Abstract

This thesis is dedicated to the hardware implementation of a novel moving object detection algorithm. Proposed circuit includes several stages, each of which implements a particular step of the algorithm. Four higher bit planes are extracted from a grayscale image and stored in memristive crossbar arrays, and the respective bit planes are compared via memristive threshold logic gates in XOR configuration. In the next stage, compared bit planes are combined by weighted summation, with a highest weight assigned to MSB plane and smaller weights for less significant bit planes. After summation stage, obtained grayscale image is thresholded to obtain binary image. The last stage is implemented via memristive content-addressable memory array, which serves two purposes. It is used as a long-term memory in comparison to crossbar arrays, which serve as a short-term memory of proposed circuit. Content-addressable memory is updated based on the row-by-row difference between first and second pair of frames processed by previous stages. It also allows for analysis of object movement direction and velocity by observing the row capacitors' discharge. Simulations show that accuracy of proposed circuit operation is increased with the larger array size. Delay analysis of the circuit is carried out, power and area calculations show that proposed circuit is a viable candidate as a co-processing operator for existing image sensors.

# Acknowledgments

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# Chapter 1 – Introduction

This thesis focuses on hardware implementation of the moving object detection algorithm presented in "Moving object detection using bit-plane slicing" thesis by Nazgul Dastanova. The key objectives of this thesis include step-by-step hardware simulations by proper design and choice of circuit elements and stages. These stages comprise:

1. Storage of binary images in short-term memory
2. Comparison of binary images
3. Combination of binary images to obtain grayscale image
4. Thesholding of the grayscale image
5. Storage of binary images in longer-term memory

Circuit simulations are implemented mostly based on memristive elements, which have found many applications in digital (memory and logic) [1], [2], [3], [4], [5] and analog (oscillators, amplifiers, and comparators) circuits [6], [7], [8]. In this thesis, memristors are utilized in digital manner, with the binary state being memorized in them.

The motivation behind this work lies in the internet-of-things (IOT), which has started encompassing almost every aspect of human life. Increased attention is paid to smart technologies connected over network to allow automation and intelligence. Particularly within IOT, we want to focus on video-over-IOT using existing image sensors and transmission devices. Bearing this in mind, proposed circuit could be potentially implemented in security, law enforcement and military applications.

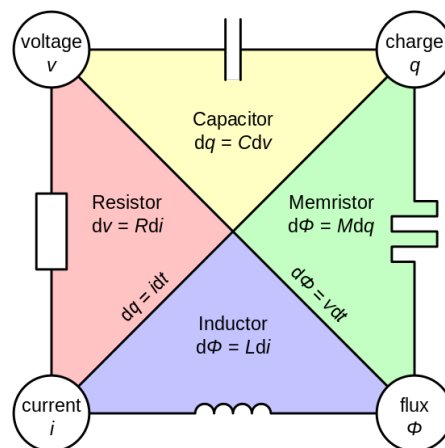
# Chapter 2 – Literature review

## 2.1 Memristor

Leon Chua, nonlinear circuit theorist, realized the symmetric connection in three basic passive circuit elements (capacitor, inductor, resistor) in 1971 [9]. By analyzing the fact that there are four fundamental variables from a circuit's point of view (i.e. flux linkage  $\phi$ , charge  $q$ , voltage  $v$ , current  $i$ ), he suggested the existence of a fourth circuit element. Four fundamental variables should have been connected with each other via basic circuit elements: inductor connecting the flux linkage  $\phi$  with the current  $i$ , capacitor connecting the voltage  $v$  with the charge  $q$ , and resistor connecting the voltage  $v$  with the current  $i$  [10]. Based on the missing relationship between the flux linkage  $\phi$  and charge  $q$ , Chua argued about the existence of fourth circuit element connecting those fundamental variables by:

$$d\phi = M dq \quad (2.1)$$

where  $M$  represents memristance, parameter of the theoretical circuit element.



*Figure 2.1: Circuit elements connecting four fundamental circuit variables*

This theorized circuit element was named as a memory resistor, or memristor in short, since it could remember previous state. Memristor shares the same characteristics as potentiometer in changing the active resistance; however, it is a two-terminal device, where the effective resistance is altered by applying specific voltage across device terminals [11]. The memristor has been physically implemented only after more than 40 years in 2008 by HP Labs [12].

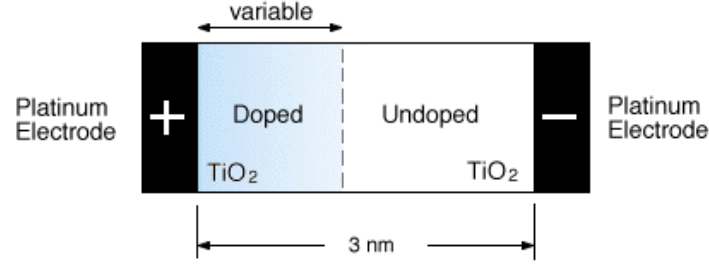
Theory behind the memristor prototype produced by HP Labs is discussed in [13]. Figure 2.2 shows the HP prototype memristor model. Prototype is implemented by putting a thin two-layer titanium dioxide ( $TiO_2$ ) film between platinum contacts. By introducing oxygen vacancies into one film, semiconductor property is enhanced, while the undoped region remains as an insulator [14]. The resistance is changed by modulating the width of doped region based on charge passing through device. The doped region boundary is moved in the direction of passing current [13]. The total resistance of element  $R_{MEMRISTOR}$  is calculated by:

$$R_{MEMRISTOR}(x) = R_{ON}x + R_{OFF}(1 - x), \quad (2.2)$$

where  $x$  is the ratio of doped region width to total width of memristor,  $R_{ON}$  and  $R_{OFF}$  are resistances for fully undoped region (insulator) and fully doped (semiconductor) regions respectively.

Many factors, including resistances of doped area, current, and other factors, have an effect on boundary movement speed, which is given by:

$$\frac{dx}{dt} = ki(t)f(x) \quad (2.3)$$



*Figure 2.2: HP prototype memristor model*

$$k = \frac{\mu_v R_{ON}}{D^2} \quad (2.4)$$

where  $D$  is total memristor width, and  $\mu_v$  is dopant mobility.

HP memristor is susceptible to ionic transport nonlinearities which are generated by huge electric fields [12]. These ionic transport nonlinearities are manifested at the memristor edges, where boundary movement speed drops to zero [13]. This change in boundary movement speed is called nonlinear dopant drift and is modeled by introduction of window function given by  $f(x)$  in 2.3. Window function, according to [13], is given by:

$$f(x) = 1 - (2x - 1)^{2p} \quad (2.5)$$

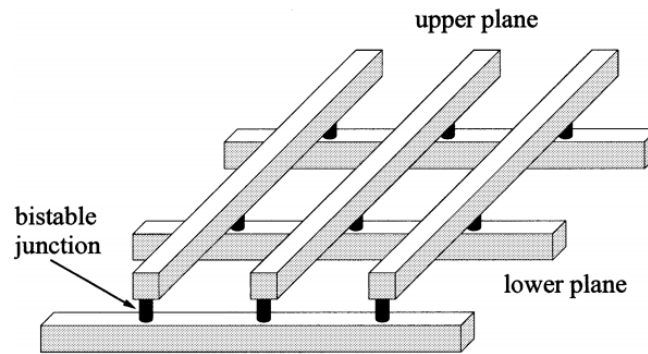
where  $p$  is a positive integer.

This model is used to simulate memristors used in proposed circuit, and the SPICE code for the model is presented in appendix.

## 2.2 Crossbar array

Crossbar array structure has been implemented since 1970s for both memory and logic applications. Simple crossbar array structure consists of a mesh of parallel

and perpendicular wires with a switch at the junction [15]. The switch state can be either open or closed. Memory is stored in the form of state switch, and is extracted by applying a defined voltage on a wire. Logic implementation is also done by presetting the switch state and applying appropriate voltage level [16]. Simple crossbar structure is presented in Fig. 2.3.

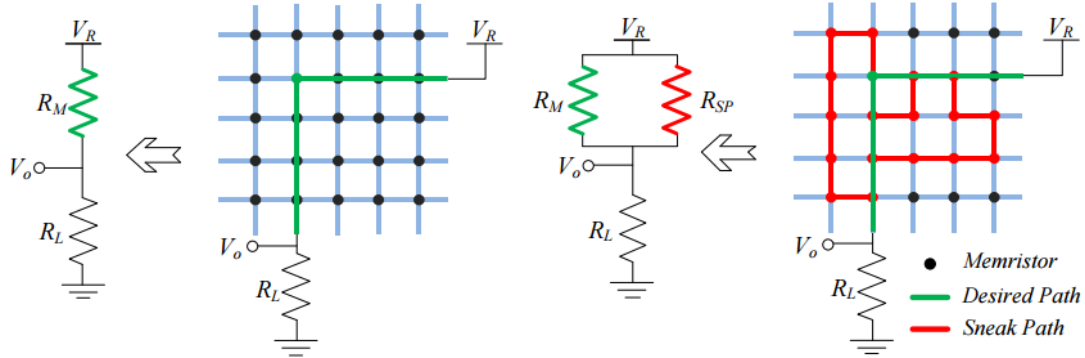


*Figure 2.3: Simple crossbar structure*

Crossbar technologies have been inferior to conventional CMOS memory and logic design in terms of power-efficiency, area and performance [3]. These disadvantages arose primarily due to the inherent characteristics of device implemented as a switch. Application of memristors as switch elements for crossbar architecture has addressed these issues and vast research has been accomplished in the area of memristive crossbar arrays. As CMOS technology is reaching a stagnation point in Moore's law, memristor crossbar memory arrays have been considered as a successor to conventional memory architectures due to high density [17].

Fundamental problem lying on the implementation of such a passive crossbar array (network of wires with a memristor switch) lies in the occurrence of sneak paths [18]. During the read cycle, current starts passing through the desired and undesired memristors. This could lead to potential errors during the

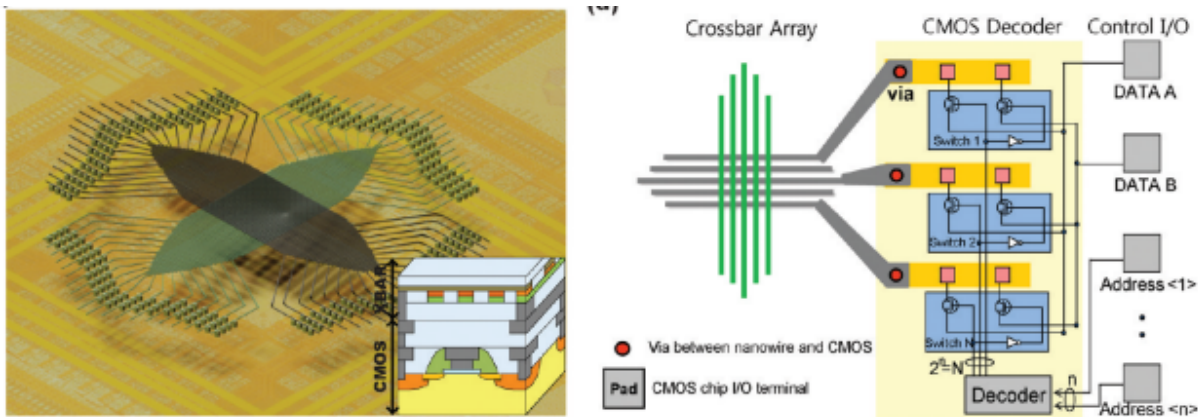
read stage and deteriorate the system accuracy [19]. Furthermore, sneak path increase energy consumption of the overall circuit as the array size increases [20]. For this reason, successful implementation of a memristive crossbar array implementation lies in addressing the issue of sneak paths.



**Figure 2.4: Sneak path representation during the read phase**

Manifold architectures have been proposed to deal with sneak paths and design high-density, accurate and power-efficient crossbar structures. For instance, in [21], hybrid crossbar/CMOS system is presented for memory applications. In this structure, memristive crossbar array is integrated on top of CMOS system without implementing transistors or diodes to avoid sneak paths. Instead, hybrid structure utilizes inherent physical characteristics of the memristor itself. Authors in [21] were able to store the 1600 pixel binary and multilevel images into such an array. Figure 2.5 illustrates the architecture proposed in [21]. Another promising architecture is illustrated in [22]. The architecture combines high-density arrays with transistor isolation for sneak path prevention. Transistor isolate smaller crossbar tiles withing larger memristive crossbar array [22]. Pulse generator sends data to each row in tiles while grounding the others. Row decoders turn on a single row of tile to be accessed during read or write opera-

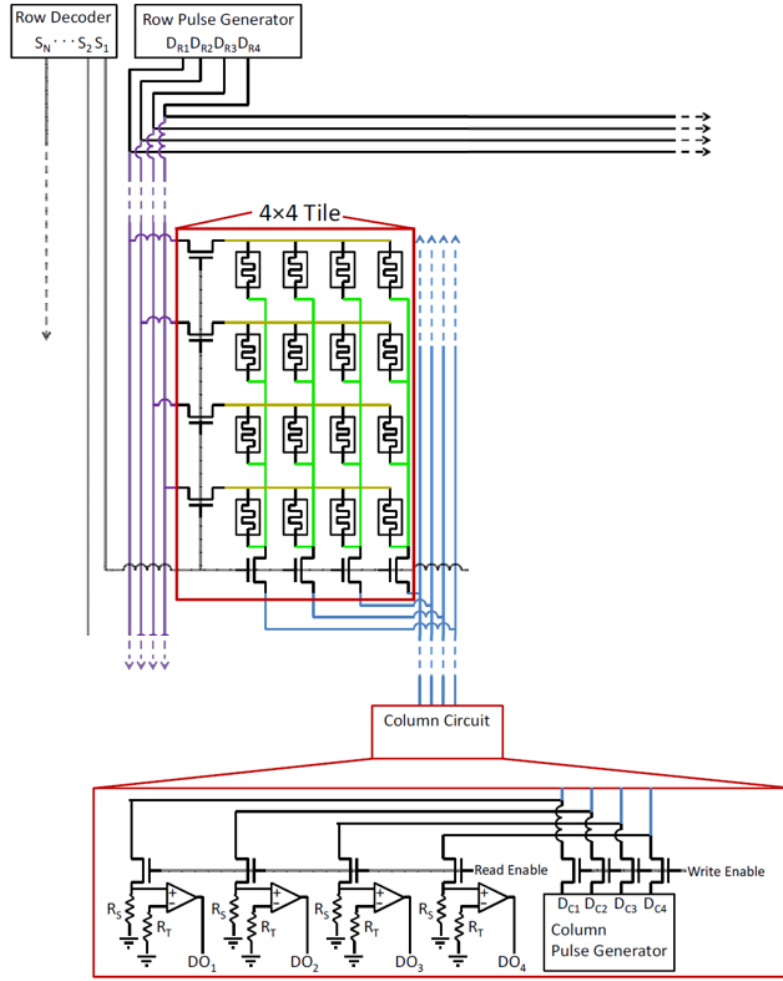
tions. This design allows for constraining the sneak paths in smaller tiles rather than in the whole crossbar array. Proposed transistor isolated architecture is illustrated in Fig. 2.6.



*Figure 2.5: Hybrid memristive crossbar/CMOS system design*

## 2.3 Threshold logic

Threshold logic has found many applications in computing, including microprocessing and bio-inspired processing [23]. Threshold logic gates (TLG) have been considered as a successor to conventional logic gates. The ability to accomplish complex function by using intrinsic properties of threshold logic gates allows for fewer gates and levels compared to standard logic design. Threshold logic design has attracted attention due to potential to implement multiple addition, multiplication, division and sorting [24]. Furthermore, TLG has found applications in modeling neural networks and brain-inspired processes, including learning, adaptive and pattern-recognition systems [25].



**Figure 2.6: Hybrid tiled memristive crossbar design**

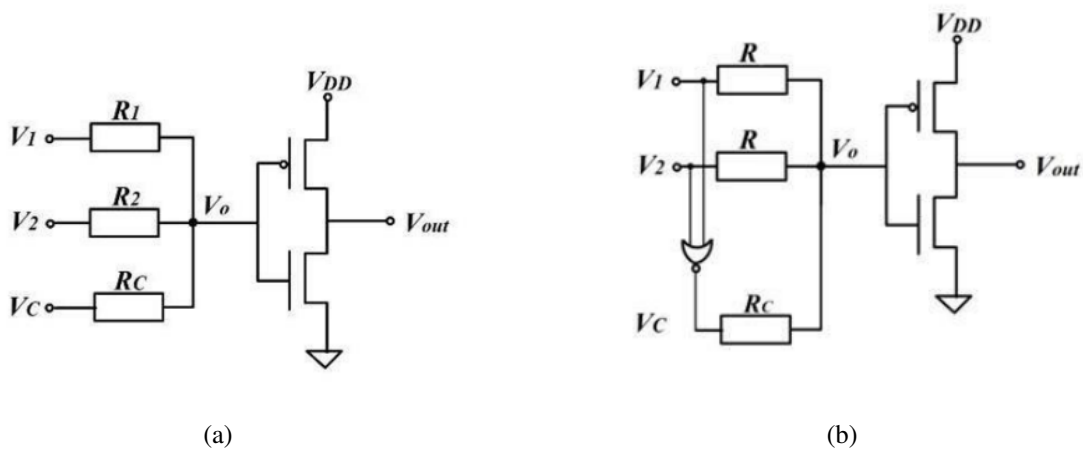
In general, transfer function for a linear threshold logic gate is given by:

$$f(x_1, \dots, x_n) = \begin{cases} 1, & \sum_{i=1}^n w_i x_i \geq T \\ 0, & \text{otherwise} \end{cases} \quad (2.6)$$

where  $x_i$  is the input variable,  $w_i$  is the weight corresponding to input  $i$  and  $T$  is the threshold given by an integer number.

Threshold logic gates using memristors as input weights are discussed in [24], [25], [23]. The most promising design is discussed in [26], which

proposes hybrid memristor/CMOS threshold logic gate. In mentioned configuration, memristors are used as reconfigurable weights, while CMOS inverter is implemented as a threshold logic device. By utilizing the resistive switching ability of memristive devices, weights are assigned and the threshold logic gate configuration may be changed to *NAND*, *NOR* or *XOR* configuration. Figure 2.7 illustrates the threshold logic gate proposed in [26].



**Figure 2.7: Hybrid memristive/CMOS linear threshold logic gate in (a) *NAND* & *NOR* configuration, (b) *XOR* configuration**

*NAND* and *NOR* configuration is achieved by setting all memristors (two input and one control)  $R_1$ ,  $R_2$ , and  $R_C$  to high resistance state. By setting control voltage  $V_C$  higher than  $0.5V$ , *NOR* functionality is achieved, and *NAND* configuration is achieved by setting  $V_C$  lower than  $0.5V$  [26]. *XOR* functionality is achieved by setting  $V_C$  equal to *NOR* output of two input voltages and setting control memristor  $R_C$  according to:

$$R_C = \begin{cases} R_L, & \text{if } V_C = 1 \\ R_H, & \text{if } V_C = 0 \end{cases} \quad (2.7)$$

where  $R_L$  and  $R_H$  represent low and high resistances respectively.

## 2.4 Content-addressable memory

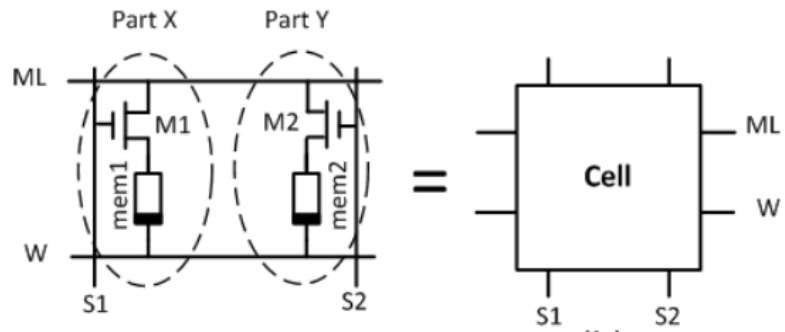
Content-addressable memory (CAM) is a memory type where the input data is compared to the stored in memory [27]. CAM has a significant advantage in speed, since the comparison is achieved in a single clock cycle. As a result, content-addressable memories have been used in Huffman coding [28], Lempel-Ziv compression [29], and image coding [30]. Although showing fast performance, CAM circuits have a very high power consumption, which limits its applications. Additional disadvantage of using CAMs comes from an increased silicon area [31]. Typical operation of CAM is illustrated in Fig. 2.8. Input to CAM array is provided by searchlines, which is compared to the stored pattern. The output of CAM is provided by matchlines, which is dependent on the similarity between input and stored patterns.



Figure 2.8: Basic content-addressable diagram depicting search and match lines

In order to address the issue of high power consumption and low area scalability, memristors have been proposed as an efficient alternative for transistors in CAMs [32], [33], [34]. Promising design of memristive content-addressable memory cell is proposed in [33], which utilizes two transistors and two mem-

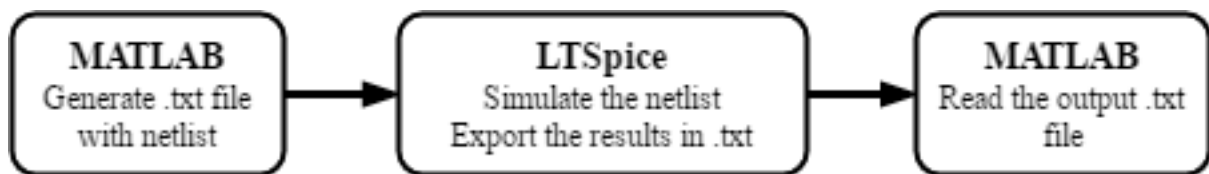
ristors ( $2T - 2M$  configuration) for a single cell. CAM cell proposed in [33] is depicted in Fig. 2.9.



**Figure 2.9: Memristive CAM cell in  $2T-2M$  topology**

## Chapter 3 – Methodology

Extensive research concerning the algorithm implementation is more thoroughly discussed in "Moving Object Detection Using Bit-Plane Slicing" thesis presented by Nazgul Dastanova. Hardware implementation of the algorithm is presented in this thesis. Circuit simulation is achieved via integrating MATLAB and LTSpice [35] as shown in Fig.3.1. Circuit netlist is generated in MATLAB by defining and embedding the necessary elements, models and options. The obtained netlist is then simulated in LTSpice with the exported output. Output from simulation is extracted via using MATLAB for reading.



*Figure 3.1: Block diagram of circuit simulation stages*

Hardware block diagram of the proposed circuit is illustrated in Fig. 3.2. Higher order binary bit planes are stored in memristive crossbar arrays. Twelve crossbar arrays are generated to store four higher order bit planes of three consecutive frames in total. Each arrays' columns are integrated with comparator circuit to read the stored bit. Output from comparator circuits from frame #1 and frame #2 are compared using the first group of threshold logic gates, while frames #2 and #3 are compared via another group of threshold logic gates. Grayscale image of moving object is obtained by applying weighted addition of bit planes. Outputs from TLGs are fed to summation circuit, with each compared bit plane having a defined weight. Object's binary image is obtained by thresholding stage. Content-addressable memory is used at the

output stage to store the object detected from the previous pair of consecutive frames and compare it with the one detected from the current pair of consecutive frames.

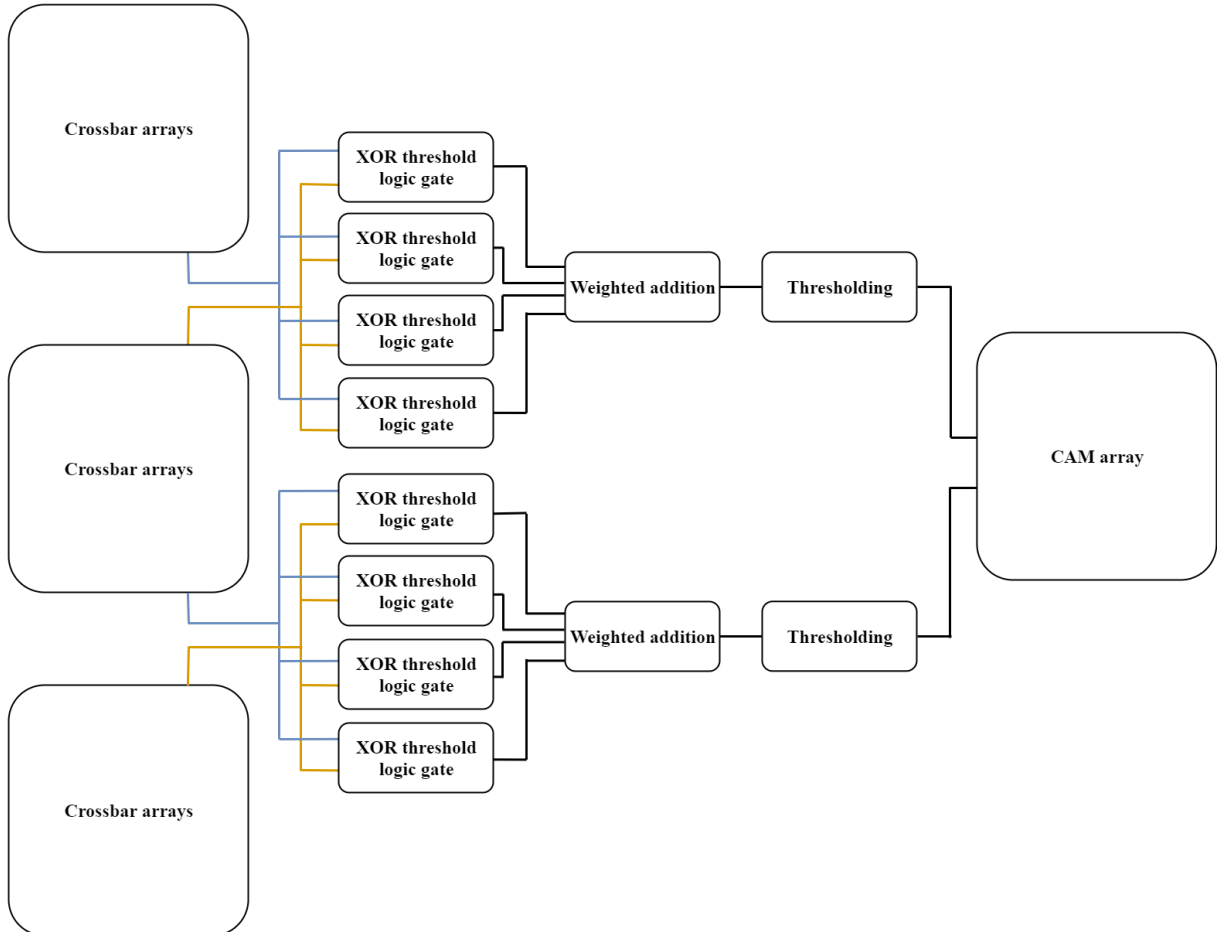
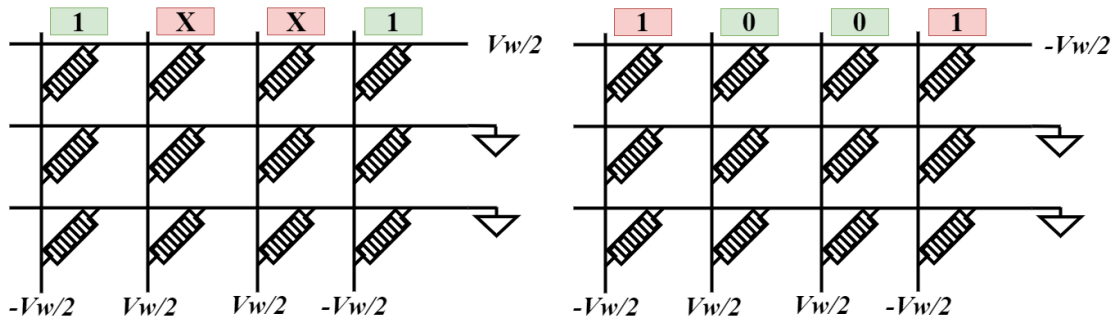


Figure 3.2: Hardware block diagram of the proposed circuit

### 3.1 Memristive crossbar arrays

Bit planes in memristive crossbar arrays are stored in two row-by-row successive write cycles, which are illustrated in Fig. 3.3. Memristors are set applying positive or negative write voltage, which is greater than memristor's threshold voltage ( $V_w > V_{thresh}$ ). During the first cycle, bits of value "1" are written into memristors in the form of low resistance while "0" valued bits remain idle. This

is achieved by applying positive write voltage across memristor terminals,  $V_w/2$  as the row voltage and  $-V_w/2$  as the column voltage. "0" bits are remained idle by applying  $V_w/2$  both as row and column voltage. During the second cycle, bits of value "0" are written in the form of high resistance while already stored "1" bits remain idle.  $-V_w/2$  is applied as the row voltage and  $V_w/2$  as the column voltage resulting in negative write voltage applied across memristor terminals.



**Figure 3.3: Memristor crossbar array write cycle**

Stored bits are read by applying read voltage, which is smaller than threshold voltage in order to avoid resetting the switches ( $V_r < V_{thresh}$ ). Bits are extracted via comparator circuits embedded into crossbar's columns. Comparator circuit comprises load resistor and op-amp along with reference voltage. Depending on memristor's resistance, either "0" or "1" is obtained at the output of comparator circuit in the form of voltage waveform. Potential issue during the read cycle from the crossbar array lies in sneak-path problem. For this reason, conventional row-wise reading becomes error-prone due to decrease of effective resistance by forming a network of parallel memristor. In order to deal with the sneak path problem, memristors are read element-wise after applying read voltage to each row. This is accomplished by introducing an isolating switch between crossbar array and a comparator stage. Memristor crossbar array with the comparator stage is represented in Fig. 3.4

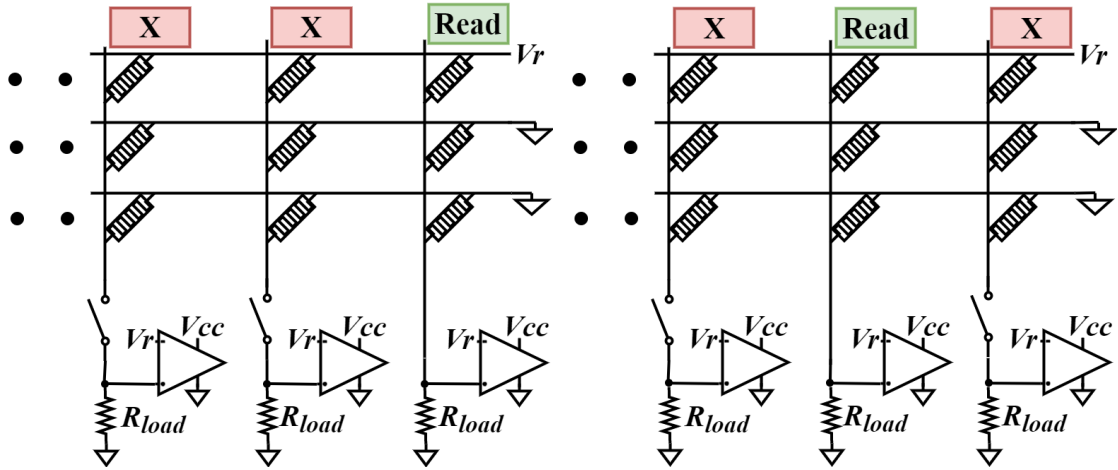


Figure 3.4: Memristor crossbar array read cycle

Comparator stage outputs the stored bits in the form of voltage waveforms. Figure 3.5 illustrates the stored bit sequence  $V_1$  ("1101"), with each bit duration of  $5\mu\text{s}$  and 25% duty cycle.

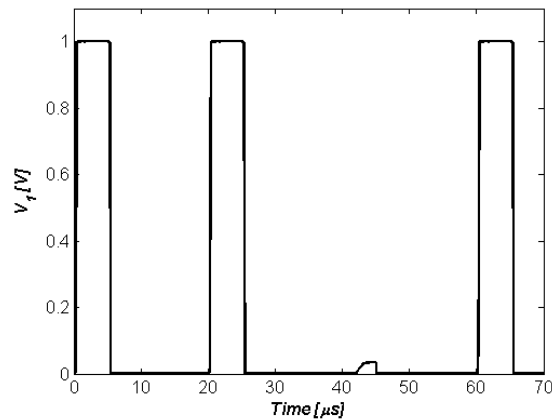


Figure 3.5: Bit sequence "1101" stored and extracted from memristive crossbar array

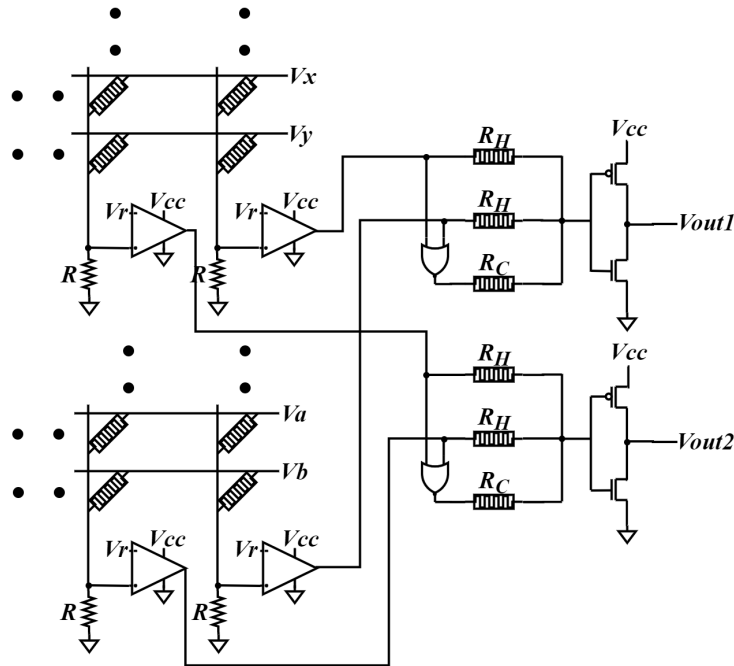
## 3.2 Threshold logic gates

The next stage comprises memristive threshold logic gate presented in [26]. Bits stored in crossbar arrays are accepted as inputs to threshold logic gate. For instance, crossbar array storing the MSB plane of frame 1 and the one storing

MSB plane of frame 2 are connected to a single threshold logic gate. Logic gate is setup to XOR configuration, which requires the control voltage  $V_c$  to correspond to NOR output of two input voltages. Control resistance is also varied according to control voltage, which is represented in Table 4.1, where  $R_L$  and  $R_H$  correspond to low and high resistances respectively. The output from TLG corresponds to the compared bit value and thus compared bit planes are formed. Crossbar arrays with the integrated TLG are illustrated in Fig. 3.6.

**Table 3.1: Truth table for TLG operation in XOR configuration**

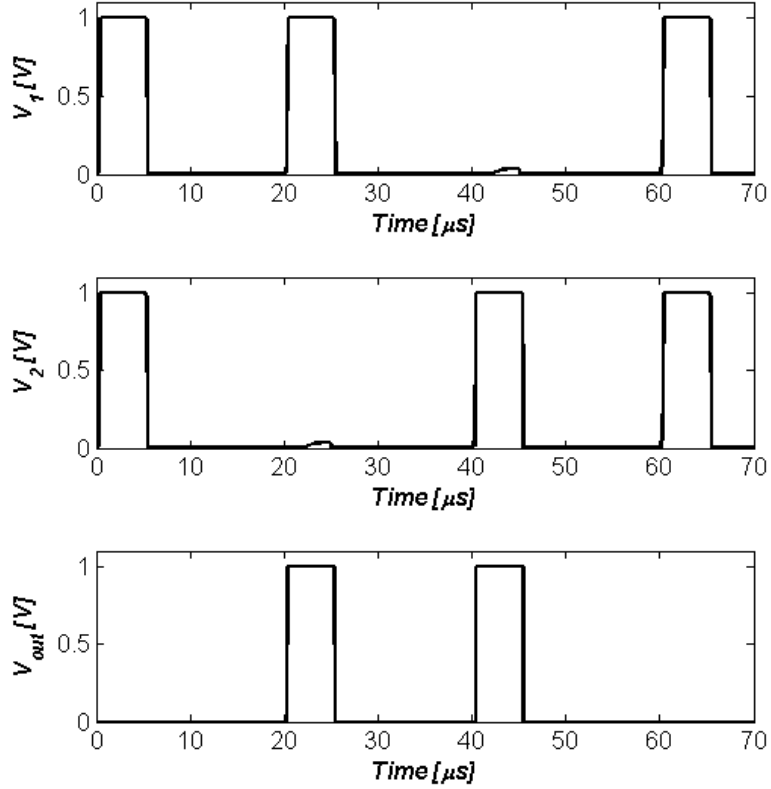
$V_1$	$V_2$	$V_c$	$R_c$	$V_{out}$
0	0	1	$R_L$	0
0	1	0	$R_H$	1
1	0	0	$R_H$	1
1	1	0	$R_H$	0



**Figure 3.6: Memristive crossbar arrays integrated with memristive threshold logic gates**

The operation of the memristive threshold logic gate in XOR configuration

is represented in Fig. 3.7. Two input bit sequences  $V_1$  ("1101") and  $V_2$  ("1011") are compared via TLG with the corresponding XOR output. Bit voltage pulses are of  $5\mu s$  duration and 25% duty cycle.



*Figure 3.7: Timing diagram showing the operation of TLG in XOR configuration*

### 3.3 Weighted summation and tresholding circuit

After comparison, bit planes are combined again to obtain a grayscale image. The combination is performed via weighted addition of obtained bit planes, which is implemented in the form of summing operational amplifier in proposed circuit. Weights in the summing operational amplifier are adjusted according to:

$$V_{out} = - \left[ \frac{R_F}{R_{IN1}} V_1 + \frac{R_F}{R_{IN2}} V_2 + \frac{R_F}{R_{IN3}} V_3 + \frac{R_F}{R_{IN4}} V_4 \right], \quad (3.1)$$

where  $V_{out}$  is the output voltage,  $R_F$  is the feedback resistance,  $R_{IN1}$ ,  $R_{IN2}$ ,  $R_{IN3}$ ,  $R_{IN4}$  are input resistances, and  $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$  are input voltages respectively.

MSB plane is assigned a weight of 0.5, 6th bit plane - 0.25, 5th bit plane - 0.125, and 4th bit plane - 0.0625. This is achieved by setting  $R_{IN1}$  equal to  $2R_F$ ,  $R_{IN2}$  equal to  $4R_F$ ,  $R_{IN3}$  equal to  $8R_F$ , and  $R_{IN4}$  equal to  $16R_F$ . Weights are assigned with the help of proper memristor ratioing. Since no change in resistance is required in this stage, memristors are configured to have threshold voltage higher than the pulse amplitude  $V_{thresh} > 1V$ . Figure 3.8 illustrates the weighted summing stage circuit setup. Voltage waveforms obtained from weighted summation stage are illustrated in Fig. 3.9.

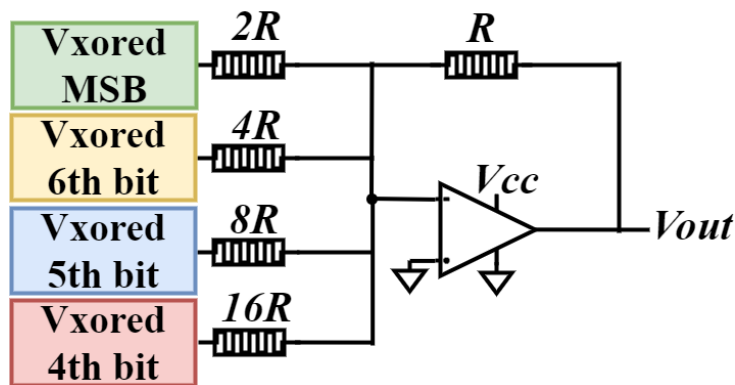


Figure 3.8: Weighted summing circuit stage

The next step according to algorithm includes thresholding of the obtained grayscale image. This is done via comparator circuit embedded after weighted summation stage. Depending on the value of grayscale pixel, either "0" or "1" is produced at the output and final binary image is formed. Thresholding circuit stage is represented in Fig. 3.10. The operation of the thresholding circuit is shown in Fig. 3.11, with the reference voltage  $V_{REF}$  set to  $0.25V$ .

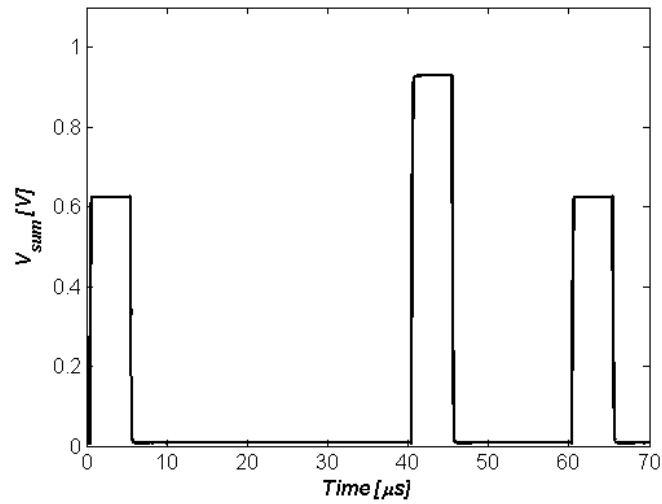


Figure 3.9: Voltage waveforms generated by weighted summing stage

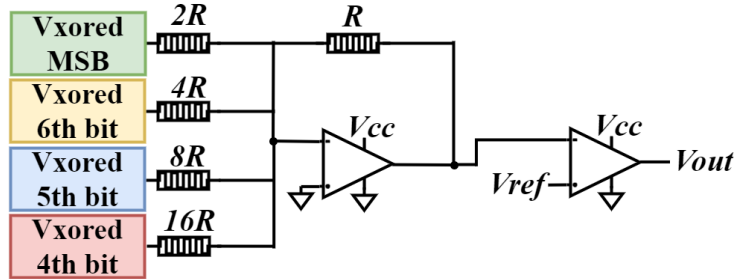
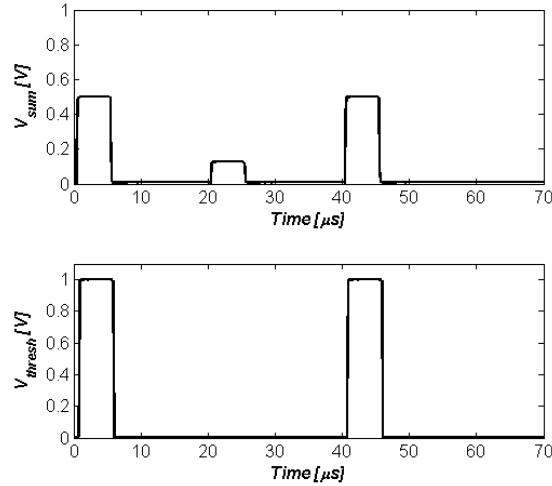


Figure 3.10: Op amp comparator embedded into weighted summing circuit stage

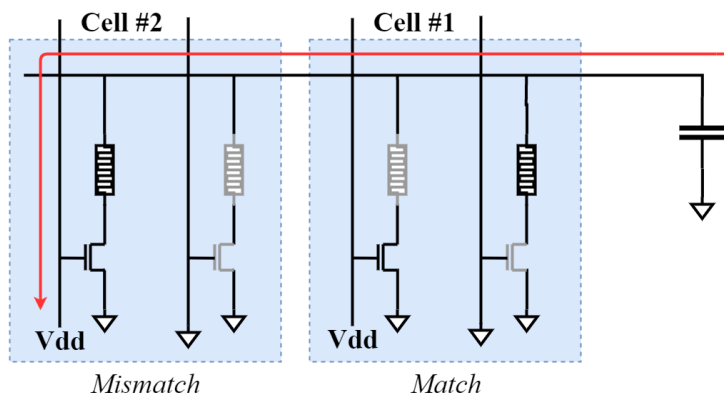
### 3.4 Content-addressable memory

The final stage of proposed circuit consists of memristive content-addressable memory (CAM). Memristive CAM pursuits several purposes in circuit. By observing the difference in discharge operation, it is possible to determine horizontal, vertical or diagonal direction of object movement. In addition to this, CAM array allows for less memory utilization by storing row bits, which are different and leaving the same bits idle. Memristive CAM array or ReCAM (resistive CAM) is based on 2T-2M topology, which utilizes a pair of transistors and memristors. Binary data is stored in the CAM array in the form of high or low resistance. The charge stored in the row capacitor is leaked through a



**Figure 3.11: Timing graph showing the weighted summing generated voltage being thresholded**

mismatched cell, where transistor is ON and memristor has a low resistance opening a path to ground. Binary data is stored in complementary mode since high resistance mismatched cell will not leak charge to ground, while the complementary memristive device with low resistance will. Memristive CAM array circuit is presented in Fig. 3.12. Memristive devices depicted in gray have a "1" stored and high resistance providing no path to ground, while the one depicted in black has a "0" stored and low resistance.



**Figure 3.12: Memristive CAM array circuit in 2T-2M topology with the discharge path in red**

Memristive CAM array operates in two cycles. In the first cycle, output

from the first pair of compared, combined and thresholded frames is written into memristors. Transistor inputs as well row capacitors are disconnected during the write cycle. During the second cycle, output from the second pair of compared, combined and thresholded frames is provided as an input to transistor's gate and a comparison is carried out. Since complementary output are required, thresholding stage is embedded with an inverter to produce complementary outputs. Write and read cycles for CAM array are illustrated in Fig. 3.13 .

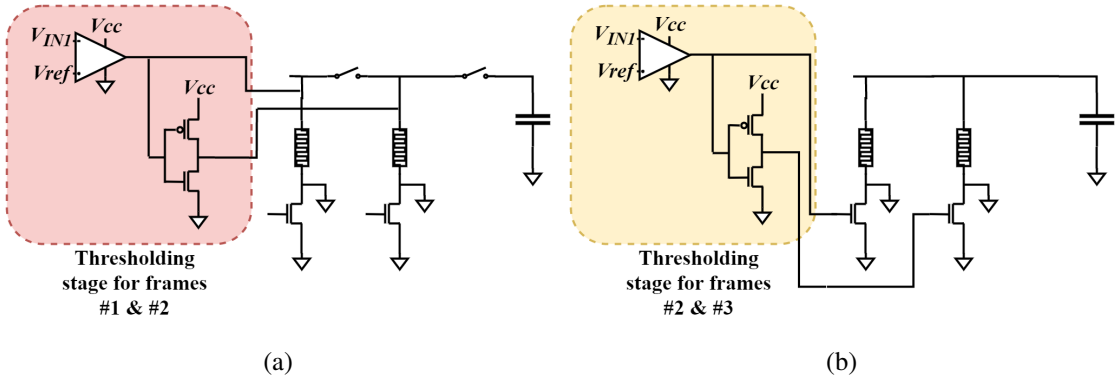


Figure 3.13: Write and read cycles for memristive CAM array. (a) write cycle, (b) read cycle

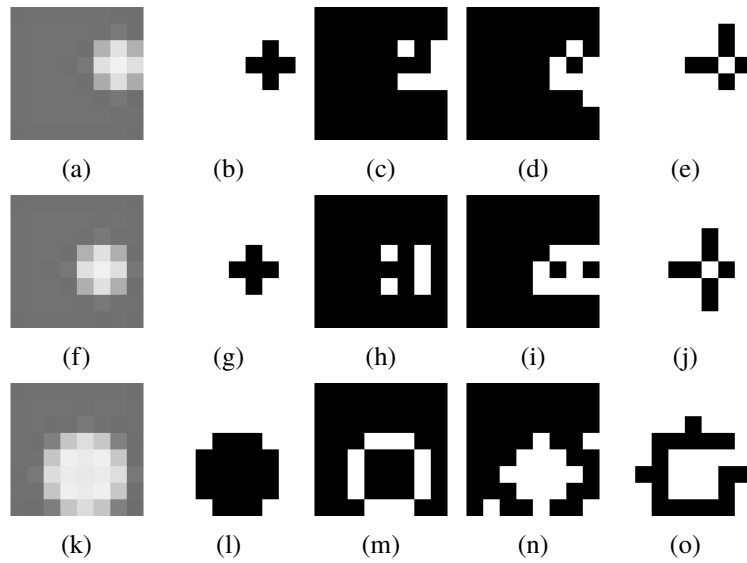
## Chapter 4 – Results

Simulations were performed in LTSpice environment with the help of netlist generated in MATLAB. CMOS technology is based on *TSMC* technology *BSIM* model with a feature size of  $250nm$ . Memristive device model is based on the model presented in [13], which has a large  $R_{ON}/R_{OFF}$  ratio. The memristor model used in the circuit has some variations in device's threshold voltage  $V_{thresh}$ . In crossbar array and weighted summation circuit, memristive devices have threshold voltage  $V_{thresh}$  higher than  $1V$ . Input memristors for threshold logic gate (different from control memristor) also have a static resistance, while in all other stages memristors' threshold voltage  $V_{thresh}$  is set to be smaller than  $1V$ . The power supply  $V_{CC}$  is kept at  $1V$ , the logic gate output is  $1V$  for logic high and  $0V$  for logic low. Op amp model used in the circuit is based on LM741 model. CAM capacitor has a capacitance of  $100pF$  and an initial charged voltage of  $0.65V$  in order to avoid resetting of memristive devices in CAM.

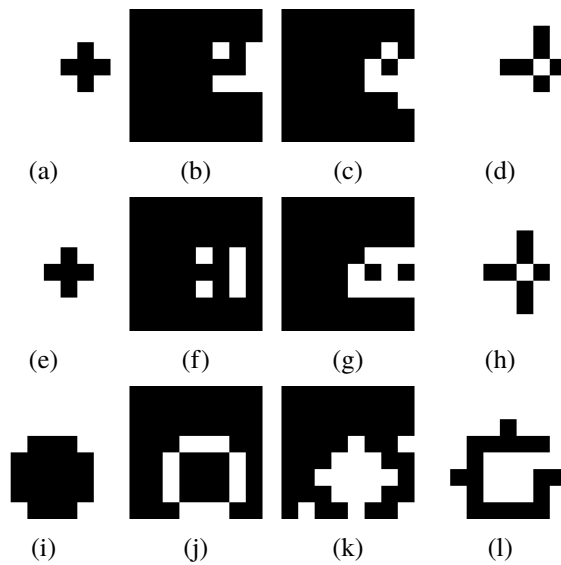
### 4.1 Crossbar array

Crossbar array performance is observed via storing 4 high order bit planes of three target images, imitating three consequent frames. Images have a size of  $8 \times 8$  pixels and have a distinct difference between each other. Target images along with their higher order bit planes are represented in Fig. 4.1 respectively. Bit sequences are extracted from the comparator circuit in the form of voltage waveforms. Circuit results are exported into MATLAB in order to visualize the extracted sequences. Binary images corresponding to bit planes of three

different frames stored to and extracted from crossbar array are presented in Fig. 4.2.



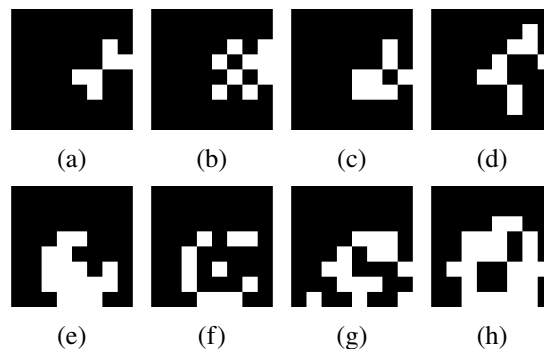
**Figure 4.1:** Original grayscale images for frames #1, #2, and #3 with higher order bit planes. (a),(f),(k) Original grayscale image, (b),(g),(l) MSB plane, (c),(h),(m) 6th bit plane, (d),(i),(n) 5th bit plane, (e),(j),(o) 4th bit plane



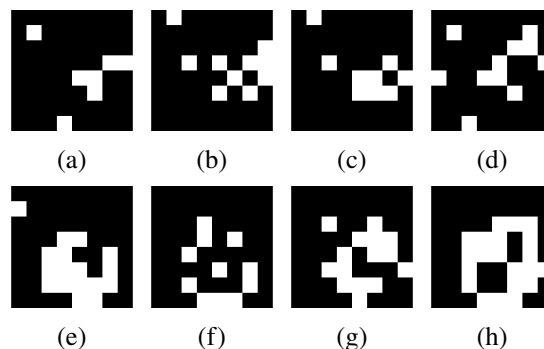
**Figure 4.2:** Bit planes stored to and extracted from crossbar array by using MATLAB. (a)-(d) bit planes of frame #1, (e)-(h) bit planes of frame #2, (i)-(l) bit planes of frame #3

## 4.2 Threshold logic gates

Logic gates compare the corresponding bit planes of first and second pair of consecutive frames. First pair implies frames #1 and #2, while the second pair implies frames #2 and #3. Performance of threshold logic gate is observed by exporting SPICE output into MATLAB. Manually XORed bit planes and TLG output of first and second pair of frames are presented in Fig. 4.3 and Fig. 4.4 respectively. As can be seen from the figures, there are slight deviations between manually obtained XORed bit planes and the ones obtained from circuit. Accuracy aspect is more thoroughly observed in the following chapters, with the dependence on the simulation array size.



**Figure 4.3:** Manually XORed bit planes of the first (a)-(d) and second (e)-(h) pair of consecutive frames. (a),(e) - MSB, (b),(f) - 6th bit, (c),(g) - 5th bit, (d),(h) - 4th bit

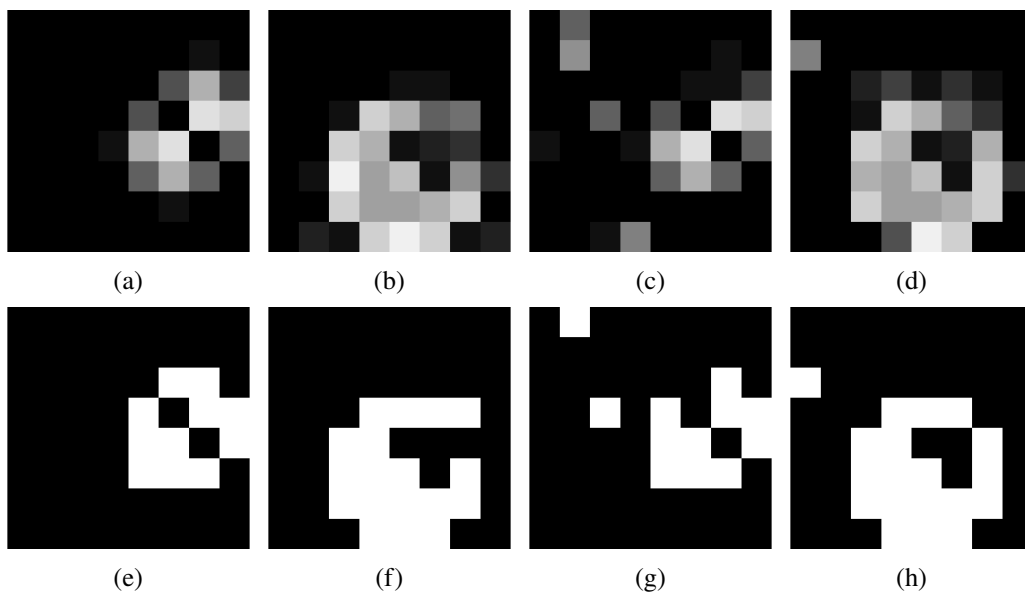


**Figure 4.4:** XORed bit planes of the first (a)-(d) and second (e)-(h) pair of consecutive frames derived from threshold logic gate. (a),(e) - MSB, (b),(f) - 6th bit, (c),(g) - 5th bit, (d),(h) - 4th bit

### 4.3 Weighted summation and thresholding

In order to observe the operation of the weighted summation stage and thresholding stage, results obtained from the algorithm and from the circuit are illustrated. Manual weighted summation is accomplished via multiplying the respective bit planes by the assigned weights and adding them together in MATLAB, while the output from circuit is exported and read via MATLAB. The results are presented in Fig. 4.5.

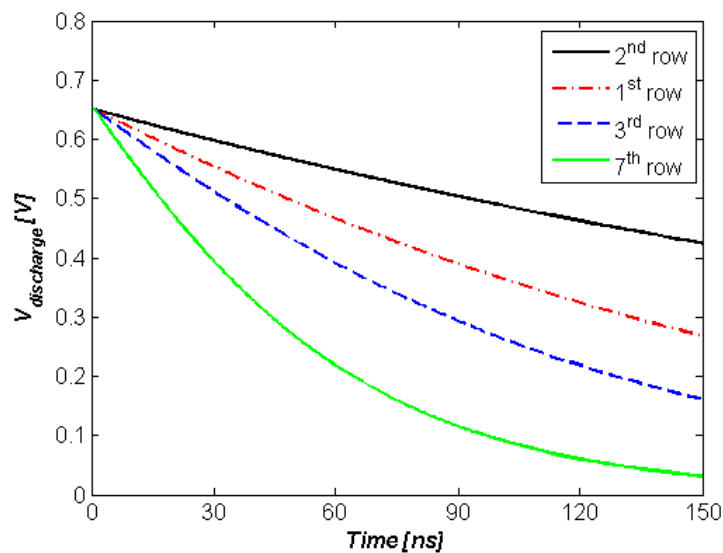
Thresholding results are obtained by using *im2bw* function in MATLAB with thresholding value of 0.25, while circuit output is exported and read. The circuit's reference voltage  $V_{REF}$  is also set to 0.25V. Thresholded images for both methods are illustrated in Fig. 4.5.



**Figure 4.5:** Grayscale and thresholded images from weighted addition manually (a),(b) and from circuit(c),(d). (a),(c) first pair of frames, (b),(d) second pair of frames

## 4.4 CAM array

Output from the CAM array is formed by observing the discharge curves from matching and mismatching of the thresholded images from the first and second pair of frames. Discharge behaviour is dependent on the number of different bits in each row. Discharge curves from the CAM array for several scenarios are presented in Fig. 4.6. Note that the second row of two images ( $g$ ), ( $h$ ) from Fig. 4.5 are fully matched, first row is mismatched by 1 bit, 3rd row is mismatched by 2 bits, and the 7th row is mismatched by 5 bits.

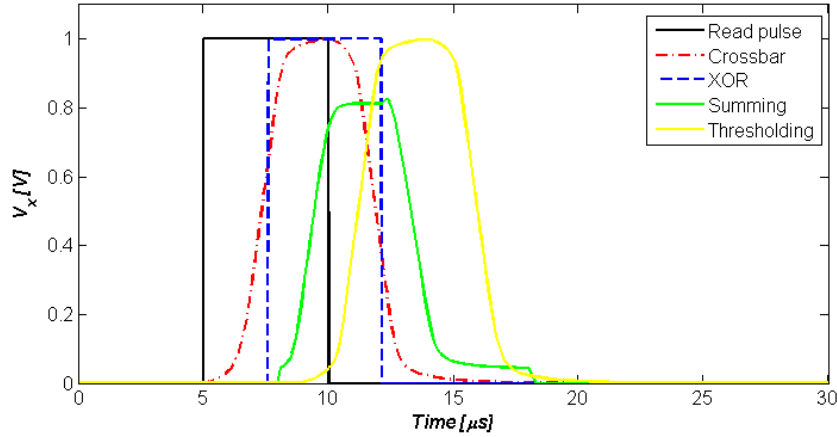


*Figure 4.6: Capacitor voltage discharge curves for match and mismatch cases*

## 4.5 Delay and pulse duration

Due to the implementation of CMOS technologies and op amps, the delay is obtained at the output of each stage. Delay is visualized by analyzing output voltage waveforms after each stage. In addition to signal delays, the effective

duration of pulses is also altered after each stage. This can be seen in Fig 4.7 , where read pulses as well as voltages after each stage are illustrated.



*Figure 4.7: Voltage waveforms obtained after each stage*

*Table 4.1: Delay and changes in pulse duration after each stage*

Stage	Delay ( $\mu s$ )	Pulse duration ( $\mu s$ )
Read	0	5
Crossbar	2.35	4.6
XOR	0.27	4.5
Summing	1.94	3.9
Thesholding	1.82	3.8
Total	6.35	NA

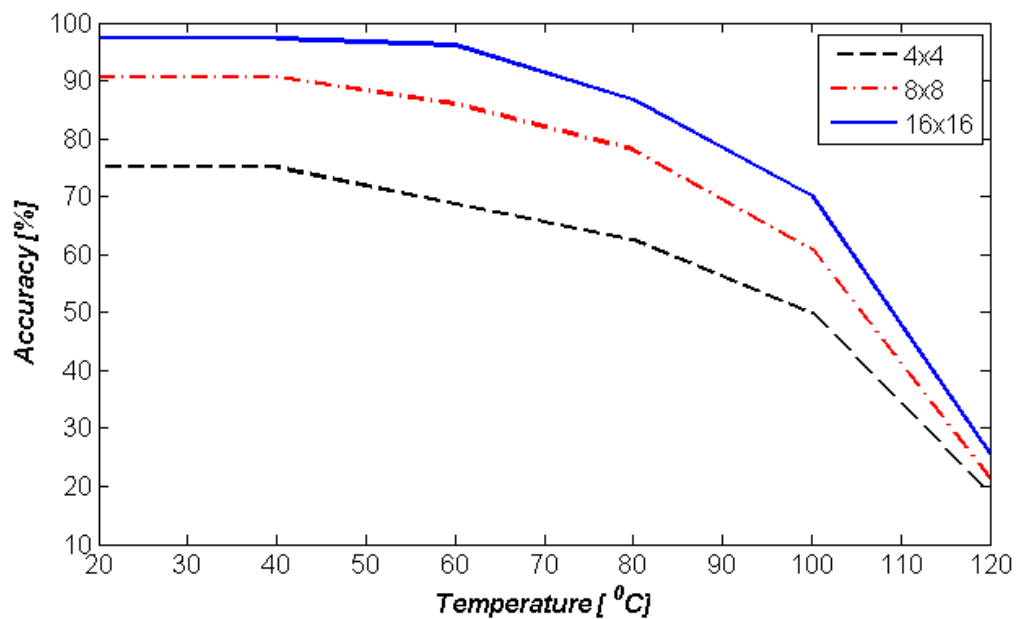
## 4.6 Accuracy, power & area

As can be seen for the XOR stage output, deviations between the circuit output and MATLAB processed images are present. Errors are mostly introduced by TLG stage; however, simulations of larger arrays display better accuracy since incorrectly perceived pixels' number lies in the vicinity of 4-6 pixels for each array. Accuracy, power and area of the proposed circuit for three size configurations are shown in Table 4.2.

In addition to this, temperature sensitivity analysis is accomplished to observe the dependence on temperature variations. Temperature sensitivity analysis shows the acceptable operation of circuit up to  $60^{\circ}\text{C}$  for smaller array size and up to  $80^{\circ}\text{C}$  for bigger array. Dependence of accuracy on temperature is illustrated in Fig. 4.8

**Table 4.2: Accuracy, area and power for different array size**

Array size	Accuracy (%)	Area ( $\mu\text{m}^2$ )	Power ( $\mu\text{W}$ )
4x4	75	1398.2	27.34
8x8	90.6	2703.5	51.63
16x16	97.3	5932.3	107.3



**Figure 4.8: Sensitivity graph showing dependence of accuracy on temperature**

## Chapter 5 – Discussions and conclusions

This thesis focuses on implementation of moving object detection algorithm via incorporation of memristive devices. In the first stage of proposed circuit, extracted binary bit planes of test images are stored in memristive cross-bar arrays in either low or high resistance. Respective bit planes are compared via memristive TLG and combined by weighted addition. Binary image of the detected object is obtained by setting appropriate thresholding level and filtering the noise out. The last stage comprises CAM array, which serves two purposes. First, CAM array is used as a long-term memory which updates when significant difference between two inputs is observed. This allows for more efficient memory utilization and less dissipated power by overwriting only different rows of bits. Second, CAM array allows for analysing capability by observing the capacitor discharge behaviour. Row-wise discharge analysis allows for determining horizontal, vertical or diagonal movement of the object. In addition to this, it is also possible to determine the velocity of the object. If particular rows are discharged with a difference of specific number of bits/pixels, by knowing the time between two input images, it is possible to estimate object's velocity.

As can be seen from the results, very high accuracy is potentially achieved with the increasing array size. The errors are introduced during the comparison stage, which incorporates memristive threshold logic gate. This is ascribed to the resistance of several control memristive devices in TLG, which do not completely tend to change its resistance to produce necessary output. Although, it poses a significant issue for a small array, the number of incorrectly compared pixels is fixed in the range of 4-6 pixels, which still leads to a high accuracy

using a large array size. According to results, proposed circuit is also tolerant to temperature fluctuations and illustrate satisfactory operation up to  $60^{\circ}C$  for small array size and up to  $80^{\circ}C$  for larger array size.

Additional issue lies in the delay and alteration of pulse duration of output signals. This is due to parasitic capacitance in CMOS inverters and slew rate of op amps. It can be seen that the output of the proposed circuit is delayed by  $6.35 \mu s$ , which is detrimental for very high frequency image processing. However, for conventional videos of 30 frames per second, the delay is insignificant. Number of stages stays the same irrespective of array size leading to the same delay time for both small and large pixel frames. This means that high-quality videos of high resolution can potentially be processed with the same delay as the test figures used in thesis.

Power and area calculation results show that proposed circuit has small area and overall power dissipation. In addition to this, crossbar arrangement allows for parallel scalability and high speed operation in parallel. Taking all these features into account, the proposed circuit is a viable candidate for integration with the existing image sensors as a co-processing operator.

Proposed circuit shows satisfactory operation and the results obtained are mostly compliant with algorithm implementation. Improvements could be potentially introduced to several stages of proposed circuit to increase robustness, speed and overall performance. As mentioned before, memristive elements in crossbar array are read row-wise one element at a time. With this approach, sneak path problem is solved; however, the reading time for large images may increase to several seconds for a single frame. Long reading time issue can be tackled by one of the solutions to sneak path problem proposed in [20]. Proposed

circuit can also be improved using a better option for comparator and summing circuits than LM741 op amp. Choice of an operational amplifier with a higher slew rate and smaller power dissipation can significantly boost circuit performance. To further enhance the accuracy, the issue of TLG should be addressed as it is the only stage where the error is introduced at a room temperature operation. Future work for this project would comprise several steps. First step would be to simulate the proposed circuit with the inclusion of tolerance and a small degree of randomness. This will better approximate real-life hardware implementation of circuit and give a better analysis in terms of metrics. Second step would be a simulation of a larger array (e.g. 1024\*768 px) to observe the performance on real-live videos from surveillance cameras, for example. After careful consideration of all these issues, hardware implementation of the proposed circuit can be carried out.

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# Appendix

## Appendix A - SPICE memristor model

```

*****
* MS - Modified S model;
*****
.SUBCKT MSmodel A B
*Modified S-model
.params RON=0.1K ROFF=100K VTH=0.7 K=-200e7 a=400 RINI=19K
.params DELTAR='ROFF-RON' XINI='(ROFF-RINI)/DELTAR'
.func FS(x)={1/a*log((1+exp(a*(x+0.5)))/
+           (1+exp(a*(x-0.5))))}
.param Y0='xini-0.5+1/a*log(1-exp(-a*xini))
+           -1/a*log(1-exp(-a*(1-xini)))'
.func thr(x,th)='if(x<=-th,x+th,if(x>=th,x-th,0))'

*State Equation
GY 0 Y VALUE={1m*k*thr(v(A,B),Vth)/
+           (ROFF-DELTAR*FS(Y0+V(Y)))}
CY Y 0 1m
RY Y 0 1T
.IC v(Y)=0

*Port Equation
GM A B VALUE={v(A,B)/(ROFF-DELTAR*FS(Y0+V(Y)))}
Rp A B 1T

.ENDS MSmodel

```

## Appendix B - MATLAB code (without CAM)

```

%% MATLAB code to generate memristor CAM array netlist

clc,clear all;
% initialization of array size
rows = 8;
cols = 8;

% initialization of cells to store grayscale images &
% bit planes
N = 3;
T=cell(N,9);
xored=cell(N-1,4);
final=cell(N-1,1);
for i=1:N;
    I=imread(strcat(num2str(i),'.jpg'));
    bbb= rgb2gray(I);
    bbb=imresize(bbb,[rows cols]);
    T{i,1}=bbb;
    filename=strcat('figure',num2str(i),'.jpg');
    imwrite(bbb,filename);
    for j=2:9
        T{i,j}=mod(floor(T{i,1}/2^(j-2)),2);
        T{i,j}=im2double(T{i,j}*255);
    end
end

% formation of XORed bit planes to compare with circuit output
for kk=5:8
    for ll=1:N-1
        xored{ll,kk}=xor(T{ll,kk+1},T{ll+1,kk+1});
    end
end

% formation of grayscale image to compare with circuit output
for tr=1:N-1
    final{tr,1}=0.5*xored{tr,8}+0.25*xored{tr,7}+...
        0.125*xored{tr,6}+0.0625*xored{tr,5};
end

%%

%creation of txt file to save the generated netlist
ID = fopen('spice.txt','wt');

%comments in netlist for clarification
fprintf(ID,['* This is a SPICE code generator\n',...
'* Bit planes of frame #1 are stored in crossbar arrays #1-4\n',...
'* Bit planes of frame #2 are stored in crossbar arrays #5-8\n',...
'* Bit planes of frame #3 are stored in crossbar arrays #9-12\n',...
'* Bits are read from all crossbar arrays simultaneously\n',...
'* Respective bit planes of consequent frames are XORed\n',...
'* E.g. XOR(frame #1 bit plane 8, frame #2 bit plane 8)\n',...
'* Vp, Vn - voltages to set the memristors into ON/OFF states\n',...
'* Vwrite, Vread - voltages to control switches for write and read cycle\n',...
'* Vr - input voltage for reading (< than memristor Vth)\n',...
'* Vrefcross - reference voltage for crossbar comparator circuit\n',...
'* Vrefthresh - reference voltage for thresholding stage\n',...
'* Vccomp, Vnncomp - +ve & -ve supply voltages for crossbar comparator op amp\n',...
'* Vccsum, Vnnsum - +ve & -ve supply voltages for summing op amp\n',...
'* Vdd - CMOS supply voltage\n',...
'* Voutread - voltage corresponding to bit values stored in crossbar array\n',...
'* Vxored - voltage corresponding XORED value of bits\n',...
'* Vinvsum - voltage corresponding to weighted addition of XORED bits\n',...
'* Vtotal - voltage corresponding to thresholded output\n\n\n']);

%inclusion of required libraries and models
fprintf(ID,['.model SW SW(Vt=0.5 Roff=1T)\n','.lib MScam.sub\n',...1
'.include tsmc_model_250nm.txt\n','.lib MS.sub\n',...
'.lib MSnew.sub\n',...
'.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.mos\n',...
'.model NMOS NMOS\n','.model PMOS PMOS\n','.lib UniversalOpamps2.sub\n',...
'.lib BEE215\ua741.lib\n\n']);

%adjusting parameters to increase simulation speed
fprintf(ID,['.options gmin=1e-9\n',...
'.options abstol=1e-9\n',...

```

```

'.options reltol=0.003\n',...
'.options cshunt=1e-16\n\n']);

%signal generation
fprintf(ID,['Vp Vp 0 2\n','Vn Vn 0 -7\n','Vrefcross Vrefcross 0 0.5\n',...
'Vr Vr 0 1\n','Vdd Vdd 0 1\n','Vcccomp Vcccomp 0 3.01\n',...
'Vrefthresh Vrefthresh 0 0.2\n',...
'Vnncomp Vnncomp 0 -1.995\n','Vccsum Vccsum 0 2.05\n',...
'Vnsum Vnsum 0 -3.01\n\n',...
'Vwrite Vwrite 0 PULSE (0 1 0 in 1n 9.2u 10u 1)\n']);

fprintf(ID,['Vcontrol+ Vcontrol+ 0 0.2\n',...
'Vcontrol- Vcontrol- 0 -0.2\n',...
'Vdd Vdd 0 1\n']);

for yt = 1:cols
fprintf(ID,'VwriteXOR%d VwriteXOR%d 0 PULSE(0 1 %du 1n 1n 5u %du) \n',...
[yt,yt,(yt)*5-5+0.01,5*cols]);
fprintf(ID,'VreadXOR%d VreadXOR%d 0 PULSE (0 1 %du 1n 1n 5u %du)\n',...
[yt,yt,10+(yt)*5-5+0.01,5*cols]);
end

for i=1:rows
fprintf(ID,'Vread%d Vread%d 0 PULSE(0 1 %du 1n 1n %du %du 1)\n',...
[i,i,10+(i-1)*5*cols, 5*cols, 5*cols]);
end

for y=1:cols
fprintf(ID,'Vreadcol%d Vreadcol%d 0 PULSE(0 1 %du 1n 1n 5u %du)\n',...
[y,y, 10+(y-1)*5,5*cols]);
end

fprintf(ID,'\n');
% ARRAY A

%generate crossbar array for higher order bit planes of 3 frames
%4 higher order bit planes * 3 frames = 12 crossbar arrays
for tq=1:12
if tq>0 && tq<5
A = T{1,10-tq};
elseif tq>4 && tq<9
A = T{2,10-tq+4};
else
A = T{3,10-tq+8};
end
%generation of switches connecting input to rows and cells to each other
for hh = 1:rows
for k=1:cols
if (mod(k+(hh-1)*2*cols,2*cols)==1)
fprintf(ID,'S%d Vr N%03d Vread%d 0 SW\n',...
[2*cols*(rows+1)*(tq-1)+k+(hh-1)*2*cols,...
(tq-1)*cols*(rows+2)+k+(hh-1)*cols,hh]);
else
fprintf (ID,'S%d N%03d N%03d Vread%d 0 SW\n',...
[2*cols*(rows+1)*(tq-1)+2*k-1+(hh-1)*2*cols,...
cols*(rows+2)*(tq-1)+k-1+(hh-1)*cols,...
cols*(rows+2)*(tq-1)+k+(hh-1)*cols,hh]);
end
end
end

%generation of switches for memristor setting
for ii = 1:rows
for ll = 1:cols
if A(ii,ll)==1
fprintf(ID,'S%d Vp N%03d Vwrite 0 SW\n',...
[2*cols*(rows+1)*(tq-1)+2*ll+(ii-1)*2*cols,...
cols*(rows+2)*(tq-1)+ll+(ii-1)*cols]);
elseif A(ii,ll)==0
fprintf(ID,'S%d Vn N%03d Vwrite 0 SW\n',...
[2*cols*(rows+1)*(tq-1)+2*ll+(ii-1)*2*cols,...
cols*(rows+2)*(tq-1)+ll+(ii-1)*cols]);
end
end
end

for gg = 1:cols
fprintf(ID,'S%d 0 N%03d Vwrite 0 SW\n',...
[2*cols*(rows+1)*(tq-1)+2*rows*cols+gg, ...
cols*(rows+2)*(tq-1)+rows*cols+gg]);
end

%generation of memristors in crossbar array
for jj = 1:rows

```

```

    for rr = 1:cols
        fprintf(ID,'XU%d N%03d N%03d MScammodel MScammodel\n',...
            [cols*(rows+1)*(tq-1)+rr+(jj-1)*cols,...
            cols*(rows+2)*(tq-1)+rows*cols+rr,...
            cols*(rows+2)*(tq-1)+rr+(jj-1)*cols]);
    end
end

%generation of switches for comparator circuit
for tt = 1:cols
    fprintf(ID,'S%d N%03d N%03d Vreadcol%d 0 SW\n',...
        [2*cols*(rows+1)*(tq-1)+cols*(2*rows+1)+tt,...
        cols*(rows+2)*(tq-1)+rows*cols+tt,...
        cols*(rows+2)*(tq-1)+cols*(rows+1)+tt,tt]);
end

%generation of load resistors for comparator
for oo=1:cols
    fprintf(ID,'R%d N%03d 0 57k\n',...
        [oo+cols*(tq-1),cols*(rows+2)*(tq-1)+cols*(rows+1)+oo]);
end

%generation of op-amps for comparator
for pp=1:cols
    fprintf(ID,'XU%d N%03d Vrefcross Vcccomp Vnncomp Voutread%d%d ua741\n',...
        [cols*(rows+1)*(tq-1)+rows*cols+pp,...
        cols*(rows+2)*(tq-1)+cols*(rows+1)+pp,tq,pp]);
end
%
%%% For XOR gates
if tq<5
    for qe=1:cols
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSmodel MSmodel\n',...
            [(qe-1)*3+1+(tq-1)*3*cols, tq,qe,tq,qe]);
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSmodel MSmodel\n',...
            [(qe-1)*3+2+(tq-1)*3*cols, tq,qe,tq,qe]);
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSnewmodel MSnewmodel\n',...
            [(qe)*3+1+(tq-1)*3*cols, tq,qe,tq,qe]);
    end
end
if tq>4 && tq<9
    for qe=1:cols
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSmodel MSmodel\n',...
            [(qe-1)*3+1+(tq-1)*3*cols, tq,qe,tq,qe]);
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSmodel MSmodel\n',...
            [(qe-1)*3+2+(tq-1)*3*cols, tq,qe,tq,qe]);
        fprintf(ID,'XU1000%d Voutread%d%d Vinpvtinv%d%d MSnewmodel MSnewmodel\n',...
            [(qe)*3+1+(tq-1)*3*cols, tq,qe,tq,qe]);
    end
end

%%% For summing opamps
if tq<5
    for yt=1:cols
        fprintf(ID,'Rin%d%d Vxored%d%d Vinpvt1%d %dk\n',...
            [tq,yt,tq,yt,yt,2^(tq)]);
        if tq==1
            fprintf(ID,'Rfeed%d%d Vinpvt1%d Vsum1%d 1k\n',...
                [tq,yt,yt,yt]);
            fprintf(ID,'XU%d 0 Vinpvt1%d Vccsum Vnnsum Vsum1%d ua741\n',...
                [rows*(cols+1)*12+yt,yt,yt]);
            fprintf(ID,'Rinvin%d%d Vsum1%d Vinpvtphase1%d 10k\n',...
                [tq,yt,yt,yt]);
            fprintf(ID,'Rfeedphase%d%d Vinpvtphase1%d Vinvsum1%d 10k\n',...
                [tq,yt,yt,yt]);
            fprintf(ID,'XU%d 0 Vinpvtphase1%d Vcccomp Vnncomp Vinvsum1%d ua741\n',...
                [rows*(cols+1)*12+2*cols+yt, yt,yt]);
            fprintf(ID,'XU%d Vinvsum1%d Vrefthresh Vcccomp Vnncomp Vtotal1%d ua741\n',...
                [rows*(cols+1)*12+3*cols+yt,yt,yt]);
            fprintf(ID,'M%d%d Vdd Vtotal1%d Vinvttotal1%d Vdd CMOS1 l=250n w=2500n\n',...
                [tq,yt,yt,yt]);
            fprintf(ID,'M%d%d Vinvttotal1%d Vtotal1%d 0 0 CMOSN l=250n w=2500n \n',...
                [tq,yt+cols,yt,yt]);
        end
    end
end
if tq>4 && tq<9
    for yt=1:cols
        fprintf(ID,'Rin%d%d Vxored%d%d Vinpvt2%d %dk\n',...
            [tq,yt,tq,yt,yt,2^(tq-4)]);
        if tq==5
            fprintf(ID,'Rfeed%d%d Vinpvt2%d Vsum2%d 1k\n',...
                [tq-3,yt,yt,yt]);
        end
    end
end

```

```

fprintf(ID,'XU%d 0 Vinut2%d Vccsum Vnnsum Vsum2%d ua741\n',...
[rows*(cols+1)*12+cols+yt,yt,yt]);
fprintf(ID,'Rinvin%d%d Vsum2%d Vinutphase2%d 10k\n',...
[tq-3,yt,yt,yt]);
fprintf(ID,'Rfeedphase%d%d Vinutphase2%d Vinvsum2%d 10k\n',...
[tq-3,yt,yt,yt]);
fprintf(ID,'XU%d 0 Vinutphase2%d Vcccomp Vnncomp Vinvsum2%d ua741\n',...
[rows*(cols+1)*12+4*cols+yt, yt,yt]);
fprintf(ID,'XU%d Vinvsum2%d Vrefthresh Vcccomp Vnncomp Vtotal2%d ua741\n',...
[rows*(cols+1)*12+5*cols+yt,yt,yt]);
fprintf(ID,'M%d%d Vdd Vtotal2%d Vinvtotal2%d Vdd CMOSP l=250n w=2500n\n',...
[tq-3,yt,yt,yt]);
fprintf(ID,'M%d%d Vinvtotal2%d Vtotal2%d 0 0 CMOSN l=250n w=2500n \n',...
[tq-3,yt+cols,yt,yt]);
end
end
end
end
end
fprintf(ID, '.tran 0 %du 10u uic\n',[10+rows*cols*5+2]);
fprintf(ID,['.backanno\n','end\n']);

```

## Appendix C - MATLAB code for CAM array

```

FID = fopen('CAM.txt','wt');
%netlist generation
fprintf(FID,'* This is a SPICE code generator for CAM\n');
%include libraries and models
fprintf(FID,['.model SW SW(Vt=0.5 Roff=1T)\n',' .lib MS.sub\n',...
'.include tsmc_model_250nm.txt\n',...
'.lib C:\\PROGRA~2\\LTC\\LTSPIC~1\\lib\\cmp\\standard.mos\n',...
'.model NMOS NMOS\n\n']);
%adjusting parameters to increase simulation speed
fprintf(FID,['.options gmin=1e-9\n',...
'.options abstol=1e-9\n',...
'.options reltol=0.003\n',...
'.options cshunt=1e-16\n\n']);
%generate signals
fprintf(FID,['Vcc Vcc 0 1\n','Vp Vp 0 1\n','Vn Vn 0 -1\n',...
'Vwritecam Vwritecam 0 PULSE(0 1 0 1n 1n 3u 10u 1)\n',...
'Vreadcam Vreadcam 0 PULSE(0 1 10u 1n 1n 3u 10u 1)\n\n']);
for re=1:rows
    fprintf(FID,'C%d Cap%d 0 100p IC=0.65\n',...
        [re,re]);
end
frame12 = thresha;
frame23 = threshb;
for eq=1:rows
    for tq=1:cols
        if tq==1
            fprintf(FID,'S%d%d Cap%d Memin%d%d Vreadcam 0 SW\n',...
                [eq,tq,eq,eq,tq]);
            fprintf(FID,'S%d%d Memin%d%d Memin%d%d Vreadcam 0 SW\n',...
                [eq,tq+3,eq,tq,eq,tq+1]);
        else
            fprintf(FID,'S%d%d Memin%d%d Memin%d%d Vreadcam 0 SW\n',...
                [eq,(tq-1)*6+1,eq,(tq-1)*2,eq,(tq-1)*2+1]);
            fprintf(FID,'S%d%d Memin%d%d Memin%d%d Vreadcam 0 SW\n',...
                [eq,(tq-1)*6+4,eq,(tq-1)*2+1,eq,tq*2]);
        end
        fprintf(FID,'S%d%d Memout%d%d 0 Vwritecam 0 SW\n',...
            [eq,(tq-1)*6+3,eq,(tq-1)*2+1]);
        fprintf(FID,'S%d%d Memout%d%d 0 Vwritecam 0 SW\n',...
            [eq,tq*6,eq,tq*2]);
        fprintf(FID,'XU%d%d Memin%d%d Memout%d%d MSmodel MSmodel\n',...
            [eq,(tq-1)*2+1,eq,(tq-1)*2+1,eq,(tq-1)*2+1]);
        fprintf(FID,'XU%d%d Memin%d%d Memout%d%d MSmodel MSmodel\n',...
            [eq,tq*2,eq,tq*2,eq,tq*2]);
        if frame12(eq,tq)==1
            fprintf(FID,'S%d%d Memin%d%d Vp Vwritecam 0 SW\n',...
                [eq,(tq-1)*6+2,eq,(tq-1)*2+1]);
            fprintf(FID,'S%d%d Memin%d%d Vn Vwritecam 0 SW\n',...
                [eq,(tq-1)*6+5,eq,tq*2]);
        else
            fprintf(FID,'S%d%d Memin%d%d Vn Vwritecam 0 SW\n',...
                [eq,(tq-1)*6+2,eq,(tq-1)*2+1]);
            fprintf(FID,'S%d%d Memin%d%d Vp Vwritecam 0 SW\n',...
                [eq,(tq-1)*6+5,eq,tq*2]);
        end
        if frame23(eq,tq)==1
            fprintf(FID,'M%d%d Memout%d%d Vreadcam 0 0 CMOSN l=250n w=2500n\n',...
                [eq,(tq-1)*2+1,eq,(tq-1)*2+1]);
            fprintf(FID,'M%d%d Memout%d%d 0 0 CMOSN l=250n w=2500n\n',...
                [eq,tq*2,eq,tq*2]);
        else
            fprintf(FID,'M%d%d Memout%d%d 0 0 CMOSN l=250n w=2500n\n',...
                [eq,(tq-1)*2+1,eq,(tq-1)*2+1]);
            fprintf(FID,'M%d%d Memout%d%d Vreadcam 0 0 CMOSN l=250n w=2500n\n',...
                [eq,tq*2,eq,tq*2]);
        end
    end
end
end
fprintf(FID,['.tran 0 10.1u 10u uic\n',' .backanno\n',' .end\n']);

```

# Appendix D - SPICE netlist generation code (without CAM)

```
* This is a SPICE code generator
* Higher order bit planes of frame #1 are stored in crossbar arrays #1-4 during the write cycle
* Higher order bit planes of frame #2 are stored in crossbar arrays #5-8 during the write cycle
* Higher order bit planes of frame #3 are stored in crossbar arrays #9-12 during the write cycle
* Bits are read during the read cycle from all crossbar arrays simultaneously
* Respective bit planes of consequent frames are XORed to get the desired output
* E.g. XOR(frame #1 bit plane 8, frame #2 bit plane 8)

* Vp, Vn - voltages to set the memristors into ON and OFF states respectively
* Vwrite, Vread - voltages to control crossbar switches for write and read cycle respectively
* Vr - input voltage for reading (< than memristor Vth)
* Vrefcross - reference voltage for crossbar comparator circuit
* Vrefthresh - reference voltage for thresholding stage
* Vcccomp, Vnncomp - +ve & -ve supply voltages for crossbar comparator op amp
* Vccsum, Vnnsum - +ve & -ve supply voltages for summing op amp
* Vdd - CMOS supply voltage
* Voutread - voltage corresponding to bit values stored in crossbar array
* Vxored - voltage corresponding XORED value of bits
* Vinvsum - voltage corresponding to weighted addition of XORED bits
* Vtotal - voltage corresponding to thresholded output

.model SW SW(Vt=0.5 Roff=1T)
.lib MScam.sub
.include tsmc_model_250nm.txt
.lib MS.sub
.lib MSnew.sub
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.mos
.model NMOS NMOS
.model PMOS PMOS
.lib UniversalOpamps2.sub
.lib BEE215\ua741.lib

.options gmin=1e-9
.options abstol=1e-9
.options reltol=0.003
.options cshunt=1e-16

Vp Vp 0 2
Vn Vn 0 -7
Vrefcross Vrefcross 0 0.5
Vr Vr 0 1
Vdd Vdd 0 1
Vcccomp Vcccomp 0 3.01
Vrefthresh Vrefthresh 0 0.2
Vnncomp Vnncomp 0 -1.995
Vccsum Vccsum 0 2.05
Vnnsum Vnnsum 0 -3.01

Vwrite Vwrite 0 PULSE(0 1 0 1n 1n 9.2u 10u 1)
Vread1 Vread1 0 PULSE(0 1 10u 1n 1n 40u 40u 1)
Vread2 Vread2 0 PULSE(0 1 50u 1n 1n 40u 40u 1)
Vread3 Vread3 0 PULSE(0 1 90u 1n 1n 40u 40u 1)
Vread4 Vread4 0 PULSE(0 1 130u 1n 1n 40u 40u 1)
Vread5 Vread5 0 PULSE(0 1 170u 1n 1n 40u 40u 1)
Vread6 Vread6 0 PULSE(0 1 210u 1n 1n 40u 40u 1)
Vread7 Vread7 0 PULSE(0 1 250u 1n 1n 40u 40u 1)
Vread8 Vread8 0 PULSE(0 1 290u 1n 1n 40u 40u 1)
Vreadcol1 Vreadcol1 0 PULSE(0 1 10u 1n 1n 5u 40u)
Vreadcol2 Vreadcol2 0 PULSE(0 1 15u 1n 1n 5u 40u)
Vreadcol3 Vreadcol3 0 PULSE(0 1 20u 1n 1n 5u 40u)
Vreadcol4 Vreadcol4 0 PULSE(0 1 25u 1n 1n 5u 40u)
Vreadcol5 Vreadcol5 0 PULSE(0 1 30u 1n 1n 5u 40u)
Vreadcol6 Vreadcol6 0 PULSE(0 1 35u 1n 1n 5u 40u)
Vreadcol7 Vreadcol7 0 PULSE(0 1 40u 1n 1n 5u 40u)
Vreadcol8 Vreadcol8 0 PULSE(0 1 45u 1n 1n 5u 40u)

S1 Vr N001 Vread1 0 SW
S3 N001 N002 Vread1 0 SW
S5 N002 N003 Vread1 0 SW
S7 N003 N004 Vread1 0 SW
S9 N004 N005 Vread1 0 SW
```

S11 N005 N006 Vread1 0 SW  
S13 N006 N007 Vread1 0 SW  
S15 N007 N008 Vread1 0 SW  
S17 Vr N009 Vread2 0 SW  
S19 N009 N010 Vread2 0 SW  
S21 N010 N011 Vread2 0 SW  
S23 N011 N012 Vread2 0 SW  
S25 N012 N013 Vread2 0 SW  
S27 N013 N014 Vread2 0 SW  
S29 N014 N015 Vread2 0 SW  
S31 N015 N016 Vread2 0 SW  
S33 Vr N017 Vread3 0 SW  
S35 N017 N018 Vread3 0 SW  
S37 N018 N019 Vread3 0 SW  
S39 N019 N020 Vread3 0 SW  
S41 N020 N021 Vread3 0 SW  
S43 N021 N022 Vread3 0 SW  
S45 N022 N023 Vread3 0 SW  
S47 N023 N024 Vread3 0 SW  
S49 Vr N025 Vread4 0 SW  
S51 N025 N026 Vread4 0 SW  
S53 N026 N027 Vread4 0 SW  
S55 N027 N028 Vread4 0 SW  
S57 N028 N029 Vread4 0 SW  
S59 N029 N030 Vread4 0 SW  
S61 N030 N031 Vread4 0 SW  
S63 N031 N032 Vread4 0 SW  
S65 Vr N033 Vread5 0 SW  
S67 N033 N034 Vread5 0 SW  
S69 N034 N035 Vread5 0 SW  
S71 N035 N036 Vread5 0 SW  
S73 N036 N037 Vread5 0 SW  
S75 N037 N038 Vread5 0 SW  
S77 N038 N039 Vread5 0 SW  
S79 N039 N040 Vread5 0 SW  
S81 Vr N041 Vread6 0 SW  
S83 N041 N042 Vread6 0 SW  
S85 N042 N043 Vread6 0 SW  
S87 N043 N044 Vread6 0 SW  
S89 N044 N045 Vread6 0 SW  
S91 N045 N046 Vread6 0 SW  
S93 N046 N047 Vread6 0 SW  
S95 N047 N048 Vread6 0 SW  
S97 Vr N049 Vread7 0 SW  
S99 N049 N050 Vread7 0 SW  
S101 N050 N051 Vread7 0 SW  
S103 N051 N052 Vread7 0 SW  
S105 N052 N053 Vread7 0 SW  
S107 N053 N054 Vread7 0 SW  
S109 N054 N055 Vread7 0 SW  
S111 N055 N056 Vread7 0 SW  
S113 Vr N057 Vread8 0 SW  
S115 N057 N058 Vread8 0 SW  
S117 N058 N059 Vread8 0 SW  
S119 N059 N060 Vread8 0 SW  
S121 N060 N061 Vread8 0 SW  
S123 N061 N062 Vread8 0 SW  
S125 N062 N063 Vread8 0 SW  
S127 N063 N064 Vread8 0 SW  
S2 Vp N001 Vwrite 0 SW  
S4 Vp N002 Vwrite 0 SW  
S6 Vp N003 Vwrite 0 SW  
S8 Vp N004 Vwrite 0 SW  
S10 Vp N005 Vwrite 0 SW  
S12 Vp N006 Vwrite 0 SW  
S14 Vp N007 Vwrite 0 SW  
S16 Vp N008 Vwrite 0 SW  
S18 Vp N009 Vwrite 0 SW  
S20 Vp N010 Vwrite 0 SW  
S22 Vp N011 Vwrite 0 SW  
S24 Vp N012 Vwrite 0 SW  
S26 Vp N013 Vwrite 0 SW  
S28 Vp N014 Vwrite 0 SW  
S30 Vp N015 Vwrite 0 SW  
S32 Vp N016 Vwrite 0 SW  
S34 Vp N017 Vwrite 0 SW  
S36 Vp N018 Vwrite 0 SW  
S38 Vp N019 Vwrite 0 SW  
S40 Vp N020 Vwrite 0 SW  
S42 Vp N021 Vwrite 0 SW  
S44 Vp N022 Vwrite 0 SW  
S46 Vn N023 Vwrite 0 SW  
S48 Vp N024 Vwrite 0 SW  
S50 Vp N025 Vwrite 0 SW

```

S52 Vp N026 Vwrite 0 SW
S54 Vp N027 Vwrite 0 SW
S56 Vp N028 Vwrite 0 SW
S58 Vp N029 Vwrite 0 SW
S60 Vn N030 Vwrite 0 SW
S62 Vn N031 Vwrite 0 SW
S64 Vn N032 Vwrite 0 SW
S66 Vp N033 Vwrite 0 SW
S68 Vp N034 Vwrite 0 SW
S70 Vp N035 Vwrite 0 SW
S72 Vp N036 Vwrite 0 SW
S74 Vp N037 Vwrite 0 SW
S76 Vp N038 Vwrite 0 SW
S78 Vn N039 Vwrite 0 SW
S80 Vp N040 Vwrite 0 SW
S82 Vp N041 Vwrite 0 SW
S84 Vp N042 Vwrite 0 SW
S86 Vp N043 Vwrite 0 SW
S88 Vp N044 Vwrite 0 SW
S90 Vp N045 Vwrite 0 SW
S92 Vp N046 Vwrite 0 SW
S94 Vp N047 Vwrite 0 SW
S96 Vp N048 Vwrite 0 SW
S98 Vp N049 Vwrite 0 SW
S100 Vp N050 Vwrite 0 SW
S102 Vp N051 Vwrite 0 SW
S104 Vp N052 Vwrite 0 SW
S106 Vp N053 Vwrite 0 SW
S108 Vp N054 Vwrite 0 SW
S110 Vp N055 Vwrite 0 SW
S112 Vp N056 Vwrite 0 SW
S114 Vp N057 Vwrite 0 SW
S116 Vp N058 Vwrite 0 SW
S118 Vp N059 Vwrite 0 SW
S120 Vp N060 Vwrite 0 SW
S122 Vp N061 Vwrite 0 SW
S124 Vp N062 Vwrite 0 SW
S126 Vp N063 Vwrite 0 SW
S128 Vp N064 Vwrite 0 SW
S129 0 N065 Vwrite 0 SW
S130 0 N066 Vwrite 0 SW
S131 0 N067 Vwrite 0 SW
S132 0 N068 Vwrite 0 SW
S133 0 N069 Vwrite 0 SW
S134 0 N070 Vwrite 0 SW
S135 0 N071 Vwrite 0 SW
S136 0 N072 Vwrite 0 SW
XU1 N065 N001 MScammodel MScammodel
XU2 N066 N002 MScammodel MScammodel
XU3 N067 N003 MScammodel MScammodel
XU4 N068 N004 MScammodel MScammodel
XU5 N069 N005 MScammodel MScammodel
XU6 N070 N006 MScammodel MScammodel
XU7 N071 N007 MScammodel MScammodel
XU8 N072 N008 MScammodel MScammodel
XU9 N065 N009 MScammodel MScammodel
XU10 N066 N010 MScammodel MScammodel
XU11 N067 N011 MScammodel MScammodel
XU12 N068 N012 MScammodel MScammodel
XU13 N069 N013 MScammodel MScammodel
XU14 N070 N014 MScammodel MScammodel
XU15 N071 N015 MScammodel MScammodel
XU16 N072 N016 MScammodel MScammodel
XU17 N065 N017 MScammodel MScammodel
XU18 N066 N018 MScammodel MScammodel
XU19 N067 N019 MScammodel MScammodel
XU20 N068 N020 MScammodel MScammodel
XU21 N069 N021 MScammodel MScammodel
XU22 N070 N022 MScammodel MScammodel
XU23 N071 N023 MScammodel MScammodel
XU24 N072 N024 MScammodel MScammodel
XU25 N065 N025 MScammodel MScammodel
XU26 N066 N026 MScammodel MScammodel
XU27 N067 N027 MScammodel MScammodel
XU28 N068 N028 MScammodel MScammodel
XU29 N069 N029 MScammodel MScammodel
XU30 N070 N030 MScammodel MScammodel
XU31 N071 N031 MScammodel MScammodel
XU32 N072 N032 MScammodel MScammodel
XU33 N065 N033 MScammodel MScammodel
XU34 N066 N034 MScammodel MScammodel
XU35 N067 N035 MScammodel MScammodel
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XU38 N070 N038 MScammodel MScammodel
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XU47 N071 N047 MScammodel MScammodel
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XU63 N071 N063 MScammodel MScammodel
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S137 N065 N073 Vreadcol1 0 SW
S138 N066 N074 Vreadcol2 0 SW
S139 N067 N075 Vreadcol3 0 SW
S140 N068 N076 Vreadcol4 0 SW
S141 N069 N077 Vreadcol5 0 SW
S142 N070 N078 Vreadcol6 0 SW
S143 N071 N079 Vreadcol7 0 SW
S144 N072 N080 Vreadcol8 0 SW
R1 N073 0 57k
R2 N074 0 57k
R3 N075 0 57k
R4 N076 0 57k
R5 N077 0 57k
R6 N078 0 57k
R7 N079 0 57k
R8 N080 0 57k
XU65 N073 Vrefcross Vcccomp Vnncomp Voutread11 ua741
XU66 N074 Vrefcross Vcccomp Vnncomp Voutread12 ua741
XU67 N075 Vrefcross Vcccomp Vnncomp Voutread13 ua741
XU68 N076 Vrefcross Vcccomp Vnncomp Voutread14 ua741
XU69 N077 Vrefcross Vcccomp Vnncomp Voutread15 ua741
XU70 N078 Vrefcross Vcccomp Vnncomp Voutread16 ua741
XU71 N079 Vrefcross Vcccomp Vnncomp Voutread17 ua741
XU72 N080 Vrefcross Vcccomp Vnncomp Voutread18 ua741
A11 Voutread11 Voutread51 0 0 0 0 Vxored11 0 XOR td=0.27u
A12 Voutread12 Voutread52 0 0 0 0 Vxored12 0 XOR td=0.27u
A13 Voutread13 Voutread53 0 0 0 0 Vxored13 0 XOR td=0.27u
A14 Voutread14 Voutread54 0 0 0 0 Vxored14 0 XOR td=0.27u
A15 Voutread15 Voutread55 0 0 0 0 Vxored15 0 XOR td=0.27u
A16 Voutread16 Voutread56 0 0 0 0 Vxored16 0 XOR td=0.27u
A17 Voutread17 Voutread57 0 0 0 0 Vxored17 0 XOR td=0.27u
A18 Voutread18 Voutread58 0 0 0 0 Vxored18 0 XOR td=0.27u
Rin11 Vxored11 Vininput11 2k
Rfeed11 Vininput11 Vsum11 1k
XU865 0 Vininput11 Vccsum Vnnsum Vsum11 ua741
Rinvin11 Vsum11 Vininputphase11 10k
Rfeedphase11 Vininputphase11 Vinvsum11 10k
XU881 0 Vininputphase11 Vcccomp Vnncomp Vinvsum11 ua741
XU889 Vinvsum11 Vrefthresh Vcccomp Vnncomp Vtotal11 ua741
M11 Vdd Vtotal11 Vinvtotal11 Vdd CMOS l=250n w=2500n
M19 Vinvtotal11 Vtotal11 0 0 CMOS l=250n w=2500n
Rin12 Vxored12 Vininput12 2k
Rfeed12 Vininput12 Vsum12 1k
XU866 0 Vininput12 Vccsum Vnnsum Vsum12 ua741
Rinvin12 Vsum12 Vininputphase12 10k
Rfeedphase12 Vininputphase12 Vinvsum12 10k
XU882 0 Vininputphase12 Vcccomp Vnncomp Vinvsum12 ua741
XU890 Vinvsum12 Vrefthresh Vcccomp Vnncomp Vtotal12 ua741
M12 Vdd Vtotal12 Vinvtotal12 Vdd CMOS l=250n w=2500n
M110 Vinvtotal12 Vtotal12 0 0 CMOS l=250n w=2500n
Rin13 Vxored13 Vininput13 2k
Rfeed13 Vininput13 Vsum13 1k
XU867 0 Vininput13 Vccsum Vnnsum Vsum13 ua741
Rinvin13 Vsum13 Vininputphase13 10k
Rfeedphase13 Vininputphase13 Vinvsum13 10k
XU883 0 Vininputphase13 Vcccomp Vnncomp Vinvsum13 ua741

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XU891 Vinvsu13 Vrefthresh Vcccomp Vnncomp Vtotal13 ua741
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M111 Vinvtotal13 Vtotal13 0 0 CMOSN l=250n w=2500n
Rin14 Vxored14 Vinput14 2k
Rfeed14 Vinput14 Vsum14 1k
XU868 0 Vinput14 Vccsum Vnnsum Vsum14 ua741
Rinvin14 Vsum14 Vinputphase14 10k
Rfeedphase14 Vinputphase14 Vinvsu14 10k
XU884 0 Vinputphase14 Vcccomp Vnncomp Vinvsu14 ua741
XU892 Vinvsu14 Vrefthresh Vcccomp Vnncomp Vtotal14 ua741
M14 Vdd Vtotal14 Vinvtotal14 Vdd CMOSP l=250n w=2500n
M112 Vinvtotal14 Vtotal14 0 0 CMOSN l=250n w=2500n
Rin15 Vxored15 Vinput15 2k
Rfeed15 Vinput15 Vsum15 1k
XU869 0 Vinput15 Vccsum Vnnsum Vsum15 ua741
Rinvin15 Vsum15 Vinputphase15 10k
Rfeedphase15 Vinputphase15 Vinvsu15 10k
XU885 0 Vinputphase15 Vcccomp Vnncomp Vinvsu15 ua741
XU893 Vinvsu15 Vrefthresh Vcccomp Vnncomp Vtotal15 ua741
M15 Vdd Vtotal15 Vinvtotal15 Vdd CMOSP l=250n w=2500n
M113 Vinvtotal15 Vtotal15 0 0 CMOSN l=250n w=2500n
Rin16 Vxored16 Vinput16 2k
Rfeed16 Vinput16 Vsum16 1k
XU870 0 Vinput16 Vccsum Vnnsum Vsum16 ua741
Rinvin16 Vsum16 Vinputphase16 10k
Rfeedphase16 Vinputphase16 Vinvsu16 10k
XU886 0 Vinputphase16 Vcccomp Vnncomp Vinvsu16 ua741
XU894 Vinvsu16 Vrefthresh Vcccomp Vnncomp Vtotal16 ua741
M16 Vdd Vtotal16 Vinvtotal16 Vdd CMOSP l=250n w=2500n
M114 Vinvtotal16 Vtotal16 0 0 CMOSN l=250n w=2500n
Rin17 Vxored17 Vinput17 2k
Rfeed17 Vinput17 Vsum17 1k
XU871 0 Vinput17 Vccsum Vnnsum Vsum17 ua741
Rinvin17 Vsum17 Vinputphase17 10k
Rfeedphase17 Vinputphase17 Vinvsu17 10k
XU887 0 Vinputphase17 Vcccomp Vnncomp Vinvsu17 ua741
XU895 Vinvsu17 Vrefthresh Vcccomp Vnncomp Vtotal17 ua741
M17 Vdd Vtotal17 Vinvtotal17 Vdd CMOSP l=250n w=2500n
M115 Vinvtotal17 Vtotal17 0 0 CMOSN l=250n w=2500n
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Rfeed18 Vinput18 Vsum18 1k
XU872 0 Vinput18 Vccsum Vnnsum Vsum18 ua741
Rinvin18 Vsum18 Vinputphase18 10k
Rfeedphase18 Vinputphase18 Vinvsu18 10k
XU888 0 Vinputphase18 Vcccomp Vnncomp Vinvsu18 ua741
XU896 Vinvsu18 Vrefthresh Vcccomp Vnncomp Vtotal18 ua741
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M116 Vinvtotal18 Vtotal18 0 0 CMOSN l=250n w=2500n
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S147 N081 N082 Vread1 0 SW
S149 N082 N083 Vread1 0 SW
S151 N083 N084 Vread1 0 SW
S153 N084 N085 Vread1 0 SW
S155 N085 N086 Vread1 0 SW
S157 N086 N087 Vread1 0 SW
S159 N087 N088 Vread1 0 SW
S161 Vr N089 Vread2 0 SW
S163 N089 N090 Vread2 0 SW
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S171 N093 N094 Vread2 0 SW
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S175 N095 N096 Vread2 0 SW
S177 Vr N097 Vread3 0 SW
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S205 N110 N111 Vread4 0 SW
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S225 Vr N121 Vread6 0 SW  
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XU135 N151 N143 MScammodel MScammodel  
XU136 N152 N144 MScammodel MScammodel  
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S282 N146 N154 Vreadcol2 0 SW  
S283 N147 N155 Vreadcol3 0 SW

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S284 N148 N156 Vreadcol4 0 SW
S285 N149 N157 Vreadcol5 0 SW
S286 N150 N158 Vreadcol6 0 SW
S287 N151 N159 Vreadcol7 0 SW
S288 N152 N160 Vreadcol8 0 SW
R9 N153 0 57k
R10 N154 0 57k
R11 N155 0 57k
R12 N156 0 57k
R13 N157 0 57k
R14 N158 0 57k
R15 N159 0 57k
R16 N160 0 57k
XU137 N153 Vrefcross Vcccomp Vnncomp Voutread21 ua741
XU138 N154 Vrefcross Vcccomp Vnncomp Voutread22 ua741
XU139 N155 Vrefcross Vcccomp Vnncomp Voutread23 ua741
XU140 N156 Vrefcross Vcccomp Vnncomp Voutread24 ua741
XU141 N157 Vrefcross Vcccomp Vnncomp Voutread25 ua741
XU142 N158 Vrefcross Vcccomp Vnncomp Voutread26 ua741
XU143 N159 Vrefcross Vcccomp Vnncomp Voutread27 ua741
XU144 N160 Vrefcross Vcccomp Vnncomp Voutread28 ua741
A21 Voutread21 Voutread61 0 0 0 0 Vxored21 0 XOR td=0.27u
A22 Voutread22 Voutread62 0 0 0 0 Vxored22 0 XOR td=0.27u
A23 Voutread23 Voutread63 0 0 0 0 Vxored23 0 XOR td=0.27u
A24 Voutread24 Voutread64 0 0 0 0 Vxored24 0 XOR td=0.27u
A25 Voutread25 Voutread65 0 0 0 0 Vxored25 0 XOR td=0.27u
A26 Voutread26 Voutread66 0 0 0 0 Vxored26 0 XOR td=0.27u
A27 Voutread27 Voutread67 0 0 0 0 Vxored27 0 XOR td=0.27u
A28 Voutread28 Voutread68 0 0 0 0 Vxored28 0 XOR td=0.27u
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Rin22 Vxored22 Vinput12 4k
Rin23 Vxored23 Vinput13 4k
Rin24 Vxored24 Vinput14 4k
Rin25 Vxored25 Vinput15 4k
Rin26 Vxored26 Vinput16 4k
Rin27 Vxored27 Vinput17 4k
Rin28 Vxored28 Vinput18 4k
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S291 N161 N162 Vread1 0 SW
S293 N162 N163 Vread1 0 SW
S295 N163 N164 Vread1 0 SW
S297 N164 N165 Vread1 0 SW
S299 N165 N166 Vread1 0 SW
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S303 N167 N168 Vread1 0 SW
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S381 N206 N207 Vread6 0 SW

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S389 N210 N211 Vread7 0 SW  
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S422 0 N230 Vwrite 0 SW
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XU150 N230 N166 MScammodel MScammodel
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S718 N390 N398 Vreadcol6 0 SW
S719 N391 N399 Vreadcol7 0 SW
S720 N392 N400 Vreadcol8 0 SW
R33 N393 0 57k
R34 N394 0 57k
R35 N395 0 57k
R36 N396 0 57k
R37 N397 0 57k
R38 N398 0 57k
R39 N399 0 57k
R40 N400 0 57k
XU353 N393 Vrefcross Vcccomp Vnncomp Voutread51 ua741
XU354 N394 Vrefcross Vcccomp Vnncomp Voutread52 ua741
XU355 N395 Vrefcross Vcccomp Vnncomp Voutread53 ua741
XU356 N396 Vrefcross Vcccomp Vnncomp Voutread54 ua741
XU357 N397 Vrefcross Vcccomp Vnncomp Voutread55 ua741
XU358 N398 Vrefcross Vcccomp Vnncomp Voutread56 ua741
XU359 N399 Vrefcross Vcccomp Vnncomp Voutread57 ua741
XU360 N400 Vrefcross Vcccomp Vnncomp Voutread58 ua741
A51 Voutread51 Voutread91 0 0 0 0 Vxored51 0 XOR td=0.27u
A52 Voutread52 Voutread92 0 0 0 0 Vxored52 0 XOR td=0.27u
A53 Voutread53 Voutread93 0 0 0 0 Vxored53 0 XOR td=0.27u
A54 Voutread54 Voutread94 0 0 0 0 Vxored54 0 XOR td=0.27u
A55 Voutread55 Voutread95 0 0 0 0 Vxored55 0 XOR td=0.27u
A56 Voutread56 Voutread96 0 0 0 0 Vxored56 0 XOR td=0.27u
A57 Voutread57 Voutread97 0 0 0 0 Vxored57 0 XOR td=0.27u
A58 Voutread58 Voutread98 0 0 0 0 Vxored58 0 XOR td=0.27u
Rin51 Vxored51 Vininput21 2k
Rfeed21 Vininput21 Vsum21 1k
XU873 0 Vininput21 Vccsum Vnnsum Vsum21 ua741
Rinvin21 Vsum21 Vininputphase21 10k
Rfeedphase21 Vininputphase21 Vinvsum21 10k
XU897 0 Vininputphase21 Vcccomp Vnncomp Vinvsum21 ua741
XU905 Vinvsum21 Vrefthresh Vcccomp Vnncomp Vtotal21 ua741

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M21 Vdd Vtotal21 Vinvtotal21 Vdd CMOS l=250n w=2500n
M29 Vinvtotal21 Vtotal21 0 0 CMOSN l=250n w=2500n
Rin52 Vxored52 Vinut22 2k
Rfeed22 Vinut22 Vsum22 1k
XU874 0 Vinut22 Vccsum Vnnsum Vsum22 ua741
Rinvin22 Vsum22 Vinutphase22 10k
Rfeedphase22 Vinutphase22 Vinvsum22 10k
XU898 0 Vinutphase22 Vcccomp Vnncomp Vinvsum22 ua741
XU906 Vinvsum22 Vrefthresh Vcccomp Vnncomp Vtotal22 ua741
M22 Vdd Vtotal22 Vinvtotal22 Vdd CMOS l=250n w=2500n
M210 Vinvtotal22 Vtotal22 0 0 CMOSN l=250n w=2500n
Rin53 Vxored53 Vinut23 2k
Rfeed23 Vinut23 Vsum23 1k
XU875 0 Vinut23 Vccsum Vnnsum Vsum23 ua741
Rinvin23 Vsum23 Vinutphase23 10k
Rfeedphase23 Vinutphase23 Vinvsum23 10k
XU899 0 Vinutphase23 Vcccomp Vnncomp Vinvsum23 ua741
XU907 Vinvsum23 Vrefthresh Vcccomp Vnncomp Vtotal23 ua741
M23 Vdd Vtotal23 Vinvtotal23 Vdd CMOS l=250n w=2500n
M211 Vinvtotal23 Vtotal23 0 0 CMOSN l=250n w=2500n
Rin54 Vxored54 Vinut24 2k
Rfeed24 Vinut24 Vsum24 1k
XU876 0 Vinut24 Vccsum Vnnsum Vsum24 ua741
Rinvin24 Vsum24 Vinutphase24 10k
Rfeedphase24 Vinutphase24 Vinvsum24 10k
XU900 0 Vinutphase24 Vcccomp Vnncomp Vinvsum24 ua741
XU908 Vinvsum24 Vrefthresh Vcccomp Vnncomp Vtotal24 ua741
M24 Vdd Vtotal24 Vinvtotal24 Vdd CMOS l=250n w=2500n
M212 Vinvtotal24 Vtotal24 0 0 CMOSN l=250n w=2500n
Rin55 Vxored55 Vinut25 2k
Rfeed25 Vinut25 Vsum25 1k
XU877 0 Vinut25 Vccsum Vnnsum Vsum25 ua741
Rinvin25 Vsum25 Vinutphase25 10k
Rfeedphase25 Vinutphase25 Vinvsum25 10k
XU901 0 Vinutphase25 Vcccomp Vnncomp Vinvsum25 ua741
XU909 Vinvsum25 Vrefthresh Vcccomp Vnncomp Vtotal25 ua741
M25 Vdd Vtotal25 Vinvtotal25 Vdd CMOS l=250n w=2500n
M213 Vinvtotal25 Vtotal25 0 0 CMOSN l=250n w=2500n
Rin56 Vxored56 Vinut26 2k
Rfeed26 Vinut26 Vsum26 1k
XU878 0 Vinut26 Vccsum Vnnsum Vsum26 ua741
Rinvin26 Vsum26 Vinutphase26 10k
Rfeedphase26 Vinutphase26 Vinvsum26 10k
XU902 0 Vinutphase26 Vcccomp Vnncomp Vinvsum26 ua741
XU910 Vinvsum26 Vrefthresh Vcccomp Vnncomp Vtotal26 ua741
M26 Vdd Vtotal26 Vinvtotal26 Vdd CMOS l=250n w=2500n
M214 Vinvtotal26 Vtotal26 0 0 CMOSN l=250n w=2500n
Rin57 Vxored57 Vinut27 2k
Rfeed27 Vinut27 Vsum27 1k
XU879 0 Vinut27 Vccsum Vnnsum Vsum27 ua741
Rinvin27 Vsum27 Vinutphase27 10k
Rfeedphase27 Vinutphase27 Vinvsum27 10k
XU903 0 Vinutphase27 Vcccomp Vnncomp Vinvsum27 ua741
XU911 Vinvsum27 Vrefthresh Vcccomp Vnncomp Vtotal27 ua741
M27 Vdd Vtotal27 Vinvtotal27 Vdd CMOS l=250n w=2500n
M215 Vinvtotal27 Vtotal27 0 0 CMOSN l=250n w=2500n
Rin58 Vxored58 Vinut28 2k
Rfeed28 Vinut28 Vsum28 1k
XU880 0 Vinut28 Vccsum Vnnsum Vsum28 ua741
Rinvin28 Vsum28 Vinutphase28 10k
Rfeedphase28 Vinutphase28 Vinvsum28 10k
XU904 0 Vinutphase28 Vcccomp Vnncomp Vinvsum28 ua741
XU912 Vinvsum28 Vrefthresh Vcccomp Vnncomp Vtotal28 ua741
M28 Vdd Vtotal28 Vinvtotal28 Vdd CMOS l=250n w=2500n
M216 Vinvtotal28 Vtotal28 0 0 CMOSN l=250n w=2500n
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S723 N401 N402 Vread1 0 SW
S725 N402 N403 Vread1 0 SW
S727 N403 N404 Vread1 0 SW
S729 N404 N405 Vread1 0 SW
S731 N405 N406 Vread1 0 SW
S733 N406 N407 Vread1 0 SW
S735 N407 N408 Vread1 0 SW
S737 Vr N409 Vread2 0 SW
S739 N409 N410 Vread2 0 SW
S741 N410 N411 Vread2 0 SW
S743 N411 N412 Vread2 0 SW
S745 N412 N413 Vread2 0 SW
S747 N413 N414 Vread2 0 SW
S749 N414 N415 Vread2 0 SW
S751 N415 N416 Vread2 0 SW
S753 Vr N417 Vread3 0 SW
S755 N417 N418 Vread3 0 SW

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S793 N436 N437 Vread5 0 SW  
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S797 N438 N439 Vread5 0 SW  
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XU424 N472 N464 MScammodel MScammodel
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S859 N467 N475 Vreadcol3 0 SW
S860 N468 N476 Vreadcol4 0 SW
S861 N469 N477 Vreadcol5 0 SW
S862 N470 N478 Vreadcol6 0 SW
S863 N471 N479 Vreadcol7 0 SW
S864 N472 N480 Vreadcol8 0 SW
R41 N473 0 57k
R42 N474 0 57k
R43 N475 0 57k
R44 N476 0 57k
R45 N477 0 57k
R46 N478 0 57k
R47 N479 0 57k
R48 N480 0 57k
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XU426 N474 Vrefcross Vcccomp Vnncomp Voutread62 ua741
XU427 N475 Vrefcross Vcccomp Vnncomp Voutread63 ua741
XU428 N476 Vrefcross Vcccomp Vnncomp Voutread64 ua741
XU429 N477 Vrefcross Vcccomp Vnncomp Voutread65 ua741
XU430 N478 Vrefcross Vcccomp Vnncomp Voutread66 ua741
XU431 N479 Vrefcross Vcccomp Vnncomp Voutread67 ua741
XU432 N480 Vrefcross Vcccomp Vnncomp Voutread68 ua741
A61 Voutread61 Voutread101 0 0 0 0 Vxored61 0 XOR td=0.27u
A62 Voutread62 Voutread102 0 0 0 0 Vxored62 0 XOR td=0.27u
A63 Voutread63 Voutread103 0 0 0 0 Vxored63 0 XOR td=0.27u
A64 Voutread64 Voutread104 0 0 0 0 Vxored64 0 XOR td=0.27u
A65 Voutread65 Voutread105 0 0 0 0 Vxored65 0 XOR td=0.27u
A66 Voutread66 Voutread106 0 0 0 0 Vxored66 0 XOR td=0.27u
A67 Voutread67 Voutread107 0 0 0 0 Vxored67 0 XOR td=0.27u
A68 Voutread68 Voutread108 0 0 0 0 Vxored68 0 XOR td=0.27u
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Rin62 Vxored62 Vinput22 4k
Rin63 Vxored63 Vinput23 4k
Rin64 Vxored64 Vinput24 4k
Rin65 Vxored65 Vinput25 4k
Rin66 Vxored66 Vinput26 4k
Rin67 Vxored67 Vinput27 4k
Rin68 Vxored68 Vinput28 4k
S865 Vr N481 Vread1 0 SW
S867 N481 N482 Vread1 0 SW
S869 N482 N483 Vread1 0 SW
S871 N483 N484 Vread1 0 SW
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S875 N485 N486 Vread1 0 SW
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A74 Voutread74 Voutread114 0 0 0 0 Vxored74 0 XOR td=0.27u
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Rin76 Vxored76 Vinput26 8k
Rin77 Vxored77 Vinput27 8k
Rin78 Vxored78 Vinput28 8k
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A84 Voutread84 Voutread124 0 0 0 0 Vxored84 0 XOR td=0.27u
A85 Voutread85 Voutread125 0 0 0 0 Vxored85 0 XOR td=0.27u
A86 Voutread86 Voutread126 0 0 0 0 Vxored86 0 XOR td=0.27u
A87 Voutread87 Voutread127 0 0 0 0 Vxored87 0 XOR td=0.27u
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Rin86 Vxored86 Vinput26 16k
Rin87 Vxored87 Vinput27 16k
Rin88 Vxored88 Vinput28 16k
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S1647 N911 N912 Vread4 0 SW  
S1649 Vr N913 Vread5 0 SW  
S1651 N913 N914 Vread5 0 SW  
S1653 N914 N915 Vread5 0 SW  
S1655 N915 N916 Vread5 0 SW  
S1657 N916 N917 Vread5 0 SW  
S1659 N917 N918 Vread5 0 SW  
S1661 N918 N919 Vread5 0 SW  
S1663 N919 N920 Vread5 0 SW  
S1665 Vr N921 Vread6 0 SW  
S1667 N921 N922 Vread6 0 SW  
S1669 N922 N923 Vread6 0 SW  
S1671 N923 N924 Vread6 0 SW  
S1673 N924 N925 Vread6 0 SW  
S1675 N925 N926 Vread6 0 SW  
S1677 N926 N927 Vread6 0 SW  
S1679 N927 N928 Vread6 0 SW  
S1681 Vr N929 Vread7 0 SW  
S1683 N929 N930 Vread7 0 SW  
S1685 N930 N931 Vread7 0 SW  
S1687 N931 N932 Vread7 0 SW  
S1689 N932 N933 Vread7 0 SW  
S1691 N933 N934 Vread7 0 SW

S1693 N934 N935 Vread7 0 SW  
S1695 N935 N936 Vread7 0 SW  
S1697 Vr N937 Vread8 0 SW  
S1699 N937 N938 Vread8 0 SW  
S1701 N938 N939 Vread8 0 SW  
S1703 N939 N940 Vread8 0 SW  
S1705 N940 N941 Vread8 0 SW  
S1707 N941 N942 Vread8 0 SW  
S1709 N942 N943 Vread8 0 SW  
S1711 N943 N944 Vread8 0 SW  
S1586 Vp N881 Vwrite 0 SW  
S1588 Vp N882 Vwrite 0 SW  
S1590 Vp N883 Vwrite 0 SW  
S1592 Vp N884 Vwrite 0 SW  
S1594 Vp N885 Vwrite 0 SW  
S1596 Vp N886 Vwrite 0 SW  
S1598 Vp N887 Vwrite 0 SW  
S1600 Vp N888 Vwrite 0 SW  
S1602 Vp N889 Vwrite 0 SW  
S1604 Vp N890 Vwrite 0 SW  
S1606 Vp N891 Vwrite 0 SW  
S1608 Vp N892 Vwrite 0 SW  
S1610 Vp N893 Vwrite 0 SW  
S1612 Vp N894 Vwrite 0 SW  
S1614 Vp N895 Vwrite 0 SW  
S1616 Vp N896 Vwrite 0 SW  
S1618 Vp N897 Vwrite 0 SW  
S1620 Vp N898 Vwrite 0 SW  
S1622 Vp N899 Vwrite 0 SW  
S1624 Vp N900 Vwrite 0 SW  
S1626 Vn N901 Vwrite 0 SW  
S1628 Vp N902 Vwrite 0 SW  
S1630 Vp N903 Vwrite 0 SW  
S1632 Vp N904 Vwrite 0 SW  
S1634 Vp N905 Vwrite 0 SW  
S1636 Vp N906 Vwrite 0 SW  
S1638 Vn N907 Vwrite 0 SW  
S1640 Vn N908 Vwrite 0 SW  
S1642 Vn N909 Vwrite 0 SW  
S1644 Vn N910 Vwrite 0 SW  
S1646 Vn N911 Vwrite 0 SW  
S1648 Vp N912 Vwrite 0 SW  
S1650 Vp N913 Vwrite 0 SW  
S1652 Vp N914 Vwrite 0 SW  
S1654 Vn N915 Vwrite 0 SW  
S1656 Vp N916 Vwrite 0 SW  
S1658 Vp N917 Vwrite 0 SW  
S1660 Vp N918 Vwrite 0 SW  
S1662 Vp N919 Vwrite 0 SW  
S1664 Vp N920 Vwrite 0 SW  
S1666 Vp N921 Vwrite 0 SW  
S1668 Vn N922 Vwrite 0 SW  
S1670 Vn N923 Vwrite 0 SW  
S1672 Vp N924 Vwrite 0 SW  
S1674 Vp N925 Vwrite 0 SW  
S1676 Vp N926 Vwrite 0 SW  
S1678 Vn N927 Vwrite 0 SW  
S1680 Vn N928 Vwrite 0 SW  
S1682 Vp N929 Vwrite 0 SW  
S1684 Vp N930 Vwrite 0 SW  
S1686 Vn N931 Vwrite 0 SW  
S1688 Vp N932 Vwrite 0 SW  
S1690 Vp N933 Vwrite 0 SW  
S1692 Vp N934 Vwrite 0 SW  
S1694 Vn N935 Vwrite 0 SW  
S1696 Vp N936 Vwrite 0 SW  
S1698 Vp N937 Vwrite 0 SW  
S1700 Vp N938 Vwrite 0 SW  
S1702 Vn N939 Vwrite 0 SW  
S1704 Vn N940 Vwrite 0 SW  
S1706 Vn N941 Vwrite 0 SW  
S1708 Vn N942 Vwrite 0 SW  
S1710 Vn N943 Vwrite 0 SW  
S1712 Vp N944 Vwrite 0 SW  
S1713 0 N945 Vwrite 0 SW  
S1714 0 N946 Vwrite 0 SW  
S1715 0 N947 Vwrite 0 SW  
S1716 0 N948 Vwrite 0 SW  
S1717 0 N949 Vwrite 0 SW  
S1718 0 N950 Vwrite 0 SW  
S1719 0 N951 Vwrite 0 SW  
S1720 0 N952 Vwrite 0 SW  
XU793 N945 N881 MScammodel MScammodel  
XU794 N946 N882 MScammodel MScammodel

XU795	N947	N883	MScammodel	MScammodel
XU796	N948	N884	MScammodel	MScammodel
XU797	N949	N885	MScammodel	MScammodel
XU798	N950	N886	MScammodel	MScammodel
XU799	N951	N887	MScammodel	MScammodel
XU800	N952	N888	MScammodel	MScammodel
XU801	N945	N889	MScammodel	MScammodel
XU802	N946	N890	MScammodel	MScammodel
XU803	N947	N891	MScammodel	MScammodel
XU804	N948	N892	MScammodel	MScammodel
XU805	N949	N893	MScammodel	MScammodel
XU806	N950	N894	MScammodel	MScammodel
XU807	N951	N895	MScammodel	MScammodel
XU808	N952	N896	MScammodel	MScammodel
XU809	N945	N897	MScammodel	MScammodel
XU810	N946	N898	MScammodel	MScammodel
XU811	N947	N899	MScammodel	MScammodel
XU812	N948	N900	MScammodel	MScammodel
XU813	N949	N901	MScammodel	MScammodel
XU814	N950	N902	MScammodel	MScammodel
XU815	N951	N903	MScammodel	MScammodel
XU816	N952	N904	MScammodel	MScammodel
XU817	N945	N905	MScammodel	MScammodel
XU818	N946	N906	MScammodel	MScammodel
XU819	N947	N907	MScammodel	MScammodel
XU820	N948	N908	MScammodel	MScammodel
XU821	N949	N909	MScammodel	MScammodel
XU822	N950	N910	MScammodel	MScammodel
XU823	N951	N911	MScammodel	MScammodel
XU824	N952	N912	MScammodel	MScammodel
XU825	N945	N913	MScammodel	MScammodel
XU826	N946	N914	MScammodel	MScammodel
XU827	N947	N915	MScammodel	MScammodel
XU828	N948	N916	MScammodel	MScammodel
XU829	N949	N917	MScammodel	MScammodel
XU830	N950	N918	MScammodel	MScammodel
XU831	N951	N919	MScammodel	MScammodel
XU832	N952	N920	MScammodel	MScammodel
XU833	N945	N921	MScammodel	MScammodel
XU834	N946	N922	MScammodel	MScammodel
XU835	N947	N923	MScammodel	MScammodel
XU836	N948	N924	MScammodel	MScammodel
XU837	N949	N925	MScammodel	MScammodel
XU838	N950	N926	MScammodel	MScammodel
XU839	N951	N927	MScammodel	MScammodel
XU840	N952	N928	MScammodel	MScammodel
XU841	N945	N929	MScammodel	MScammodel
XU842	N946	N930	MScammodel	MScammodel
XU843	N947	N931	MScammodel	MScammodel
XU844	N948	N932	MScammodel	MScammodel
XU845	N949	N933	MScammodel	MScammodel
XU846	N950	N934	MScammodel	MScammodel
XU847	N951	N935	MScammodel	MScammodel
XU848	N952	N936	MScammodel	MScammodel
XU849	N945	N937	MScammodel	MScammodel
XU850	N946	N938	MScammodel	MScammodel
XU851	N947	N939	MScammodel	MScammodel
XU852	N948	N940	MScammodel	MScammodel
XU853	N949	N941	MScammodel	MScammodel
XU854	N950	N942	MScammodel	MScammodel
XU855	N951	N943	MScammodel	MScammodel
XU856	N952	N944	MScammodel	MScammodel
S1721	N945	N953	Vreadcol1	0 SW
S1722	N946	N954	Vreadcol2	0 SW
S1723	N947	N955	Vreadcol3	0 SW
S1724	N948	N956	Vreadcol4	0 SW
S1725	N949	N957	Vreadcol5	0 SW
S1726	N950	N958	Vreadcol6	0 SW
S1727	N951	N959	Vreadcol7	0 SW
S1728	N952	N960	Vreadcol8	0 SW
R89	N953	0	57k	
R90	N954	0	57k	
R91	N955	0	57k	
R92	N956	0	57k	
R93	N957	0	57k	
R94	N958	0	57k	
R95	N959	0	57k	
R96	N960	0	57k	
XU857	N953	Vrefcross	Vcccomp	Vnncomp Voutread121 ua741
XU858	N954	Vrefcross	Vcccomp	Vnncomp Voutread122 ua741
XU859	N955	Vrefcross	Vcccomp	Vnncomp Voutread123 ua741
XU860	N956	Vrefcross	Vcccomp	Vnncomp Voutread124 ua741
XU861	N957	Vrefcross	Vcccomp	Vnncomp Voutread125 ua741
XU862	N958	Vrefcross	Vcccomp	Vnncomp Voutread126 ua741

```
XU863 N959 Vrefcross Vcccomp Vnncomp Voutread127 ua741
XU864 N960 Vrefcross Vcccomp Vnncomp Voutread128 ua741
.tran 0 332u 10u uic
.backanno
.end
```

# Appendix E -SPICE netlist generation code (CAM array)

```
* This is a SPICE code generator for CAM
.model SW SW(Vt=0.5 Roff=1T)
.lib MS.sub
.include tsmc_model_250nm.txt
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.mos
.model NMOS NMOS

.options gmin=1e-9
.options abstol=1e-9
.options reltol=0.003
.options cshunt=1e-16

Vcc Vcc 0 1
Vp Vp 0 1
Vn Vn 0 -1
Vwritecam Vwritecam 0 PULSE(0 1 0 1n 1n 3u 10u 1)
Vreadcam Vreadcam 0 PULSE(0 1 10u 1n 1n 3u 10u 1)

C1 Cap1 0 100p IC=0.65
C2 Cap2 0 100p IC=0.65
C3 Cap3 0 100p IC=0.65
C4 Cap4 0 100p IC=0.65
C5 Cap5 0 100p IC=0.65
C6 Cap6 0 100p IC=0.65
C7 Cap7 0 100p IC=0.65
C8 Cap8 0 100p IC=0.65
S11 Cap1 Memin11 Vreadcam 0 SW
S14 Memin11 Memin12 Vreadcam 0 SW
S13 Memout11 0 Vwritecam 0 SW
S16 Memout12 0 Vwritecam 0 SW
XU11 Memin11 Memout11 MSmodel MSmodel
XU12 Memin12 Memout12 MSmodel MSmodel
S12 Memin11 Vn Vwritecam 0 SW
S15 Memin12 Vp Vwritecam 0 SW
M11 Memout11 0 0 0 CMOSN l=250n w=2500n
M12 Memout12 Vreadcam 0 0 CMOSN l=250n w=2500n
S17 Memin12 Memin13 Vreadcam 0 SW
S110 Memin13 Memin14 Vreadcam 0 SW
S19 Memout13 0 Vwritecam 0 SW
S112 Memout14 0 Vwritecam 0 SW
XU13 Memin13 Memout13 MSmodel MSmodel
XU14 Memin14 Memout14 MSmodel MSmodel
S18 Memin13 Vp Vwritecam 0 SW
S111 Memin14 Vn Vwritecam 0 SW
M13 Memout13 0 0 0 CMOSN l=250n w=2500n
M14 Memout14 Vreadcam 0 0 CMOSN l=250n w=2500n
S113 Memin14 Memin15 Vreadcam 0 SW
S116 Memin15 Memin16 Vreadcam 0 SW
S115 Memout15 0 Vwritecam 0 SW
S118 Memout16 0 Vwritecam 0 SW
XU15 Memin15 Memout15 MSmodel MSmodel
XU16 Memin16 Memout16 MSmodel MSmodel
S114 Memin15 Vn Vwritecam 0 SW
S117 Memin16 Vp Vwritecam 0 SW
M15 Memout15 0 0 0 CMOSN l=250n w=2500n
M16 Memout16 Vreadcam 0 0 CMOSN l=250n w=2500n
S119 Memin16 Memin17 Vreadcam 0 SW
S122 Memin17 Memin18 Vreadcam 0 SW
S121 Memout17 0 Vwritecam 0 SW
S124 Memout18 0 Vwritecam 0 SW
XU17 Memin17 Memout17 MSmodel MSmodel
XU18 Memin18 Memout18 MSmodel MSmodel
S120 Memin17 Vn Vwritecam 0 SW
S123 Memin18 Vp Vwritecam 0 SW
M17 Memout17 0 0 0 CMOSN l=250n w=2500n
M18 Memout18 Vreadcam 0 0 CMOSN l=250n w=2500n
S125 Memin18 Memin19 Vreadcam 0 SW
S128 Memin19 Memin110 Vreadcam 0 SW
S127 Memout19 0 Vwritecam 0 SW
S130 Memout110 0 Vwritecam 0 SW
XU19 Memin19 Memout19 MSmodel MSmodel
XU110 Memin110 Memout110 MSmodel MSmodel
S126 Memin19 Vn Vwritecam 0 SW
```

```

S129 Memin110 Vp Vwritecam 0 SW
M19 Memout19 0 0 0 CMOSN l=250n w=2500n
M110 Memout110 Vreadcam 0 0 CMOSN l=250n w=2500n
S131 Memin110 Memin111 Vreadcam 0 SW
S134 Memin111 Memin112 Vreadcam 0 SW
S133 Memout111 0 Vwritecam 0 SW
S136 Memout112 0 Vwritecam 0 SW
XU111 Memin111 Memout111 MSmodel MSmodel
XU112 Memin112 Memout112 MSmodel MSmodel
S132 Memin111 Vn Vwritecam 0 SW
S135 Memin112 Vp Vwritecam 0 SW
M111 Memout111 0 0 0 CMOSN l=250n w=2500n
M112 Memout112 Vreadcam 0 0 CMOSN l=250n w=2500n
S137 Memin112 Memin113 Vreadcam 0 SW
S140 Memin113 Memin114 Vreadcam 0 SW
S139 Memout113 0 Vwritecam 0 SW
S142 Memout114 0 Vwritecam 0 SW
XU113 Memin113 Memout113 MSmodel MSmodel
XU114 Memin114 Memout114 MSmodel MSmodel
S138 Memin113 Vn Vwritecam 0 SW
S141 Memin114 Vp Vwritecam 0 SW
M113 Memout113 0 0 0 CMOSN l=250n w=2500n
M114 Memout114 Vreadcam 0 0 CMOSN l=250n w=2500n
S143 Memin114 Memin115 Vreadcam 0 SW
S146 Memin115 Memin116 Vreadcam 0 SW
S145 Memout115 0 Vwritecam 0 SW
S148 Memout116 0 Vwritecam 0 SW
XU115 Memin115 Memout115 MSmodel MSmodel
XU116 Memin116 Memout116 MSmodel MSmodel
S144 Memin115 Vn Vwritecam 0 SW
S147 Memin116 Vp Vwritecam 0 SW
M115 Memout115 0 0 0 CMOSN l=250n w=2500n
M116 Memout116 Vreadcam 0 0 CMOSN l=250n w=2500n
S21 Cap2 Memin21 Vreadcam 0 SW
S24 Memin21 Memin22 Vreadcam 0 SW
S23 Memout21 0 Vwritecam 0 SW
S26 Memout22 0 Vwritecam 0 SW
XU21 Memin21 Memout21 MSmodel MSmodel
XU22 Memin22 Memout22 MSmodel MSmodel
S22 Memin21 Vn Vwritecam 0 SW
S25 Memin22 Vp Vwritecam 0 SW
M21 Memout21 0 0 0 CMOSN l=250n w=2500n
M22 Memout22 Vreadcam 0 0 CMOSN l=250n w=2500n
S27 Memin22 Memin23 Vreadcam 0 SW
S210 Memin23 Memin24 Vreadcam 0 SW
S29 Memout23 0 Vwritecam 0 SW
S212 Memout24 0 Vwritecam 0 SW
XU23 Memin23 Memout23 MSmodel MSmodel
XU24 Memin24 Memout24 MSmodel MSmodel
S28 Memin23 Vn Vwritecam 0 SW
S211 Memin24 Vp Vwritecam 0 SW
M23 Memout23 0 0 0 CMOSN l=250n w=2500n
M24 Memout24 Vreadcam 0 0 CMOSN l=250n w=2500n
S213 Memin24 Memin25 Vreadcam 0 SW
S216 Memin25 Memin26 Vreadcam 0 SW
S215 Memout25 0 Vwritecam 0 SW
S218 Memout26 0 Vwritecam 0 SW
XU25 Memin25 Memout25 MSmodel MSmodel
XU26 Memin26 Memout26 MSmodel MSmodel
S214 Memin25 Vn Vwritecam 0 SW
S217 Memin26 Vp Vwritecam 0 SW
M25 Memout25 0 0 0 CMOSN l=250n w=2500n
M26 Memout26 Vreadcam 0 0 CMOSN l=250n w=2500n
S219 Memin26 Memin27 Vreadcam 0 SW
S222 Memin27 Memin28 Vreadcam 0 SW
S221 Memout27 0 Vwritecam 0 SW
S224 Memout28 0 Vwritecam 0 SW
XU27 Memin27 Memout27 MSmodel MSmodel
XU28 Memin28 Memout28 MSmodel MSmodel
S220 Memin27 Vn Vwritecam 0 SW
S223 Memin28 Vp Vwritecam 0 SW
M27 Memout27 0 0 0 CMOSN l=250n w=2500n
M28 Memout28 Vreadcam 0 0 CMOSN l=250n w=2500n
S225 Memin28 Memin29 Vreadcam 0 SW
S228 Memin29 Memin210 Vreadcam 0 SW
S227 Memout29 0 Vwritecam 0 SW
S230 Memout210 0 Vwritecam 0 SW
XU29 Memin29 Memout29 MSmodel MSmodel
XU210 Memin210 Memout210 MSmodel MSmodel
S226 Memin29 Vn Vwritecam 0 SW
S229 Memin210 Vp Vwritecam 0 SW
M29 Memout29 0 0 0 CMOSN l=250n w=2500n
M210 Memout210 Vreadcam 0 0 CMOSN l=250n w=2500n
S231 Memin210 Memin211 Vreadcam 0 SW

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S234 Memin211 Memin212 Vreadcam 0 SW  
S233 Memout211 0 Vwritecam 0 SW  
S236 Memout212 0 Vwritecam 0 SW  
XU211 Memin211 Memout211 MSmodel MSmodel  
XU212 Memin212 Memout212 MSmodel MSmodel  
S232 Memin211 Vn Vwritecam 0 SW  
S235 Memin212 Vp Vwritecam 0 SW  
M211 Memout211 0 0 0 CMOSN l=250n w=2500n  
M212 Memout212 Vreadcam 0 0 CMOSN l=250n w=2500n  
S237 Memin212 Memin213 Vreadcam 0 SW  
S240 Memin213 Memin214 Vreadcam 0 SW  
S239 Memout213 0 Vwritecam 0 SW  
S242 Memout214 0 Vwritecam 0 SW  
XU213 Memin213 Memout213 MSmodel MSmodel  
XU214 Memin214 Memout214 MSmodel MSmodel  
S238 Memin213 Vn Vwritecam 0 SW  
S241 Memin214 Vp Vwritecam 0 SW  
M213 Memout213 0 0 0 CMOSN l=250n w=2500n  
M214 Memout214 Vreadcam 0 0 CMOSN l=250n w=2500n  
S243 Memin214 Memin215 Vreadcam 0 SW  
S246 Memin215 Memin216 Vreadcam 0 SW  
S245 Memout215 0 Vwritecam 0 SW  
S248 Memout216 0 Vwritecam 0 SW  
XU215 Memin215 Memout215 MSmodel MSmodel  
XU216 Memin216 Memout216 MSmodel MSmodel  
S244 Memin215 Vn Vwritecam 0 SW  
S247 Memin216 Vp Vwritecam 0 SW  
M215 Memout215 0 0 0 CMOSN l=250n w=2500n  
M216 Memout216 Vreadcam 0 0 CMOSN l=250n w=2500n  
S31 Cap3 Memin31 Vreadcam 0 SW  
S34 Memin31 Memin32 Vreadcam 0 SW  
S33 Memout31 0 Vwritecam 0 SW  
S36 Memout32 0 Vwritecam 0 SW  
XU31 Memin31 Memout31 MSmodel MSmodel  
XU32 Memin32 Memout32 MSmodel MSmodel  
S32 Memin31 Vn Vwritecam 0 SW  
S35 Memin32 Vp Vwritecam 0 SW  
M31 Memout31 Vreadcam 0 0 CMOSN l=250n w=2500n  
M32 Memout32 0 0 0 CMOSN l=250n w=2500n  
S37 Memin32 Memin33 Vreadcam 0 SW  
S310 Memin33 Memin34 Vreadcam 0 SW  
S39 Memout33 0 Vwritecam 0 SW  
S312 Memout34 0 Vwritecam 0 SW  
XU33 Memin33 Memout33 MSmodel MSmodel  
XU34 Memin34 Memout34 MSmodel MSmodel  
S38 Memin33 Vn Vwritecam 0 SW  
S311 Memin34 Vp Vwritecam 0 SW  
M33 Memout33 0 0 0 CMOSN l=250n w=2500n  
M34 Memout34 Vreadcam 0 0 CMOSN l=250n w=2500n  
S313 Memin34 Memin35 Vreadcam 0 SW  
S316 Memin35 Memin36 Vreadcam 0 SW  
S315 Memout35 0 Vwritecam 0 SW  
S318 Memout36 0 Vwritecam 0 SW  
XU35 Memin35 Memout35 MSmodel MSmodel  
XU36 Memin36 Memout36 MSmodel MSmodel  
S314 Memin35 Vn Vwritecam 0 SW  
S317 Memin36 Vp Vwritecam 0 SW  
M35 Memout35 0 0 0 CMOSN l=250n w=2500n  
M36 Memout36 Vreadcam 0 0 CMOSN l=250n w=2500n  
S319 Memin36 Memin37 Vreadcam 0 SW  
S322 Memin37 Memin38 Vreadcam 0 SW  
S321 Memout37 0 Vwritecam 0 SW  
S324 Memout38 0 Vwritecam 0 SW  
XU37 Memin37 Memout37 MSmodel MSmodel  
XU38 Memin38 Memout38 MSmodel MSmodel  
S320 Memin37 Vn Vwritecam 0 SW  
S323 Memin38 Vp Vwritecam 0 SW  
M37 Memout37 0 0 0 CMOSN l=250n w=2500n  
M38 Memout38 Vreadcam 0 0 CMOSN l=250n w=2500n  
S325 Memin38 Memin39 Vreadcam 0 SW  
S328 Memin39 Memin310 Vreadcam 0 SW  
S327 Memout39 0 Vwritecam 0 SW  
S330 Memout310 0 Vwritecam 0 SW  
XU39 Memin39 Memout39 MSmodel MSmodel  
XU310 Memin310 Memout310 MSmodel MSmodel  
S326 Memin39 Vn Vwritecam 0 SW  
S329 Memin310 Vp Vwritecam 0 SW  
M39 Memout39 0 0 0 CMOSN l=250n w=2500n  
M310 Memout310 Vreadcam 0 0 CMOSN l=250n w=2500n  
S331 Memin310 Memin311 Vreadcam 0 SW  
S334 Memin311 Memin312 Vreadcam 0 SW  
S333 Memout311 0 Vwritecam 0 SW  
S336 Memout312 0 Vwritecam 0 SW  
XU311 Memin311 Memout311 MSmodel MSmodel

XU312 Memin312 Memout312 MSmodel MSmodel  
S332 Memin311 Vn Vwritecam 0 SW  
S335 Memin312 Vp Vwritecam 0 SW  
M311 Memout311 0 0 0 CMOSN l=250n w=2500n  
M312 Memout312 Vreadcam 0 0 CMOSN l=250n w=2500n  
S337 Memin312 Memin313 Vreadcam 0 SW  
S340 Memin313 Memin314 Vreadcam 0 SW  
S339 Memout313 0 Vwritecam 0 SW  
S342 Memout314 0 Vwritecam 0 SW  
XU313 Memin313 Memout313 MSmodel MSmodel  
XU314 Memin314 Memout314 MSmodel MSmodel  
S338 Memin313 Vp Vwritecam 0 SW  
S341 Memin314 Vn Vwritecam 0 SW  
M313 Memout313 0 0 0 CMOSN l=250n w=2500n  
M314 Memout314 Vreadcam 0 0 CMOSN l=250n w=2500n  
S343 Memin314 Memin315 Vreadcam 0 SW  
S346 Memin315 Memin316 Vreadcam 0 SW  
S345 Memout315 0 Vwritecam 0 SW  
S348 Memout316 0 Vwritecam 0 SW  
XU315 Memin315 Memout315 MSmodel MSmodel  
XU316 Memin316 Memout316 MSmodel MSmodel  
S344 Memin315 Vn Vwritecam 0 SW  
S347 Memin316 Vp Vwritecam 0 SW  
M315 Memout315 0 0 0 CMOSN l=250n w=2500n  
M316 Memout316 Vreadcam 0 0 CMOSN l=250n w=2500n  
S41 Cap4 Memin41 Vreadcam 0 SW  
S44 Memin41 Memin42 Vreadcam 0 SW  
S43 Memout41 0 Vwritecam 0 SW  
S46 Memout42 0 Vwritecam 0 SW  
XU41 Memin41 Memout41 MSmodel MSmodel  
XU42 Memin42 Memout42 MSmodel MSmodel  
S42 Memin41 Vn Vwritecam 0 SW  
S45 Memin42 Vp Vwritecam 0 SW  
M41 Memout41 0 0 0 CMOSN l=250n w=2500n  
M42 Memout42 Vreadcam 0 0 CMOSN l=250n w=2500n  
S47 Memin42 Memin43 Vreadcam 0 SW  
S410 Memin43 Memin44 Vreadcam 0 SW  
S49 Memout43 0 Vwritecam 0 SW  
S412 Memout44 0 Vwritecam 0 SW  
XU43 Memin43 Memout43 MSmodel MSmodel  
XU44 Memin44 Memout44 MSmodel MSmodel  
S48 Memin43 Vn Vwritecam 0 SW  
S411 Memin44 Vp Vwritecam 0 SW  
M43 Memout43 0 0 0 CMOSN l=250n w=2500n  
M44 Memout44 Vreadcam 0 0 CMOSN l=250n w=2500n  
S413 Memin44 Memin45 Vreadcam 0 SW  
S416 Memin45 Memin46 Vreadcam 0 SW  
S415 Memout45 0 Vwritecam 0 SW  
S418 Memout46 0 Vwritecam 0 SW  
XU45 Memin45 Memout45 MSmodel MSmodel  
XU46 Memin46 Memout46 MSmodel MSmodel  
S414 Memin45 Vp Vwritecam 0 SW  
S417 Memin46 Vn Vwritecam 0 SW  
M45 Memout45 0 0 0 CMOSN l=250n w=2500n  
M46 Memout46 Vreadcam 0 0 CMOSN l=250n w=2500n  
S419 Memin46 Memin47 Vreadcam 0 SW  
S422 Memin47 Memin48 Vreadcam 0 SW  
S421 Memout47 0 Vwritecam 0 SW  
S424 Memout48 0 Vwritecam 0 SW  
XU47 Memin47 Memout47 MSmodel MSmodel  
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S428 Memin49 Memin410 Vreadcam 0 SW  
S427 Memout49 0 Vwritecam 0 SW  
S430 Memout410 0 Vwritecam 0 SW  
XU49 Memin49 Memout49 MSmodel MSmodel  
XU410 Memin410 Memout410 MSmodel MSmodel  
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S429 Memin410 Vn Vwritecam 0 SW  
M49 Memout49 Vreadcam 0 0 CMOSN l=250n w=2500n  
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S434 Memin411 Memin412 Vreadcam 0 SW  
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S436 Memout412 0 Vwritecam 0 SW  
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XU412 Memin412 Memout412 MSmodel MSmodel  
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M412 Memout412 0 0 0 CMOSN l=250n w=2500n  
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S440 Memin413 Memin414 Vreadcam 0 SW  
S439 Memout413 0 Vwritecam 0 SW  
S442 Memout414 0 Vwritecam 0 SW  
XU413 Memin413 Memout413 MSmodel MSmodel  
XU414 Memin414 Memout414 MSmodel MSmodel  
S438 Memin413 Vp Vwritecam 0 SW  
S441 Memin414 Vn Vwritecam 0 SW  
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S448 Memout416 0 Vwritecam 0 SW  
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XU416 Memin416 Memout416 MSmodel MSmodel  
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S447 Memin416 Vn Vwritecam 0 SW  
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S56 Memout52 0 Vwritecam 0 SW  
XU51 Memin51 Memout51 MSmodel MSmodel  
XU52 Memin52 Memout52 MSmodel MSmodel  
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S55 Memin52 Vp Vwritecam 0 SW  
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XU53 Memin53 Memout53 MSmodel MSmodel  
XU54 Memin54 Memout54 MSmodel MSmodel  
S58 Memin53 Vn Vwritecam 0 SW  
S511 Memin54 Vp Vwritecam 0 SW  
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S518 Memout56 0 Vwritecam 0 SW  
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XU56 Memin56 Memout56 MSmodel MSmodel  
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XU58 Memin58 Memout58 MSmodel MSmodel  
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S530 Memout510 0 Vwritecam 0 SW  
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XU514 Memin514 Memout514 MSmodel MSmodel  
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S548 Memout516 0 Vwritecam 0 SW  
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XU516 Memin516 Memout516 MSmodel MSmodel  
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S547 Memin516 Vn Vwritecam 0 SW  
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M516 Memout516 Vreadcam 0 0 CMOSN l=250n w=2500n  
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S66 Memout62 0 Vwritecam 0 SW  
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XU62 Memin62 Memout62 MSmodel MSmodel  
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S612 Memout64 0 Vwritecam 0 SW  
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S611 Memin64 Vp Vwritecam 0 SW  
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S618 Memout66 0 Vwritecam 0 SW  
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XU66 Memin66 Memout66 MSmodel MSmodel  
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S617 Memin66 Vp Vwritecam 0 SW  
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S622 Memin67 Memin68 Vreadcam 0 SW  
S621 Memout67 0 Vwritecam 0 SW  
S624 Memout68 0 Vwritecam 0 SW  
XU67 Memin67 Memout67 MSmodel MSmodel  
XU68 Memin68 Memout68 MSmodel MSmodel  
S620 Memin67 Vn Vwritecam 0 SW  
S623 Memin68 Vp Vwritecam 0 SW  
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S630 Memout610 0 Vwritecam 0 SW  
XU69 Memin69 Memout69 MSmodel MSmodel  
XU610 Memin610 Memout610 MSmodel MSmodel  
S626 Memin69 Vp Vwritecam 0 SW  
S629 Memin610 Vn Vwritecam 0 SW  
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XU611 Memin611 Memout611 MSmodel MSmodel  
XU612 Memin612 Memout612 MSmodel MSmodel  
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S635 Memin612 Vn Vwritecam 0 SW  
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S640 Memin613 Memin614 Vreadcam 0 SW  
S639 Memout613 0 Vwritecam 0 SW  
S642 Memout614 0 Vwritecam 0 SW  
XU613 Memin613 Memout613 MSmodel MSmodel  
XU614 Memin614 Memout614 MSmodel MSmodel  
S638 Memin613 Vp Vwritecam 0 SW

S641 Memin614 Vn Vwritecam 0 SW  
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S648 Memout616 0 Vwritecam 0 SW  
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XU616 Memin616 Memout616 MSmodel MSmodel  
S644 Memin615 Vn Vwritecam 0 SW  
S647 Memin616 Vp Vwritecam 0 SW  
M615 Memout615 0 0 0 CMOSN l=250n w=2500n  
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S74 Memin71 Memin72 Vreadcam 0 SW  
S73 Memout71 0 Vwritecam 0 SW  
S76 Memout72 0 Vwritecam 0 SW  
XU71 Memin71 Memout71 MSmodel MSmodel  
XU72 Memin72 Memout72 MSmodel MSmodel  
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S75 Memin72 Vp Vwritecam 0 SW  
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S77 Memin72 Memin73 Vreadcam 0 SW  
S710 Memin73 Memin74 Vreadcam 0 SW  
S79 Memout73 0 Vwritecam 0 SW  
S712 Memout74 0 Vwritecam 0 SW  
XU73 Memin73 Memout73 MSmodel MSmodel  
XU74 Memin74 Memout74 MSmodel MSmodel  
S78 Memin73 Vn Vwritecam 0 SW  
S711 Memin74 Vp Vwritecam 0 SW  
M73 Memout73 0 0 0 CMOSN l=250n w=2500n  
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S713 Memin74 Memin75 Vreadcam 0 SW  
S716 Memin75 Memin76 Vreadcam 0 SW  
S715 Memout75 0 Vwritecam 0 SW  
S718 Memout76 0 Vwritecam 0 SW  
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XU76 Memin76 Memout76 MSmodel MSmodel  
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S717 Memin76 Vp Vwritecam 0 SW  
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S719 Memin76 Memin77 Vreadcam 0 SW  
S722 Memin77 Memin78 Vreadcam 0 SW  
S721 Memout77 0 Vwritecam 0 SW  
S724 Memout78 0 Vwritecam 0 SW  
XU77 Memin77 Memout77 MSmodel MSmodel  
XU78 Memin78 Memout78 MSmodel MSmodel  
S720 Memin77 Vn Vwritecam 0 SW  
S723 Memin78 Vp Vwritecam 0 SW  
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S728 Memin79 Memin710 Vreadcam 0 SW  
S727 Memout79 0 Vwritecam 0 SW  
S730 Memout710 0 Vwritecam 0 SW  
XU79 Memin79 Memout79 MSmodel MSmodel  
XU710 Memin710 Memout710 MSmodel MSmodel  
S726 Memin79 Vn Vwritecam 0 SW  
S729 Memin710 Vp Vwritecam 0 SW  
M79 Memout79 Vreadcam 0 0 CMOSN l=250n w=2500n  
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S731 Memin710 Memin711 Vreadcam 0 SW  
S734 Memin711 Memin712 Vreadcam 0 SW  
S733 Memout711 0 Vwritecam 0 SW  
S736 Memout712 0 Vwritecam 0 SW  
XU711 Memin711 Memout711 MSmodel MSmodel  
XU712 Memin712 Memout712 MSmodel MSmodel  
S732 Memin711 Vn Vwritecam 0 SW  
S735 Memin712 Vp Vwritecam 0 SW  
M711 Memout711 Vreadcam 0 0 CMOSN l=250n w=2500n  
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S737 Memin712 Memin713 Vreadcam 0 SW  
S740 Memin713 Memin714 Vreadcam 0 SW  
S739 Memout713 0 Vwritecam 0 SW  
S742 Memout714 0 Vwritecam 0 SW  
XU713 Memin713 Memout713 MSmodel MSmodel  
XU714 Memin714 Memout714 MSmodel MSmodel  
S738 Memin713 Vn Vwritecam 0 SW  
S741 Memin714 Vp Vwritecam 0 SW  
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S743 Memin714 Memin715 Vreadcam 0 SW

S746 Memin715 Memin716 Vreadcam 0 SW  
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S748 Memout716 0 Vwritecam 0 SW  
XU715 Memin715 Memout715 MSmodel MSmodel  
XU716 Memin716 Memout716 MSmodel MSmodel  
S744 Memin715 Vn Vwritecam 0 SW  
S747 Memin716 Vp Vwritecam 0 SW  
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M716 Memout716 Vreadcam 0 0 CMOSN l=250n w=2500n  
S81 Cap8 Memin81 Vreadcam 0 SW  
S84 Memin81 Memin82 Vreadcam 0 SW  
S83 Memout81 0 Vwritecam 0 SW  
S86 Memout82 0 Vwritecam 0 SW  
XU81 Memin81 Memout81 MSmodel MSmodel  
XU82 Memin82 Memout82 MSmodel MSmodel  
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S85 Memin82 Vp Vwritecam 0 SW  
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S89 Memout83 0 Vwritecam 0 SW  
S812 Memout84 0 Vwritecam 0 SW  
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XU84 Memin84 Memout84 MSmodel MSmodel  
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S811 Memin84 Vp Vwritecam 0 SW  
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S816 Memin85 Memin86 Vreadcam 0 SW  
S815 Memout85 0 Vwritecam 0 SW  
S818 Memout86 0 Vwritecam 0 SW  
XU85 Memin85 Memout85 MSmodel MSmodel  
XU86 Memin86 Memout86 MSmodel MSmodel  
S814 Memin85 Vn Vwritecam 0 SW  
S817 Memin86 Vp Vwritecam 0 SW  
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M86 Memout86 Vreadcam 0 0 CMOSN l=250n w=2500n  
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S822 Memin87 Memin88 Vreadcam 0 SW  
S821 Memout87 0 Vwritecam 0 SW  
S824 Memout88 0 Vwritecam 0 SW  
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S823 Memin88 Vp Vwritecam 0 SW  
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S828 Memin89 Memin810 Vreadcam 0 SW  
S827 Memout89 0 Vwritecam 0 SW  
S830 Memout810 0 Vwritecam 0 SW  
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XU810 Memin810 Memout810 MSmodel MSmodel  
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S836 Memout812 0 Vwritecam 0 SW  
XU811 Memin811 Memout811 MSmodel MSmodel  
XU812 Memin812 Memout812 MSmodel MSmodel  
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S835 Memin812 Vp Vwritecam 0 SW  
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M812 Memout812 0 0 CMOSN l=250n w=2500n  
S837 Memin812 Memin813 Vreadcam 0 SW  
S840 Memin813 Memin814 Vreadcam 0 SW  
S839 Memout813 0 Vwritecam 0 SW  
S842 Memout814 0 Vwritecam 0 SW  
XU813 Memin813 Memout813 MSmodel MSmodel  
XU814 Memin814 Memout814 MSmodel MSmodel  
S838 Memin813 Vn Vwritecam 0 SW  
S841 Memin814 Vp Vwritecam 0 SW  
M813 Memout813 0 0 CMOSN l=250n w=2500n  
M814 Memout814 Vreadcam 0 0 CMOSN l=250n w=2500n  
S843 Memin814 Memin815 Vreadcam 0 SW  
S846 Memin815 Memin816 Vreadcam 0 SW  
S845 Memout815 0 Vwritecam 0 SW  
S848 Memout816 0 Vwritecam 0 SW  
XU815 Memin815 Memout815 MSmodel MSmodel

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XU816 Memin816 Memout816 MSmodel MSmodel
S844 Memin815 Vn Vwritecam 0 SW
S847 Memin816 Vp Vwritecam 0 SW
M815 Memout815 0 0 0 CMOSN l=250n w=2500n
M816 Memout816 Vreadcam 0 0 CMOSN l=250n w=2500n
.tran 0 10.1u 10u uic
.backanno
.end
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