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30 Gb/s integrated receiver array for parallel optical interconnects

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Abstract: A 30 Gb/s integrated receiver array for parallel optical interconnects with four channels have been designed and implemented in a 0.13 µm CMOS technology. To achieve small area and low power consumption while maintaining large bandwidth and high gain, the integrated receiver has been implemented with a regulated cascode (RGC) transimpedance amplifier (TIA), resistive and capacitive degeneration and inductorless limiting amplifier (LA), which employs active feedback and negative capacitance. From the measurement results of the optical module using 850 nm photodiode (PD), the receiver showed a constant single-ended output swing of 320 mV up to 7.5 Gb/s/ch with clear eye diagrams and BER of $<10^{-12}$. With a voltage supply of 1.2 V, a figure of merit (FOM) of 8 mW/Gb/s was obtained with a small chip area per channel of 0.28 mm^2/ch.

1 Introduction

With the trend of reducing power consumption and increasing the density of the interconnection, parallel optical interconnects recently have been considered as good replacements for the electrical counterparts in high-performance computing systems, which have limitation in the terms of link capacity and physical quantity [1]. In an optical interconnect, the receiver is a key component affecting the whole system performance in terms of speed, noise, sensitivity, and power consumption. Several achievements at high data rate operation (gigabit) have been obtained using III-V materials and technologies such as InP, HEMT, GaAs, and Bi-CMOS [2, 3]. However, the drawbacks of the III-V material based chips are high power consumption and difficulty in integrating with other system chips based on CMOS technology. The only candidate that can satisfy the integration requirements with reasonable high speed, low cost, and high yield is CMOS technology.

Recently, many efforts have been made on the CMOS optical receiver design for high-speed optical interconnects. These achievements were based on small scale of CMOS technologies which are very expensive [4] or utilised a passive inductor peaking technique which consumes very large chip area or employed an active inductor peaking technique which needs high power supply voltage [5–8]. This work presents the design of a 30 Gb/s optical integrated receiver array in a 0.13 µm CMOS technology. In order to ensure low power consumption and small size, the receiver employs an RGC TIA with resistance and capacitance degeneration and an inductorless LA with active feedback, respectively, with negative capacitance to broaden the bandwidth. The receiver also employs inductorless TIA [6] and negative impedance compensation for low power and low voltage LA [9].

2 Circuit design of the integrated receiver array

An integrated receiver consists of a TIA which receives a noisy small current signal from PD, an LA to amplify the small voltage signal from TIA and output buffer to connect the receiver with 50 ohm load. Fig. 1 shows the TIA circuit and its small signal schematic.

3 TIA design

The TIA is designed with the RGC implemented in the input stage to ensure a small input resistance for isolating the high parasitic capacitance from PD from the receiver [10]. The RGC topology has a well-defined small input impedance which could be derived from the small-signal circuit model in Fig. 1*b* and the input resistor is given by (1).

$$r_i = \frac{1}{g_{m1}(1 + g_{m2}R_2)} \tag{1}$$

To achieve higher bandwidth, many works have been done by using passive inductor peaking or passive L-C for input matching network which have large chip area [7, 8]. In our design, after RGC input stage, a gain stage with resistance and capacitance degeneration has been employed to push the dominant pole to higher frequency for broadening the 3-dB bandwidth while keeping the chip size small. From Figs. 1*b* and *c*, the transimpedance of the TIA (Z_T) can be derived as in (2).

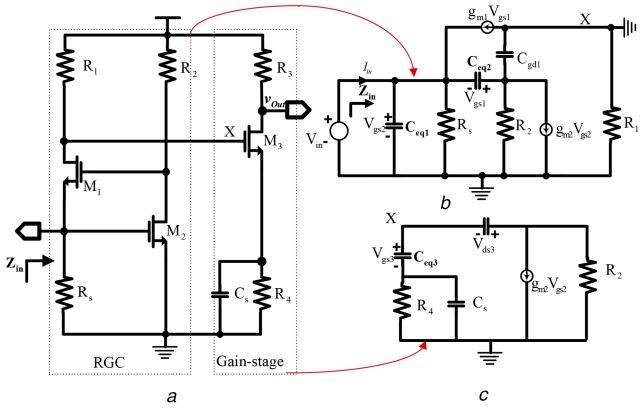


Fig. 1 *Illustration showing*
(a) TIA schematic and ***(b)***, ***(c)*** Its small signal

$$Z_T = \frac{V_{\text{out}}}{I_{\text{in}}} = R_1 \frac{1 + sC_{\text{eq2}}}{\left[1 + \left((sC_{\text{eq1}})/(1 + g_{m2}R_2)g_{m1}\right)\right]\left[1 + sR_2(C_{\text{eq3}} + C_{\text{eq2}})\right]} \times \frac{g_{m3}R_3}{1 + g_{m3}R_5} \times \frac{1 + sR_4C_s}{1 + s(R_4C_s/g_{m3}R_4)} \tag{2}$$

where $C_{\text{eq1}} = C_{\text{sb1}} + C_{\text{gs2}}$, $C_{\text{eq2}} = C_{\text{gs1}} + C_{\text{gd2}}$ and $C_{\text{eq3}} = C_{\text{gs3}} + C_{\text{gd1}}$. It can be derived from the (2) that, the TIA has 2 poles and 1 zero from RGC input stage; a zero at $(1/R_4C_s)$ and a pole at $(1 + g_{m3}R_4)/R_4C_s$ from the degeneration gain stage. With suitable value of R_4, C_s, and g_{m3}, the zero from gain stage can be used for compensating the dominant pole of the amplifier and the 3-dB frequency is, therefore, determined by the second lowest pole of the circuit $1/(R_2(C_{\text{eq3}} + C_{\text{eq2}}))$. On the other hand, the capacitor degeneration works as a filter for the gain stage to enhance the noise performance of the TIA. Fig. 2 shows the frequency response of the TIA with variations of the degeneration capacitor C_s at 250, 450, and 750 fF. Based on the obtained value, an optimal degeneration capacitance of 450 fF was used in our design for peaking the bandwidth of the TIA with the gain peaking of 2.5 dB at 5.8 GHz. The designed TIA achieved a gain of 51 dBΩ.

4 Limiting amplifier design

To provide enough gain and large output voltage swing, LA comprising of three gain cells has been employed. The number of gain cell was considered to optimise the trade-off among gain, input-referred noise, power consumption, and bandwidth. In each gain cell, the techniques to enhance the bandwidth as well as to reduce the power consumption and increase signal quality were employed. Fig. 3 shows the schematic of a gain cell. To enhance the bandwidth, traditionally, inductive peaking technique is used. Passive inductors occupy much chip area so active inductor is as a solution for this [7, 8]. The active inductor cannot apply in a low supply voltage due to voltage headroom problem [10]. Additionally, inductor peaking both active and passive leads to non-fineness gain-frequency response causing the peaking transient signal and large jitter. In this work, a negative active third-order feedback through differential transistor pair (M_{f}, M_{f}) was used to broaden the bandwidth of the gain cells and subsequently, for the LA. However, the active feedback through transistor pair gives intermediate nodes which exhibit three active devices (M_1, M_{f}, M_5) high impedance. This high impedance can cause the amplifier unstable. In order to compensate this high parasitic capacitance impedance, a negative capacitance stage has been used. The negative capacitances Z_c can be derived as in (3):

$$\begin{aligned} Z_c &= -\frac{1}{sC} \times \frac{g_{m_c} + s\left(C_{\text{gsm}_c} + 2C\right)}{g_{m_c} - sC_{\text{gsm}_c}} \\ &= -\frac{1}{sC} \times \frac{g_{m_c} + s\left(C_{\text{gsm}_c} + 2C\right)}{g_{m_c}} \\ &= -\frac{1}{sC} - \frac{(C_{\text{gsm}_c}/C) + 2}{g_{m_c}} \end{aligned} \tag{3}$$

From (4), Z_c is equivalent to a negative capacitor of $-C$ in series with a $-(((C_{\text{gsm}_c}/C) + 2)/g_{m_c})$ negative resistor. In order to compensate the high parasitic capacitance impedance caused by the active feedback resistor pairs, a negative capacitance stage has been used. This negative capacitor can compensate high parasitic impedance at X, Y and ensures the phase margin of the LA stay at the optimised point of 60°.

On the other hand, the negative capacitance also plays a role of slew-rate boosting by sharing a portion of current for the feedback circuit to remove the low-setting of the output waveform at the nodes X and Y. By carefully simulating the value of R_1, C, the size of M_c, the bandwidth as well as the stability of the gain stage can be improved. The voltage gain A_v of the LA stage can be expressed in (4)

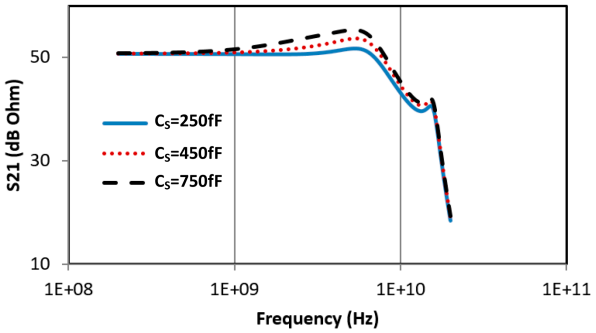


Fig. 2 *Simulated S21with different capacitor degenerations*

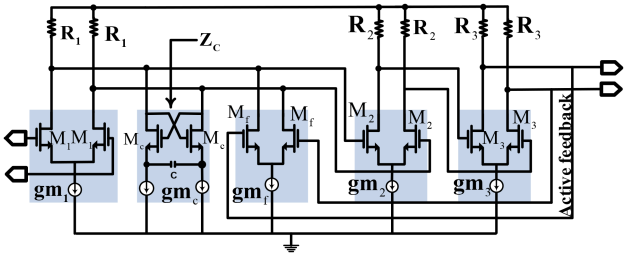


Fig. 3 *Schematics of an LA gain cell*

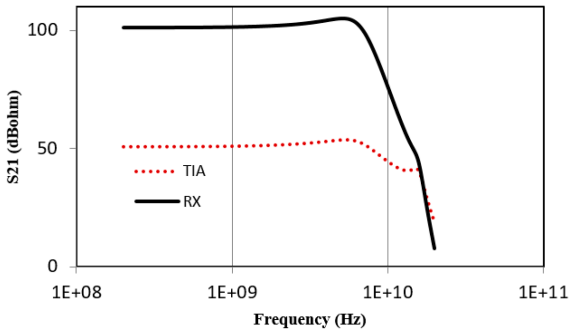


Fig. 4 *Simulated freq. response of TIA and integrated receiver*

$$\begin{aligned} A_v &= \frac{V_{\text{out}}}{V_{\text{in}}} \\ &= -\frac{g_{m1}R_1\left[1 + s\left((C_{\text{gsc}} + 2C)/g_{m3}\right)\right]}{1 + \left[\left((C_{\text{gsc}} + 2C)/g_{m3}\right) + R_1C\right]s + R_1\left((C_{\text{gs3}} + 2C)/g_{m3}\right)s^2} \\ &\quad \times \frac{G_2(s)G_3(s)}{1 + G_2(s)G_3(s)G_f(s)} \end{aligned} \tag{4}$$

Fig. 4 shows the simulated frequency response of the TIA and integrated receiver. The TIA achieved a gain of 51 dBΩ, while the integrated receiver achieved a gain of 101 dBΩ per channel.

5 Experimental results

The integrated receiver was designed and fabricated in a 0.13 µm CMOS technology with eight metal layers. Including the ESD pads, the chip occupied a total area of 1.07 mm × 1.75 mm. Fig. 5 shows the photograph of the receiver chip and its packaging. The receiver was die-bonded on a Teflon-printed circuit board (PCB) and wire-bonded to an 850 nm GaAs PD.

For measurement purposes, a commercial 10 Gb/s/ch transmitter module (TX) was used to generate optical signal, which was aligned to the PD of the receiver array. The measurements of the receiver were done based on the following system: electrical signal generators→commercial optical TX→designed optical RX array→electrical output signal→measurement instruments as shown in Fig. 6.

To obtain the transient response of the receiver array, a $2^{31} - 1$ pseudorandom binary sequence input signal, generated from an Anritsu MP1763B pulse-pattern generator, was applied; while the

Fig. 5 *Photograph of*
(a) The 4-ch receiver and ***(b)***, ***(c)*** Its packaging

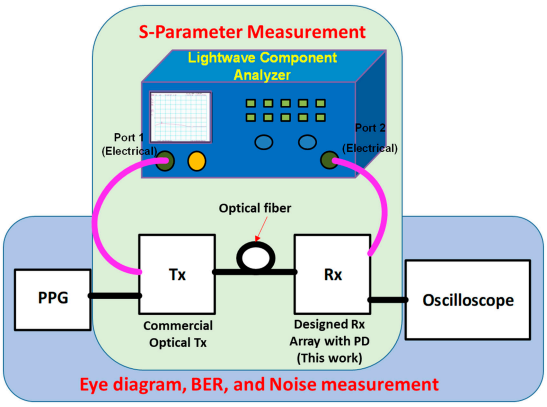


Fig. 6 *Experimental measurement setup*

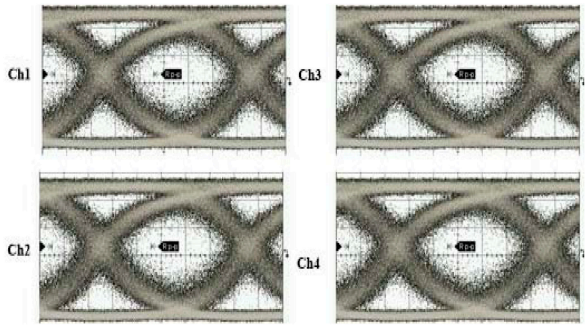


Fig. 7 *Measured eye diagrams of the output at 7.5 Gb/s/ch*

output signal was measured by using an Agilent 86,100 A oscilloscope. Fig. 7 shows the dynamic response measurement results of the receiver array at 7.5 Gb/s/ch. The receiver gives a differential output with constant voltage swing on single-ended output of 320 mVp. Agilent 8703 B lightwave component analyser was used to measure the S-parameters (S21) of the receiver. As shown in Fig. 8, the receiver achieved a measured 3-dB bandwidth of 5.5 GHz. When compared with the simulated results, the lower bandwidth of the measured result could be due to impedance mismatch between PD and RX and also process variation of both the RX chip and evaluation board. The results can be improved by including the PD model, wired bonding effects, evaluation board effects in the design stage. To measure the BER of the receiver versus input optical power, a fixed multimode attenuator was used.

The maximum power needed for BER of $<10^{-12}$ is about −7.5 dBm as can be seen in Fig. 9*a*. The BER perfomances for the four channels showed uniformity within 0.8 dB. The output referred noise was measured by disabling the input signal and using histogram function of the oscilloscope to get the output referred noise. The standard deviation of the output referred noise which includes the base noise of the oscilloscope is 2.4 mV. If the equivalent input referred current noise is independent of the frequency, then from [11], the measured input referred noise of a typical channel is calculated and plotted as shown in Fig. 9*b*. At 3-dB bandwidth, an input referred noise of 23 pA/√Hz was obtained. From Fig. 6*b*, it can be seen that the measured and simulated input referred noise results are in agreement up to 3-dB bandwidth with slight discrepancy. When compared with the simulated results, the discrepancy with measured results may be due to process variation

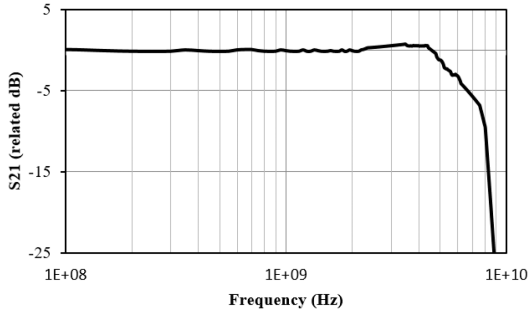
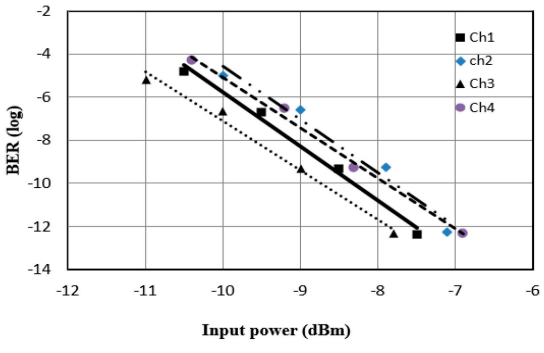
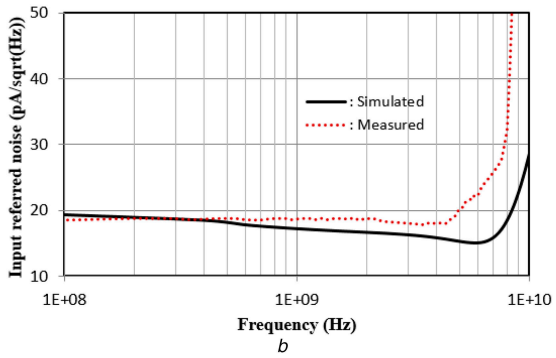


Fig. 8 *Measured frequency response of a typical channel of the 4-ch receiver*



a



b

Fig. 9 *Results showing*
(a) Sensitivity of the receiver at 7.5 Gb/s, ***(b)*** Measured and simulated output, input referred noise of the integrated receiver

during the fabrication process as well as the reasons explained in frequency response part. The performance comparison of this work and other previous works is presented in Table 1.

6 Conclusion

This work demonstrated the design of a 30 Gb/s integrated receiver array in a 0.13 µm CMOS technology. The receiver integrated an RGC TIA and an inductorless limiting amplifier employing active feedback and slew boosting techniques for high gain, large bandwidth, and small size. The optical receiver exhibits 101 dBΩ transimpedance gain and 3-dB bandwidth of 5.5 GHz. Clear measured eye diagram at constant output voltage of 320 mVp was achieved up to 7.5 Gb/s/ch. The proposed receiver consumes a power per Gbps of 8 mW/Gbps from 1.2 V supply voltage and occupies a chip area ratio of 0.28 mm^2/ch. The receiver could be applied to optical interconnects between CPU and I/O peripherals or CPU and memory stacks as well as other green IT applications.

7 Acknowledgments

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Table 1 Performance comparison of this work with other works

	This work	[12]	[5]	[4]	[9]
tech. (nm) (CMOS)	130	130	90	65	180
channel no.	4	1	1	1	1
supply (V)	1.2	2	1	1.2	1.8 (1.5)
power (mW/Gbps)	8	9.8	1.15	4.2	16.32
gain (dBΩ)	101	62	53.5	92	132.6
speed Gb/s)	30	10	5	40	3.125
VOutp (mV)	320	—	—	800	200
size (total/active) (mm^2/ch)	0.28/0.1	—/0.06	—	0.83/	0.79/—
noise (pA/sqrt(Hz) ($pA/\sqrt{Hz}$)	23	—	16.8	14	47
sensitivity	−7.5 dBm	22.4 μA	—	—	−16 dBm

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