Reconfigurable Multiphase Switched Capacitor Converters Based on Non-Binary Numeral Systems: Ternary Case

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***Abstract*–Multiphase Switched Capacitor Converters (SCC) recently gained attention due to their ability to generate different voltage Target Ratios (TR). One of the reconfigurable multiphase SCC topologies is a binary one. For this SCC, the switched capacitor normalized voltage distribution is binary as the name implies and each capacitor represents a single bit. This paper suggests SCC topologies that are based on non-binary numeral systems – ternary, quaternary etc. The potential benefits of such SCC topologies compared with binary include reduced switched capacitor stored energy and equivalent resistance. The paper investigates into ternary SCC voltage TR set, possible balanced switching implementation and equivalent resistance calculation using charge flow balance analysis. Multiphase balanced switching allows for essential switched capacitor and peak-to-peak output voltage ripple (or output filter capacitance) reduction.**

***Keywords*–DC-DC power convertor, switched capacitor converter, target ratio, multiphase switching.**

I. INTRODUCTION

Switched-Capacitor Converter (SCC) is a DC-DC power converter that transforms one voltage to another by means of semiconductor switches and capacitor elements [1], [2]. As opposed to conventional inductor-based converters, SCC doesn't employ magnetic energy storage elements. It makes an SCC topology a viable candidate for miniaturization and implementation in advanced power conversion products like power-supply-in-package and power-supply-on-chip.

Multiphase SCC become reconfigurable meaning capable of realizing multiple voltage TRs. Binary resolution converter, or binary SCC was suggested in [3]. For a step-down 3 capacitor binary SCC (Fig.1), voltage TR set includes (1/8; 3/8; 5/8; 7/8) with capacitor voltages being 1/8, 1/4, and 1/2. TRs (1/4; 3/4) are implemented with 2 capacitors, (1/2) – with a single one.

SCC equivalent circuit for average output voltage is shown in Fig.2. The equivalent resistance is a measure of SCC losses and its asymptotic approximations include Slow Switching Limit (SSL), or Complete Charge (CC), and Fast Switching Limit (FSL), or No Charge (NC) [4], [5].

For SSL approximation, switch (loop) resistances have no impact on equivalent resistance that depends on capacitances and switching frequency.

For FSL, equivalent resistance is solely defined by switch resistances. For instance, Fig.1 SCC equivalent resistance in FSL approximation equals *7r*, where *r* is a switch resistance assuming identical switches. This is because for each topology seven series switches are always in conduction. In fact, complementary switch pair 41 may be eliminated because capacitor C3 is never connected in series to the source with the same polarity. This reduces FSL equivalent resistance to *6r*.

For balanced switching, charge flow to the load in step-down multiphase SCC becomes as smooth as possible that essentially reduces switched capacitor and output voltage ripples and moderately decreases the equivalent resistance [6]-[8].

Suggested here is a concept of multiphase reconfigurable SCC based on numeral systems different from binary – ternary, quaternary etc. The potential benefits of such SCC compared with the binary one include reduced switched capacitor stored energy and equivalent resistance.

The paper investigates into ternary SCC voltage TR set, possible balanced switching implementations and equivalent resistance calculation using charge flow balance analysis.

Theoretical results are extensively verified by computer simulations.

II. TERNARY SWITCHED CAPACITOR CONVERTER

Ternary SCC topology with four switched capacitors implementing two ternary digits, or trits, is shown in Fig. 3. Such step-down ternary SCC voltage TR set is supposed to include (1/9; 2/9; 4/9; 5/9; 7/9; 8/9) with capacitor voltages

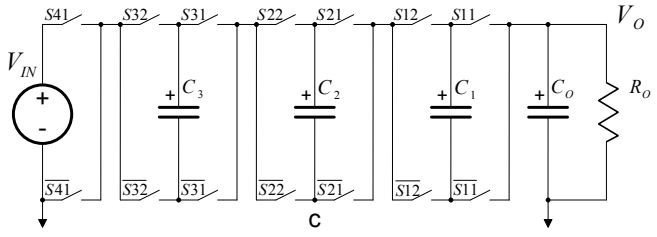

Fig. 1. Triple capacitor binary SCC.

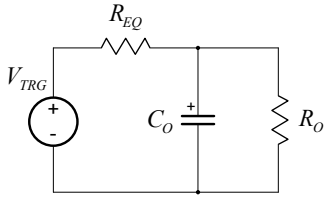

Fig. 2. SCC equivalent circuit.

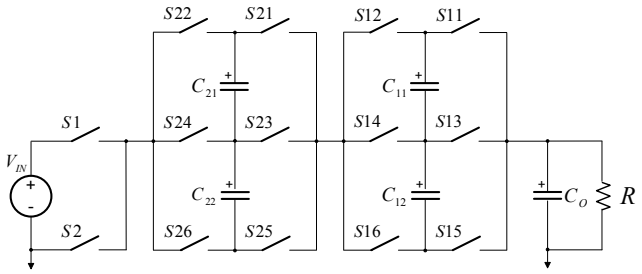

Fig. 3. Ternary SCC topology with two digits - trits.

being 1/9 in least significant trit pair and 1/3 in most significant one. TR equal to 1/3 is implemented using a single trit block.

To make a fair comparison of binary and non-binary SCC, let explore quaternary SCC with 2 quaternary digits (Fig.4) vs binary SCC with 4 bits (Fig.5).

Both SCC are capable to implement TR set (1/16; … 15/16). Binary SCC capacitor voltage distribution is 1/16; 1/8; 1/4; 1/2 while that of quaternary SCC – 1/16; 1/16; 1/16; 1/4; 1/4; 1/4.

Indeed, quaternary SCC employs more capacitors – 6 vs 4. However, switched capacitor stored energy for quaternary is less – assuming equal capacitances, it is about the sum of squared voltages which is 51/256 for quaternary vs 15/16 for binary (3.4 times difference !).

Next, quaternary SCC equivalent resistance in FSL approximation is *5r* vs *8r* for binary one (1.6 times reduction). This can be reduced by eliminating *S1/S2* complementary switch pair to *4r* but the payment will be a certain loss of functionality – not all TRs from the original set of (1/16; … 15/16) could be implemented due to imposed topological limitations (e.g., C21 and C22 can't be connected to ground).

III. Analysis of Ternary SCC

Multiphase switching with series connected capacitors may be naturally described using the language of signed binary

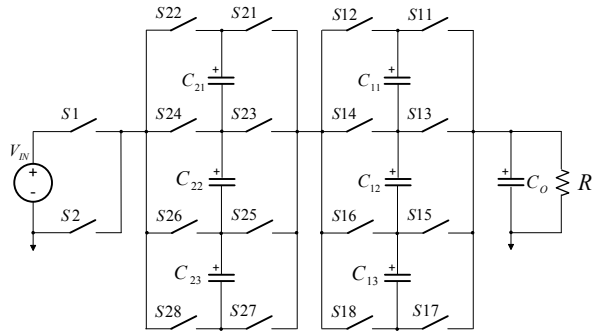

Fig. 4. Quaternary SCC with 2 digits – quads.

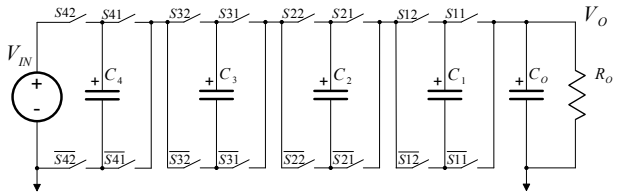

Fig. 5. Binary SCC with 4 bits.

tables [3], [7]-[11]. Table I shows all five switching topologies that implement 1/9 normalized output voltage for normalized capacitor voltages distribution 1/9, 1/9, 3/9, 3/9.

TABLE I
UNBALANCED IMPLEMENTATION OF TR=1/9; BALANCED VOLTAGES
V22=3/9; V21=3/9; V12=1/9; V11=1/9

	A	A22	A21	A12	A11
1	0	0	0	0	1
2	0	0	0	1	0
3	0	1	0	-1	-1
4	0	0	1	-1	-1
5	1	-1	-1	-1	-1

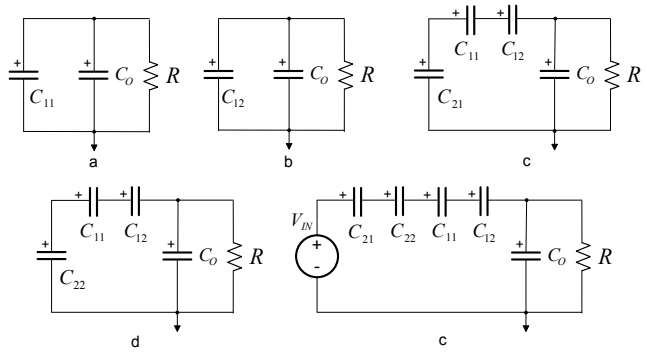

Fig. 6. Five topologies for multiphase switching – TR=1/9.

Table I topologies are presented in Fig.6.

SCC behavior is analyzed using switched capacitors charge balance equations [3], [7]-[11]. For Table I, SCC topologies charge balance equations become:

$$\begin{aligned} &Q_3 - Q_5 = 0; \quad Q_4 - Q_5 = 0; \\ &Q_2 - Q_3 - Q_4 - Q_5 = 0; \\ &Q_1 - Q_3 - Q_4 - Q_5 = 0; \\ &Q_1 + Q_2 + Q_3 + Q_4 + Q_5 = Q. \end{aligned} \tag{1}$$

The five variables in (1) present charges flowing into the load for the five switching topologies. The first four equations express capacitors C22, C21, C12 and C11 charge balance while the last one – the load charge balance over the switching period.

The solution of (1) is

$$Q_4 = Q_5 = Q/3, \quad Q_1 = Q_2 = Q_5 = Q/9. \tag{2}$$

By inspection of (2), the multiphase switching is unbalanced because different charges are supplied to the load for different switching phases. To make it balanced ([8]-[11], topologies 1 and 2 have to be replicated three times that will result in the same charge *Q/9* being transferred to the load during each of nine switching phases (Table II).

TABLE II
BALANCED IMPLEMENTATION OF TR=1/9; BALANCED VOLTAGES
V22=3/9; V21=3/9; V12=1/9; V11=1/9

	A	A22	A21	A12	A11
1	0	0	0	0	1
2	0	0	0	1	0
3	0	1	0	-1	-1
1	0	0	0	0	1
2	0	0	0	1	0
4	0	0	1	-1	-1
1	0	0	0	0	1
2	0	0	0	1	0
5	1	-1	-1	-1	-1

In Table II, the nine topologies are arranged so that every capacitor successively appears only with alternating polarities. This is a balanced switching that makes the energy transfer to converter output as smooth as possible minimizing output and individual capacitor maximum voltage ripples ([8]-[11]).

As the switching of the same trit capacitor pairs (C11, C12) and (C21, C22) is not symmetric (one of the capacitors always appears before another), the balanced voltages of the same trit capacitors are different. This way, it is suggested to add nine more switching phases (Table III) using the same topologies to make the switching symmetrical - to make "symmetrization".

TABLE III
BALANCED IMPLEMENTATION OF TR=1/9 WITH SYMMETRIZATION;
BALANCED VOLTAGES V22=3/9; V21=3/9; V12=1/9; V11=1/9

	A	A22	A21	A12	A11
1	0	0	0	0	1
2	0	0	0	1	0
3	0	1	0	-1	-1
1	0	0	0	0	1
2	0	0	0	1	0
4	0	0	1	-1	-1
1	0	0	0	0	1
2	0	0	0	1	0
5	1	-1	-1	-1	-1
2	0	0	0	1	0
1	0	0	0	0	1
4	0	0	1	-1	-1
2	0	0	0	1	0
1	0	0	0	0	1
3	0	1	0	-1	-1
2	0	0	0	1	0
1	0	0	0	0	1
5	1	-1	-1	-1	-1

Fig.7-12 present simulation results for current flow to the load along with output and switched capacitor voltages. They illustrate reduction of voltage ripples and uniform charge

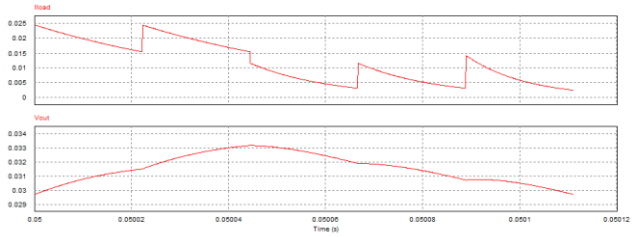

Fig. 7. Current flow to the load and output voltage for TR=1/9 unbalanced implementation.

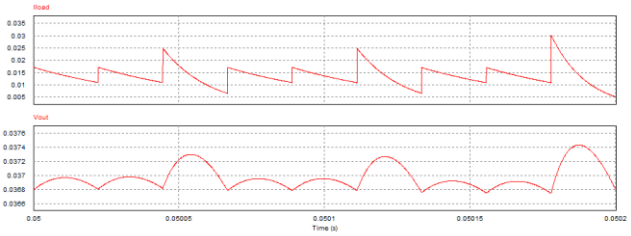

Fig. 8. Current flow to the load and output voltage for TR=1/9 balanced implementation.

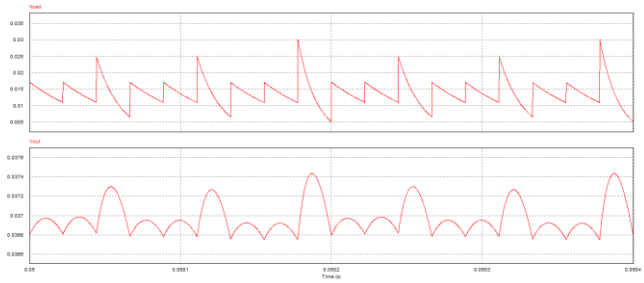

Fig. 9. Current flow to the load and output voltage for TR=1/9 balanced implementation with symmetrization

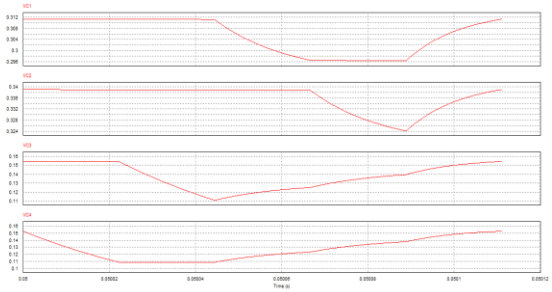

Fig. 10. Capacitor voltages for TR=1/9 unbalanced implementation.

distribution for balanced switching. From Fig.12, after symmetrization the same trit pair capacitor voltages become symmetrical shifted with the same average.

Ternary SCC with TR=1/9 equivalent resistance calculation based on phase transferred charges (phase average current) ([3], [4], [10]) yields the following formulas for unbalaced, balanced and reduced balanced implemention –

$$R_{EQ\_UB} = \frac{1}{162 f_S C}\left(18\coth\frac{\beta}{10} + 6\coth\frac{3\beta}{10} + 4\coth\frac{2\beta}{5}\right); \quad (3)$$

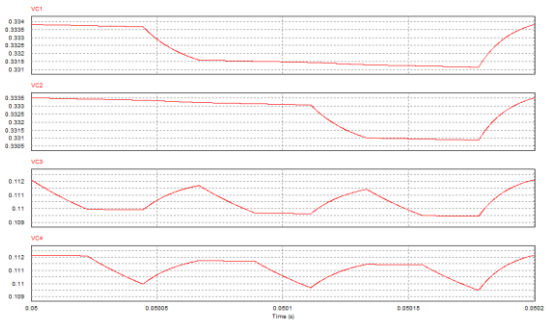

Fig. 11. Capacitor voltages for TR=1/9 balanced implementation.

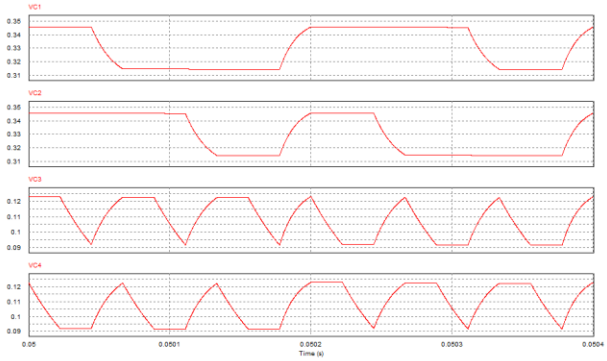

Fig. 12. Capacitor voltages for TR=1/9 balanced implementation with symmetrization.

$$R_{EQ\_B} = \frac{1}{162 f_S C}\left(6\coth\frac{\beta}{10} + 6\coth\frac{3\beta}{10} + 4\coth\frac{2\beta}{5}\right); \quad (4)$$

$$R_{EQ\_RB} = \frac{1}{162 f_S C}\left(6\coth\frac{\beta}{8} + 6\coth\frac{3\beta}{8} + 4\coth\frac{\beta}{2}\right). \quad (5)$$

where $\beta = 1/(f_{CL} rC)$; C – switched capacitance (equal for all 4 capacitors); r - switch resistance (equal for all switches); f_{CL} - clock frequency (by individual switching intervals); f_S - switching frequency (by overall switching period).

For symmetrized implementation, equivalent resistance is the same as for the balanced case since it does not depend on the order of switching topologies.

SSL and FSL equivalent resistance limits for unbalanced, balanced and reduced implementation of TR=1/9 are simply derived by taking limits of (3)-(5) for $\beta \to 0$ and $\beta \to \infty$ respectively. This yields the following expressions:

$$R_{EQ\_SSL\_UNB} = \frac{14}{81 f_S C}; \quad R_{EQ\_SSL\_BAL} = \frac{8}{81 f_S C}; \quad R_{EQ\_SSL\_RED} = \frac{8}{81 f_S C}; \quad (6)$$

$$R_{EQ\_FSL\_UNB} = 6.48r; \quad R_{EQ\_FSL\_BAL} = 5r; \quad R_{EQ\_FSL\_RED} = 4r. \quad (7)$$

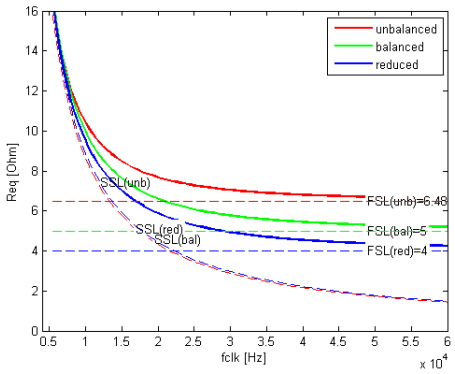

Fig. 13. Frequency behavior of equivalent resistance for unbalanced, balanced and reduced implementation of TR=1/9 for r=1 Ohm and C=10 uF.

Equivalent resistances frequency behavior graphs (including SSL) given in Fig.13 clearly illustrate that the balanced implementation is better than the unbalanced, and the reduced one is even better in terms of power dissipation.

Now consider ternary SCC implementation of TR=2/9. Seven available topologies are shown in Table IV. Charge balance equations for C22, C21, C12 and C11 become

$$Q_4 + Q_5 - Q_6 - Q_7 = 0; \quad Q_2 + Q_3 - Q_6 - Q_7 = 0;$$
$$Q_1 - Q_3 - Q_5 - Q_7 = 0; \quad Q_1 - Q_2 - Q_4 - Q_6 = 0; \quad (8)$$
$$Q_1 + Q_2 + Q_3 + Q_4 + Q_5 + Q_6 + Q_7 = Q.$$

TABLE IV
UNBALANCED IMPLEMENTATION OF TR=2/9: BALANCED VOLTAGES
V22=3/9; V21=3/9; V12=1/9; V11=1/9

	A	A22	A21	A12	A11
1	0	0	0	1	1
2	0	0	1	0	-1
3	0	0	1	-1	0
4	0	1	0	0	-1
5	0	1	0	-1	0
6	1	-1	-1	0	-1
7	1	-1	-1	-1	0

TABLE V
BALANCED IMPLEMENTATION OF TR=2/9; BALANCED VOLTAGES
V22=3/9; V21=3/9; V12=1/9; V11=1/9;

	A	A22	A21	A12	A11
1	0	0	0	1	1
2	0	0	1	0	-1
7	1	-1	-1	-1	0
1	0	0	0	1	1
3	0	0	1	-1	0
4	0	1	0	0	-1
1	0	0	0	1	1
6	1	-1	-1	0	-1
5	0	1	0	-1	0

Linear algebraic equations (8) are underdetermined because the number of unknowns - 7 - is larger than the number of equations - 5. Underdetermined equations have an infinite set of solutions. According to the Minimal Norm Principle (MNP) suggested in [10], the nature selects the solution with the minimal Euclidean norm. Application of the MNP yields

$$Q_1 = Q/3, \quad Q_2 = Q_3 = Q_4 = Q_5 = Q_6 = Q_7 = Q/9. \qquad (9)$$

Fig.14-17 illustrate ternary SCC realization of TR=2/9 for balanced and unbalanced switching.

TR=8/9 and 7/9 complementary to TR=1/9 and 2/9 are implemented using "negated" switching tables - 0s and 1s in the source column A are replaced by 1s and 0s respectively; in capacitor columns A11, A12, A21 and A22 0s remain unchanged while (-1)s are replaced by 1s and vice versa. The expressions for SCC equivalent resistance (like (3) and (4) for TR=1/9) are valid for the complementary TRs (TR=8/9).

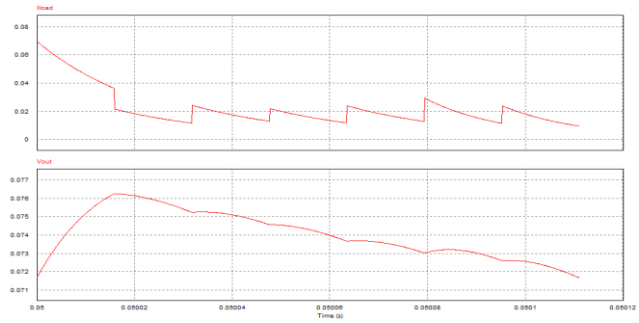

Fig. 14. Current flow to the load and output voltage for TR=2/9 unbalanced implementation.

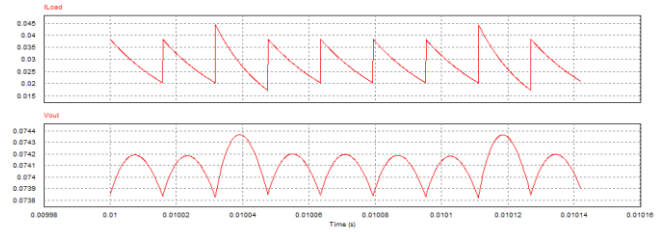

Fig. 15. Current flow to the load and output voltage for TR=2/9 balanced implementation.

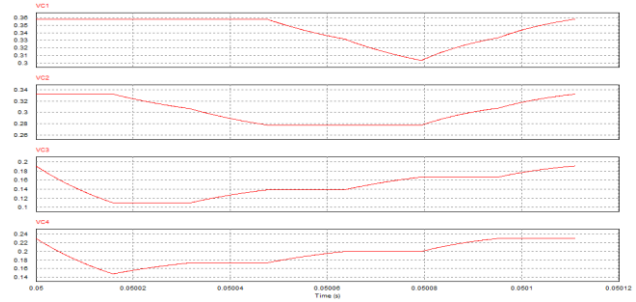

Fig. 16. Capacitor voltages for TR=2/9 unbalanced implementation.

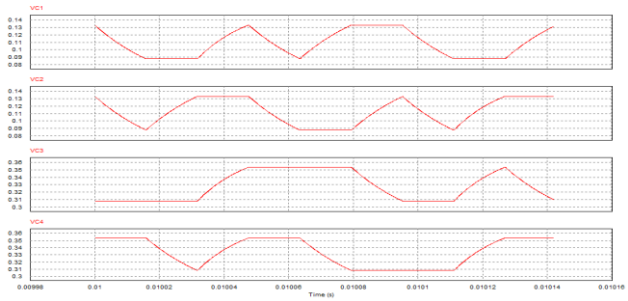

Fig. 17. Capacitor voltages for TR=2/9 balanced implementation.

For a 3 capacitor binary SCC (Fig.1), initially considered TR set was (1/8; 3/8; 5/8; 7/8). However, later on it was found that it can additionally generate any target ratio from (1/5; … ; 4/5; 1/6; … ; 5/6; 1/7; … ; 6/7) ([6], [8]). Similar to that, ternary SCC with 2 trits (4 switched capacitors) in addition to (1/9; 2/9; 4/9; 5/9; 7/9; 8/9) can deliver TR from (1/5; … ; 4/5; 1/6; … ; 5/6; 1/7; … ; 6/7; 1/8; … ; 7/8). For that, the most significant "trit" capacitor average voltage must be 3 times that of the least significant "trit".

Consider ternary SCC implementation of *TR=2/8*. Six available topologies are shown in Table VI.

TABLE VI
UNBALANCED IMPLEMENTATION OF TR =2/8;
BALANCED VOLTAGES V1=3/8; V2=3/8; V3=1/8; V4=1/8;

	A	A22	A21	A12	A11
1	0	0	0	1	1
2	0	0	1	0	-1
3	0	0	1	-1	0
4	0	1	0	0	-1
5	0	1	0	-1	0
6	1	-1	-1	0	0

TABLE VII
BALANCED IMPLEMENTATION OF TR=2/8;
BALANCED VOLTAGES V1=3/8; V2=3/8; V3=1/8; V4=1/8

	A	A22	A21	A12	A11
1	0	0	0	1	1
5	0	1	0	-1	0
2	0	0	1	0	-1
6	1	-1	-1	0	0
1	0	0	0	1	1
4	0	1	0	0	-1
3	0	0	1	-1	0
6	1	-1	-1	0	0

Table VI charge balance equations are underdetermined because the number of unknowns – 6 – is larger than the number of equations – 5. Application of the MNP yields

$$Q_1 = Q_6 = Q/4, \quad Q_2 = Q_3 = Q_4 = Q_5 = Q_7 = Q_8 = Q/8. \qquad (10)$$

Balanced implementation shown in Table VII employs two replications of topologies 1 and 6 as suggested by (10).

Fig.18-21 illustrate ternary SCC realization of TR=2/8 for balanced and unbalanced switching. As usually, balanced switching reduces output and capacitor voltage ripples.

In addition, after symmetrization the same trit pair capacitor voltages will become symmetrical with the same average.

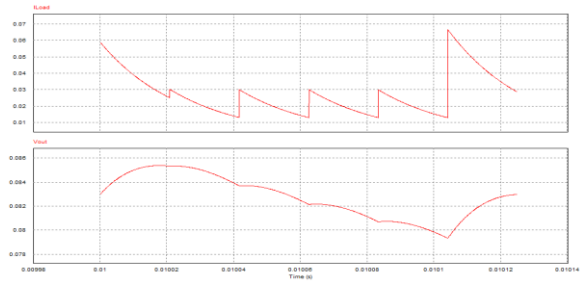

Fig. 18. Current flow to the load and output voltage for TR=2/8 unbalanced implementation.

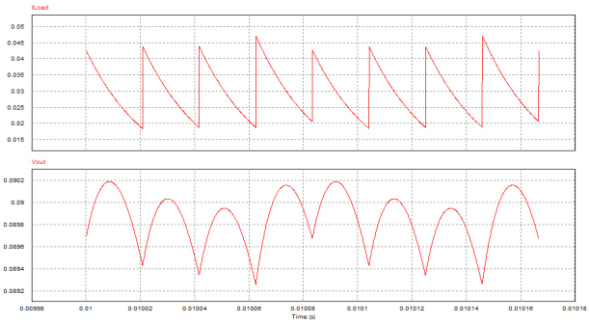

Fig. 19. Current flow to the load and output voltage for TR=2/8 balanced implementation.

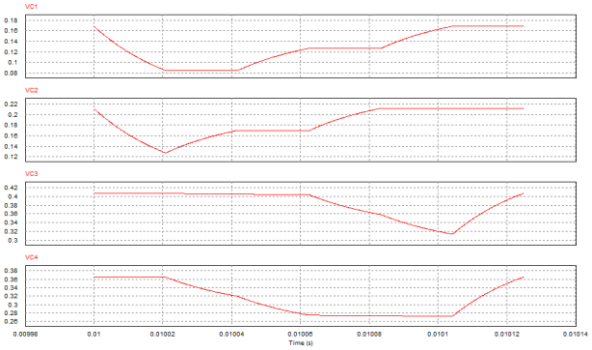

Fig. 20. Capacitor voltages for TR=2/8 unbalanced implementation.

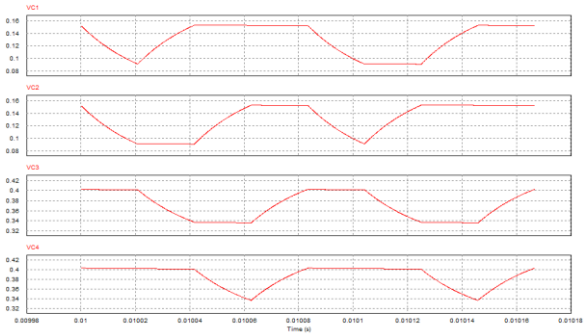

Fig. 21. Capacitor voltages for TR=2/8 balanced implementation.

IV. Conclusion

Reconfigurable multiphase Switched Capacitor Converters provide multiple voltage Target Ratios. Binary SCC can generate "binary" TRs (1/8; 3/8; 5/8; 7/8) and additionally (1/5; … ; 4/5; 1/6; … ; 5/6; 1/7; … ; 6/7). This paper suggested multiphase SCC based on non-binary numeral systems - ternary, quaternary etc. – that have the advantages of reduced switched capacitor stored energy and equivalent resistance.

Ternary SCC with 2 trits considered in the paper can generate "ternary" voltage TRs (1/9; 2/9; 4/9; 5/9; 7/9; 8/9) and additionally (1/5; … ; 4/5; 1/6; … ; 5/6; 1/7; … ; 6/7; 1/8; … ; 7/8) given that the most significant "trit" capacitor average voltage is three times that of the least significant "trit".

Balanced switching makes the energy transfer to converter output as smooth as possible minimizing output and individual capacitor voltage ripples and reduces equivalent resistance for the same clock frequency.

Based on charge balance equation, it is possible to calculate equivalent resistance formula that is valid for the whole switching frequency range from SSL to FSL. Analytical equivalent resistance calculations are well supported by SCC computer simulations. There are minor discrepancies in low frequency range due to unaccounted filter capacitance that has practically no impact for relatively high frequency switching.

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