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Advances in Top Transparent Electrodes by Physical Vapor Deposition for Buffer Layer-Free Semitransparent Perovskite Solar Cells

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The advancements in halide perovskite materials, celebrated for their exceptional optoelectronic properties, have not only led to a remarkable increase in the efficiency of perovskite solar cells (PSCs) but also opened avenues for the development of semitransparent devices. Such devices are ideally suited for integration into building facades and for use in tandem solar cell configurations. However, depositing transparent electrodes (TEs) on top of the charge transport layers in PSC poses significant challenges. Physical vapor deposition (PVD), commonly used in the industry to prepare transparent conducting oxides (TCOs) as TEs, can introduce plasma-induced damage during the process, which decreases the efficiency of the final devices. While incorporating a buffer layer is the typical approach to mitigate plasma damage, it also increases the complexity and costs of solar cell fabrication. This perspective focuses on the developments of buffer-free semitransparent PSCs. It highlights the shift away from the typical approach of incorporating a buffer layer. Through a comprehensive analysis of recent research, this work presents successful cases of direct TCO deposition onto transport layers, evaluates scalability and stability, and concludes with recommendations for optimizing PVD processes in the fabrication of buffer-free PSCs.

1. Introduction

Hybrid organic–inorganic perovskite solar cells (PSCs) have attracted significant research interest due to their remarkable surge in power conversion efficiencies (PCEs). The latest developments have achieved PCEs exceeding 26%,[1,2] which can be attributed to the excellent optoelectronic properties of halide perovskite materials, including high absorption coefficients[3] and long carrier lifetimes.[4] Moreover, the bandgap tunability and versatile thin-film deposition techniques extend their applications beyond traditional opaque single-junction solar cells to semitransparent devices. These are particularly promising for building-integrated photovoltaics and as the top cell in tandem configurations with Si or copper indium gallium selenide solar bottom cells.[5,6]

PSCs typically consist of a photoactive perovskite layer sandwiched between an electron transport layer (ETL), a hole transport layer (HTL), and two electrodes. Depending on the sequence of charge transport layers (CTLs), PSCs can be categorized into two configurations: the regular n–*i*–p and the inverted p–*i*–n structure. In the n-*i*-p configuration, the sequence from the side facing the illumination begins with the ETL, followed by the light-harvesting perovskite absorber, and then the HTL, whereas p–*i*–n structure reverses this arrangement. For semitransparent PSCs (ST-PSC), it is essential that both outer electrodes allow light to reach the absorber. The transparent electrode (TE) must exhibit low parasitic absorption to maximize light coupling into the active layer and possess minimal sheet resistance (R_{sh}) and low contact resistance with adjacent layers. The TE that faces the illumination is typically deposited on glass, allowing for higher fabrication temperatures and deposition process energies. Conversely, the deposition of the electrode atop the device stack, particularly over the delicate organic CTL, imposes additional restrictions from a fabrication viewpoint. In this manuscript, we primarily focus on the specific challenges associated with depositing transparent conducting oxides (TCOs) as the rear electrode for semitransparent PSCs. For a comprehensive examination of the requirements for TEs across various optoelectronic devices, extending beyond just solar applications and TCOs, the readers can refer to the existing detailed overview.[7]

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TCOs are the predominant choices as TEs, with physical vapor deposition methods (PVD) being the most common techniques adopted for this application. Thin films of TCOs fabricated by PVD methods (especially, magnetron sputtering [MS]) are favored for their excellent optoelectronic properties, high reproducibility, and the ability to form dense compact layers that serve as barriers against metal diffusion and humidity. However, the kinetic energy of particles, emissions from the plasma, and heat generated during PVD processes can damage the underlying sensitive layers, including the CTLs and the active perovskite material.[8,9] Such damage can lead to structural changes that adversely affect the overall performance and stability of the devices. Therefore, the effective implementation of TCOs as rear electrodes necessitates strategies to mitigate plasma-related damage while simultaneously preserving the quality of the film. A prevalent strategy to counteract plasma-induced damage involves the incorporation of additional thin-film layers that are resilient to PVD-induced effects. In this manuscript, these layers are referred to as buffer layers, though they are also commonly referred to in the literature as protective, interfacial, or blocking layers.

The integration of such buffer layers, however, introduces increased cost and complexity, especially in case of the metal oxides prepared by atomic layer deposition (ALD) for record-breaking p–*i*–n ST-PSC. Moreover, buffer layers may enhance parasitic absorption and/or reflection introduced by these layers potentially limiting the device photocurrent.[10] Additionally, it has been noted that some buffer layers can adversely affect the overall stability of the device (for instance, in case of MoO_x buffer layer[11]) presenting a significant challenge to achieving long-term reliability of PSCs. Consequently, elimination of buffer layers for PSCs becomes a desirable objective.

This works aims to provide a comprehensive overview of recent research efforts focused on the development of buffer-free ST-PSCs with the top TCO electrode prepared by PVD. The origins of damage induced by PVD will be explored. This will be followed by an examination of the impact of such damage and discussion of assessment methods at the both device level and through material characterization. Next, a detailed analysis of successful cases of devices where TCOs were applied directly onto CTL using PVD will be presented. Then the scalability and stability of these buffer-free ST-PSC devices as reported in the literature will be assessed. The perspective will be concluded with recommendations for optimizing TCO deposition via PVD in the fabrication of buffer-free PSCs.

2. Origins of Plasma-Induced Damage

The fundamental causes of plasma damage should be identified in order to establish physics-driven guidelines for optimization of fabrication processes as discussed in Section 6. PVD represents a group of techniques essential for thin-film manufacturing, with plasma-assisted PVD methods being predominant in the fabrication of TCOs for PSC. In these processes, atoms are transferred from a target material to a substrate through the bombardment by high-energy particles, typically argon ions. Oxygen is often introduced in cases of reactive sputtering or to maintain stoichiometry during oxide depositions. Operating in a low-pressure environment, these nonthermal processes allow the ejected material to form a thin film on the substrate. In addition to the common MS, other types of PVD methods, such as pulsed laser deposition (PLD) and ion beam sputtering (IBS), employ different mechanisms for plasma generation and subsequent atom ejection. PLD utilizes an optical energy source, whereas IBS uses an ion beam, in contrast to the electric field application to the cathode (target material) utilized in MS.

Damage incurred during the deposition of TCOs by PVD is often a result of the substrate being bombarded by a variety of highly energetic species. This process involves numerous participants, including atoms ejected from the target surface, negative ions from the carrier gas and the target surface itself, positive ions generated within the plasma, and reflected atoms and neutralized ions from the target surface.[12] Additionally, thermal effects, such as direct heating and the formation of cracks due to mismatches in thermal expansion coefficients[13] and UV luminescence,[14] also contribute to plasma-induced damage as shown in **Figure 1**. The latter has not been studied in detail for this family of absorber materials, but changes in strain within perovskite films have been linked to plasma radiation during the sputtering process, as shown by X-ray diffraction (XRD) analysis.[9] The structural changes can affect the thin-film properties and, consequently, the device performance. In addition, photoinjection-related mechanisms are likely to contribute to the observed degradation. UV radiation has been shown to create deep defects due to the formation of surface states at the Si/SiO_2 interfaces[15] and a-Si/c-Si interfaces, where dangling bonds are partially formed by plasma luminescence.[16] More research attention should be dedicated to understanding and mitigating these effects in PSCs. The means to monitor plasma luminescence effects would be additionally discussed in Section 6.

Despite the multitude of potential damaging factors involved, prior research has identified negatively charged oxygen ions (O^-) as the primary contributors to substrate bombardment[9,17] during the PVD process. To understand the dynamics of energy

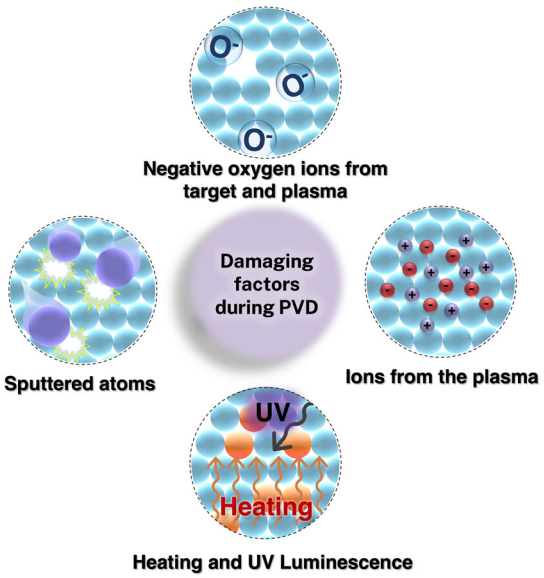

Figure 1. Overview of factors that may induce damage to underlying layers during TCO PVD.

dissipation by particles in a plasma vacuum process, it is essential to consider the interactions through collisions with surrounding particles, the impact of initial energy of the particles on these interactions, and the influence of process parameters on the overall deposition process. Prior to studying the interplay of these concepts, the concepts of thermalization distance will be elaborated. Following the approach outlined by Westwood that is based on the kinetic gas theory,[18] the thermalization distance refers to the typical distance an atom, initially emitted from a target, must travel in its initial trajectory to decrease its speed to the mean velocity of the surrounding gas.

To derive this, one can first consider the average mean free path which corresponds to the distance a given sputtered particle (SP) travels before the next collision. The mean free path length (λ_{mf}) between two spherical particles, SP and a gas particle, can be found via Equation (1).

$$\lambda_{mf} = \frac{k_b \times T}{\sqrt{2} \times P_d \times \pi \times d_m^2} \quad (1)$$

where k_b is Boltzman constant, T is background gas temperature, P_d is deposition pressure, and d_m is the mean atomic diameter between a gas and SP, that can be expressed as $d_m = \frac{d_{gas}+d_{sp}}{2}$.

The ratio between mean-free path and the target-to-substrate (d_{ts}) distance to a big extent defines the character of the film growth and the energetic impact of the sputtering process. Clearly, in the "vacuum-like" regime ($\lambda_{mf} > (d_{ts})$), where little-to-no interactions with the background gas take place, the damage from energetic particles is more expected. However, as can be seen from the equation, the mean free path does not depend on the SP energy, whereas, intuitively, the thermalization distance does since SPs with higher energies would require more collision events (n) to thermalize rather than their counterparts with lower energy.

Scattering of a sputtered atom by a gas atom is assumed to be isotropic. The sputtered atom loses some of its energy and changes direction when it collides with a gas atom. The particles are assumed to travel parallel to the target normal while scattering with alternating positive and negative scattering angles. The energy before and after a collision are written as E and E^1 respectively. The scattering angle in the chosen geometry is defined as θ. The energy of the sputtered atom each time it scatters with a background gas atom at an averaged scattering angle $\langle\theta\rangle$ is reduced by a factor $\langle E^1/E\rangle$. Using the calculated average scattering energy ratio,[18] the amount of collisions n that is required to reduce the energy of the ablated species with initial energy E_0 to E_g can be calculated via

$$n = \frac{\ln(E_o/E_g)}{\ln(\langle E^1/E\rangle)} \quad (2)$$

In its turn, thermalization distance D is expressed as: $D = n \times \lambda_{mf}$. This formula tends to underestimate the thermalization distance for particles with higher energy so for practical calculations one can use $D \approx 1.25n \times \lambda_{mf}$. As shown from Equation (1) and (2), lowering the initial scattering energy of the sputtered atoms/ions, as well as increasing deposition pressure (P_d), promotes thermalization, which could be taken into account for the PVD process optimization.

Jagt et al.[19] showed that for a typical nonoptimized 'soft landing' PVD process of doped indium oxide at $P_d = 0.4$ Pa, thermalization distance for atomic In is ≈20 cm. This is significantly larger than a common d_{ts} of 5–7 cm for many sputtering systems meaning that a substantial amount of arriving atoms has energies exceeding that of C=C bonds (6.2 eV)[20] in organic CTLs. The detrimental impact of such high-energy bombardment is discussed in Section 3.

3. Impact of Deposition of Transparent Electrodes on Perovskite Solar Cells

In PSCs of both n–*i*–p and p–*i*–n architectures, the CTLs often consist of thin films of organic materials, such as spiro-OMeTAD as HTL or C_{60} (fullerene) as ETL, which are prone to damage from plasma exposure. The energy of particles within the plasma discharge has the potential to dissociate surface bonds or etch away these soft organic layers. When damage occurs, devices often display S-shaped current density–voltage (J–V) curves, a phenomenon that has been observed in cells of both architectures, as depicted in **Figure 2**. This behavior significantly impairs

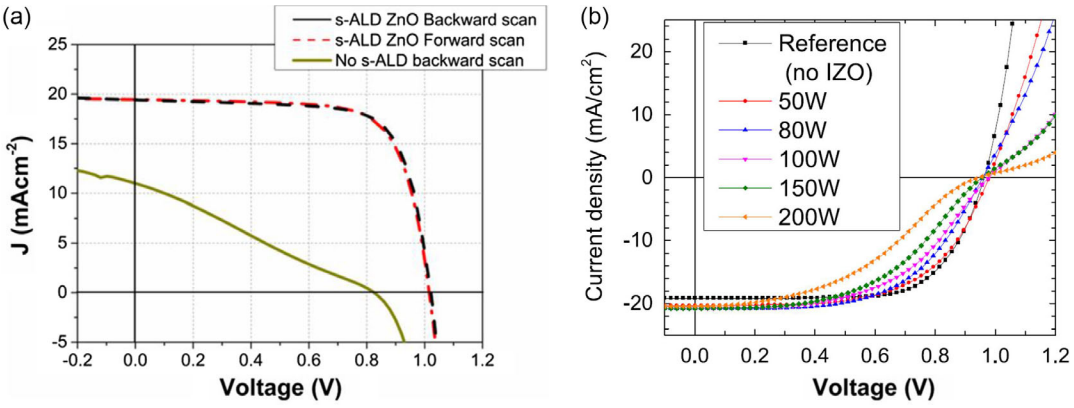

Figure 2. Sputtering damage in PSCs. a) J–V curves for p–*i*–n PSCs, comparing configurations with and without an ALD ZnO buffer layer, are presented. Reprinted with permission.[42] Copyright 2018, Wiley-VCH. b) For n–*i*–p PSCs without a buffer layer, the J–V curves exhibit an S-shape, which is more pronounced with the increase of sputtering power used for depositing the IZO layer. Reprinted with permission.[21] Copyright 2015, Elsevier.

device performance, particularly resulting in decreased fill factors (FFs) and open-circuit voltage losses, which in turn reduce the overall power output. However, the emergence of the S-shape in the curves is not merely due to compromised series and shunt resistances. Instead, it is more accurately explained by physical damage to the layers beneath TCO that can result in film cracking, which leads to changes in work function, thereby inducing energy barriers to carrier extraction or increased nonradiative recombination due to defect introduction.

This claim is further supported by the following observation: in case presented in Figure 2a, the introduction of an ALD-grown ZnO layer, despite adding extra resistance, proves beneficial for FF of devices. This suggests that the metal oxide layer serves a protective role in addition to facilitating electron extraction. Furthermore, for the n–*i*–p device with a sputtered indium zinc oxide (IZO) electrode (Figure 2b), an increase in sputter power enhances the curvature of the *J*–*V* characteristics while the sheet resistance (R_{sh}) of the TCO has insignificantly changed. This indicates that the observed changes in the *J*–*V* curve characteristics are likely due to modifications in the HTL/TCO interface properties rather than alterations in the conductive properties of the TCO layer itself.

Illumination-dependent *J*–*V* measurements are powerful techniques for investigating CTL/TCO interface degradation due to charge accumulation or carrier extraction barriers. Werner et al. in a pioneering study,[21] utilized these measurements to detect a hole extraction barrier, indicated by S-shaped *J*–*V* curve distortions that intensify with increased illumination. For a more quantitative analysis, illumination-dependent open-circuit voltage (V_{oc}) measurements can be insightful. By plotting V_{oc} against light intensity on a semilogarithmic scale and applying a linear fit, the ideality factor ranging from 1 to 2 can be calculated. This factor differentiates between purely radiative recombination ($n_{id} = 1$) and nonradiative, trap-assisted recombination ($n_{id} = 2$).[22] In a relevant case study, Hartel et al.[10] showed that using a higher RF sputter power for IZO deposition on a C_{60}/PEIE layer increases the ideality factor, from 1.42 at 2.41 W cm^{-2} to 1.50 at 4.21 W cm^{-2} (**Figure 3**a). This implies that lowering the radio frequency (RF) sputter power could improve V_{oc} and FF by reducing trap-assisted recombination.

Within the series of illumination-dependent *J*–*V* measurements, dark-current density assessments offer similar insights into ideality factors (once compared to the *J*–*V* characteristics under illumination). In addition, they also reveal potential shunt resistances and shorts, possibly induced by, for instance, indium (In) particle penetration into the organic stack during PVD. Zanoni et al.[23] explored this method to analyze devices with ITO fabricated via PLD at varying chamber pressures, from 0.007 to 0.1 mbar. The analysis of dark current density versus voltage for devices with various PLD ITO electrodes indicated that direct shorts were not generated by the deposition process, as evidenced by the leakage current characteristics displayed in Figure 3b.

To further investigate the influence of interfacial recombination on V_{oc}, temperature-dependent *J*–*V* measurements can be utilized. Rai et al.[24] conducted such measurements to compare semitransparent and opaque cells as shown in (Figure 3c). The observed V_{oc} loss in ST-PSCs is attributed to the combined effects of R_{sh} of ITO and contact barrier, with an extrapolated V_{oc} at 0 K of 1.496 V for ITO devices compared to 1.424 V for gold (Au), against a bandgap of 1.6 eV for the chosen composition of perovskite. Given identical stack configurations, this loss is attributed to recombination at the spiro-OMeTAD/electrode interface —but similar methodologies can be extended to comparisons between buffer-containing and buffer-free ST-PSCs.

3.1. Material Characterization-Related Damage Evidence

In addition to changes in the interfacial energy levels, the high-energy particle bombardment can induce structural changes within the CTL and absorber layers, observable through cross-sectional electron microscopy techniques, including both transmission electron microscopy (TEM) and scanning electron microscopy (SEM). For instance, the ITO deposition process has been linked to the formation of numerous voids within the spiro-OMeTAD layer, alongside evident damage to the perovskite layer itself, as shown in **Figure 4**a,b. In this particular study by Jeong et al.[25] NiO_x has been shown to been resistant to the same sputtering condition. In a different example for p–*i*–n structure (as seen in Figure 4c), similar high-energy particle interaction during ITO deposition by MS results in partial shrinkage and collapse of the device structure, as the kinetic and thermal energies transferred from the colliding particles affect both the double ETL consisting of PCBM and ZnO and

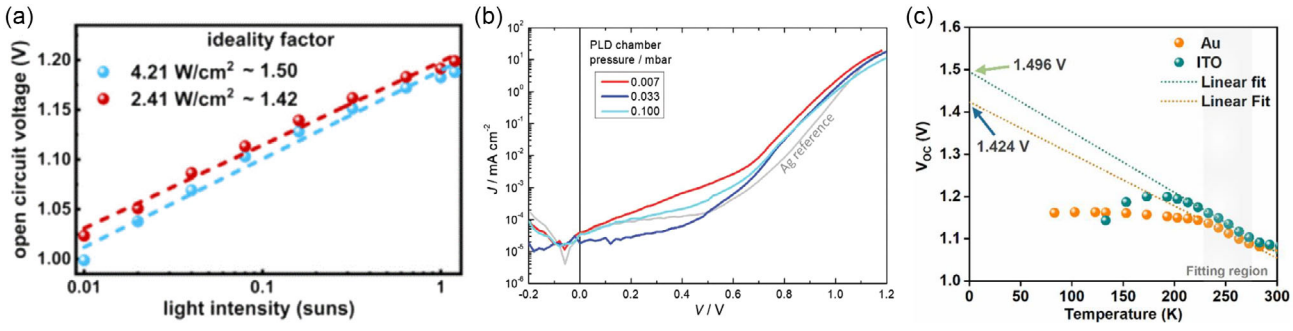

Figure 3. Device-related methods to assess the PVD-induced damage. a) Light intensity-dependent V_{oc} for single-junction devices with IZO front electrodes sputtered at power densities of 4.21 and 2.41 W cm^{-2}. Reprinted with permission.[10] Copyright 2023, Elsevier. b) Dark *J*–*V* curve for devices with ITO top electrodes deposited under different PLD chamber pressures. Reprinted with permission.[23] Copyright 2022, Wiley-VCH. Please note that minimum current density is not at zero volts, but this is an artifact of the analysis due to scan direction and scan rate. c) Temperature-dependent V_{oc} measurement of PSC with ITO or Au rear electrode. Reprinted with permission.[24] Copyright 2021, Wiley-VCH.

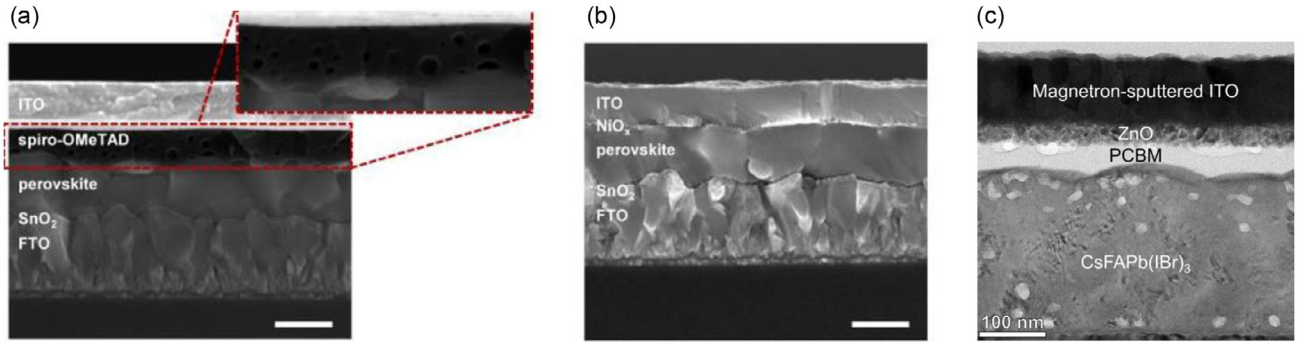

Figure 4. Cross-sectional SEM images for n–*i*–p ST-PSC stacks: a) perovskite/spiro-OMeTAD/ITO; b) perovskite/NiO_x/ITO. Reprinted with permission.[25] Copyright 2022, Wiley-VCH. c) Cross-sectional high resolution transmission electron microscopy (HRTEM) image of the p–*i*–n ST-PSCs with damaged ETL from magnetron-sputtered ITO top cathode. Reprinted with permission.[43] Copyright 2023, Elsevier.

the perovskite absorber layer beneath. In a study by Yoon et al.[26] HR-TEM was also employed to study the structural properties of the photoactive layer after TCO sputtering. These were accompanied by Fourier-transform diffraction patterns (**Figure 5**), indicating the presence of a parasitic trigonal lead iodide (PbI_2) phase in the absorber for the ITO deposited under nonoptimized conditions. The perovskite layer decomposition has been evidenced by the appearance of a PbI_2 peak in XRD analyses (Figure 5j), which is a much faster and noninvasive characterization method.

X-ray photoelectron spectroscopy (XPS) can provide valuable insights into degradation mechanisms. Recent research by Yang et al. employed XPS measurements to study a triple-cation perovskite/evaporated C_{60} system after TCO sputtering.[9] XPS revealed that C═N bonds at the perovskite surface dissociate under plasma irradiation due to phonon propagation, resulting in a minor loss of FA^+ ions from the multication perovskite layer. These observations, along with modeling in that study, indicated that impinging ions lack sufficient energy to penetrate the C_{60} and thus would not directly affect the perovskite. Instead, it is proposed that the heat transferred by polarons to the perovskite surface layer is responsible for the deterioration of final device performance.

The absence of deposition-induced damage can be reflected by no infiltration of In, tin (Sn), and/or zinc (Zn) case atoms into the device layers, achievable through direct inspection methods such as energy-dispersive X-ray spectroscopy (EDX). Notably, the integration of EDX with depth profiling techniques alongside TEM enhances the precision of visualization and elemental characterization of the device layers. In these cases, the absence of foreign material infiltration through the respective ETLs has been verified after TCO deposition.[23,27] However, it is important to acknowledge the limitations associated with these characterization techniques. Specifically, the resolution may become a challenge when analyzing extremely thin layers (≈20 nm), as the signals can become convoluted, making it difficult to discern specific elements. Furthermore, these methods are both time-intensive and costly, which may limit their accessibility and frequency of use in routine analyses.

Regarding noninvasive means of metrology, atomic force microscopy (AFM)-based techniques can also be valuable tools in evaluating the tolerance of ETLs to bombardment during PVD of TCOs. A notable study by Ying et al.[27] highlights this application, demonstrating that ST-PSCs incorporating a

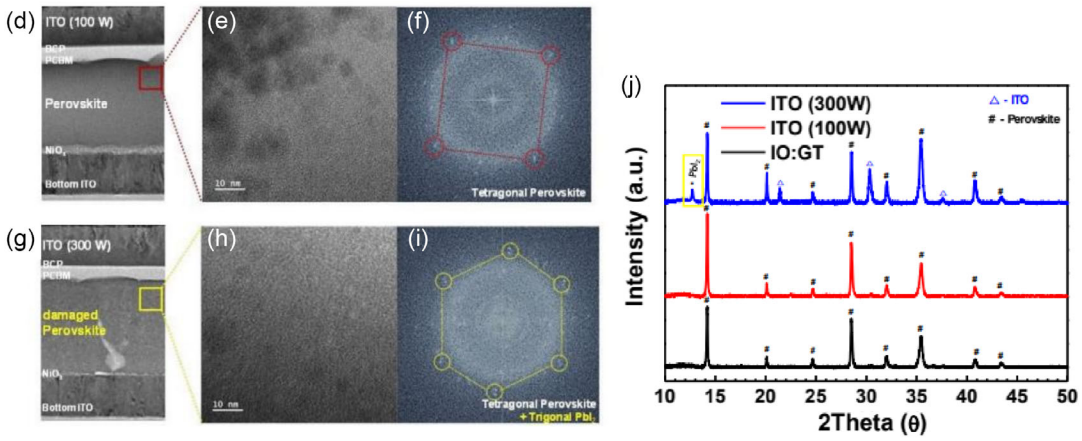

Figure 5. Cross-sectional HRTEM images of the ST-PSC featuring ITO deposited at 100 and 300 W. Detailed HRTEM images from the designated square regions for d) ITO (100 W) and g) ITO (300 W) samples. Corresponding fast Fourier transformation patterns for e) ITO (100 W) and h) ITO (300 W) samples are also presented. j) XRD patterns of ST-PSC including IO:GT, alongside low-power ITO (100 W) and high-power ITO (300 W) samples. Reprinted with permission.[26] Copyright 2022, Wiley-VCH.

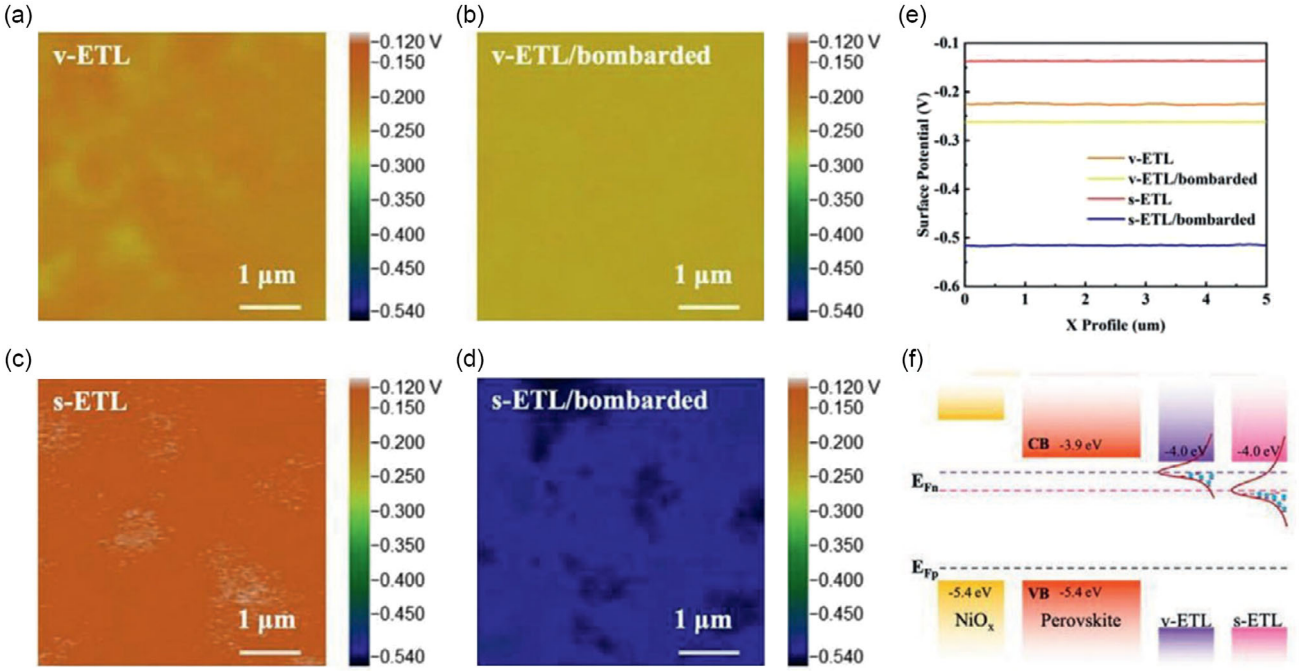

Figure 6. Surface potential mapping conducted using a Kelvin probe coupled with AFM. a) v-ETL before bombardment, b) v-ETL after bombardment, c) s-ETL before bombardment, and d) s-ETL after bombardment. e) Comparative surface potential profiles derived from the aforementioned four images. f) Schematic energy-level diagrams of PSCs incorporating s-ETL and v-ETL. Reprinted with permission.[27] Copyright 2021, Wiley-VCH.

vacuum-evaporated C_{60}/bathocuproine (BCP) stack, referred to as v-ETL, significantly outperform their counterparts with solution-processed ETL (s-ETL). This performance discrepancy is further explored through an investigation into the surface potential differences at the ETL/ITO interface, utilizing Kelvin probe measurements to elucidate the underlying mechanisms. Initially, s-ETL exhibits a higher surface potential (−137.05 mV) compared to v-ETL (−225.33 mV), correlating with the higher open-circuit voltage (V_{oc}) in s-ETL-based devices due to a lower work function. Post-IZO bombardment, both ETLs experience a decrease in surface potential, with s-ETL showing a substantial negative shift (−515.32 mV) indicative of bombardment-induced defect states that alter the surface energy significantly more than in v-ETL. This alteration leads to charge redistribution and band realignment at the IZO/ETL interface, with the generated defects and traps exacerbating device performance degradation through intensified interfacial recombination, as evidenced by the FF in the *J*–*V* curve. The study concludes that the observed shift in surface potential due to differential tolerance to IZO sputtering bombardment is the primary factor behind the performance variance between v-ETL and s-ETL devices (**Figure 6**).

4. Overview of Buffer-Free Semitransparent Perovskite Solar Cells with TCOs by PVD

Our perspective lists all identified studies on buffer-free ST-PSCs with transparent oxide electrodes by PVD. Buffer-free PSCs are developing in line with the overall progress of the field, while developing new approaches. The analysis of the collected data reveals an approximately equal distribution between n–*i*–p and p–*i*–n device architectures. Notably, there has been a shift toward p–*i*–n architectures, potentially because this configuration is increasingly used for tandem applications. In contrast, initial investigations into buffer-free devices, such as those by Fu et al.[28] and Werner et al.[21] in 2015, primarily focused on n–*i*–p devices and highlighted the critical role of MoO_x to mitigate PVD-induced damage rather than concentrating on buffer-free device advancements per se. The research has experienced a rise in scholarly interest and output from 2021, reflecting a growing consensus on the importance and potential of buffer-free ST-PSCs.

Regarding the TCO materials employed, indium oxide has been exclusively used, with indium tin oxide (ITO) being the most common, featured in 11 applications. IZO has been utilized in three instances, while the remaining applications have explored alternative doping elements (H, Zr, codoping with Ga and Ti, or W) for indium oxide. The demand on indium-based TCOs stems from their high charge mobility, which facilitates optimized electrical properties, as well as transparency in the infrared (IR) region. Furthermore, the selection is significantly limited by the thermal sensitivity of most perovskite top cell configurations, which cannot withstand annealing at temperatures exceeding 100 °C for prolonged periods without undergoing thermal degradation.

The main parameters of the buffer-free solar cells, as detailed in **Table 1**, are graphically represented in **Figure 7**. This representation categorizes devices by their transport layer and device polarity, with a dashed line distinguishing between n–*i*–p and p–*i*–n devices. Various PVD fabrication methods, each denoted

Table 1. Summary of ST-PSCs with TCO deposited directly on CTLs reported in literature. Device parameters are reported with illumination from the glass side of ST-PSCs. Additional information and data with illumination from the top TCO side is provided in Table S1, Supporting Information.

Year	TCO	Deposition	Architecture	CTL class	PCE [%]	J_{sc} [mA cm^{-2}]	V_{oc} [V]	FF [%]	Cell area [cm^2]	PCE_{opaque}	PCE ratio	References
2015	IO:H	RF[a)]	n–*i*–p	Spiro	10.1	16.6	1.03	59	0.3	14.5	0.70	[28]
2017	ITO	MS	n–*i*–p	Spiro	14.2	20.1	0.972	72	0.13	15.8	0.90	[44]
–	–	–	–	–	12	18.2	0.914	72	4	13	0.92	[44]
2018	ITO	RF	n–*i*–p	Spiro	15.7	19.94	1.071	73.4	0.16[c)]	19.7	0.78	[45]
–	–	–	–	–	15.43	21.32	1.07	67.6	0.64[d)]	–	–	[45]
2018	IZO	DC	p–*i*–n	PCBM/BCP	13.3	18.4	1.071	67.4	0.135	15.4	0.86	[46]
2019	ITO	DC	n–*i*–p	Spiro	14.6	17.3	1.167	73	0.25	–	–	[47]
2019	ITO	DC	n–*i*–p	CuSCN	14.2	20.2	0.978	72.1	0.16[c)]	–	–	[48]
2020	ITO	RF	n–*i*–p	PTAA	12.6	19.85	1.12	56.7	1.44[c)]	18.6	0.68	[49]
2021	ITO	DC	n–*i*–p	Spiro	13.12	18.11	1.05	68.9	0.09	14.83	0.88	[24]
–	–	–	–	–	9.5	2.28	7.4	56.4	21	–	–	[24]
2021	IZO	RF	p–*i*–n	C_{60}/BCP	15.83	21.29	1.001	74.3	0.1	18.71	0.85	[27]
2021	IZrO	PLD	p–*i*–n	C_{60}/BCP	15.1	21.2	1.05	68	0.09	19.8	0.76	[50]
2022	ITO	DC	n–*i*–p	Spiro	17.5	21.4	1.11	73.5	0.14	20.4	0.86	[11]
	IO:GT	LFTS	p–*i*–n	PCBM/BCP	17.8	19.27	1.12	82.6	0.04	19.6	0.91	[26]
2022	ITO	PLD	p–*i*–n	C_{60}/BCP	14	20.75	1.105	65	0.082[e)]	19	0.74	[23]
–	–	–	–	–	17.5	21	1.11	78	0.082[e)]	19	0.92	[23]
2022	ITO	MS	n–*i*–p	NiO_x	18.02	23.27	1.08	71.69	–	19.17	0.94	[25]
–	–	–	–	–	19.48	23.33	1.08	77.28	–	19.17	1.02	[25]
2023	IZO	RF	p–*i*–n	C_{60}	14.17[b)]	16.19	1.18	74.11	1.1	–	–	[10]
2023	ITO	MS	p–*i*–n	C_{60}/BCP	10.7	19.9; 156[g)]	0.98; 91.2[h)]	58.5	781F	11.65	0.92	[31]
2023	IZO	RF	p–*i*–n	C_{60}	12	18.2	1.016	65	0.12	12	1.00	[29]
2023	IWO	RPD	n–*i*–p	Spiro	16.5	21.7	1.05	75	0.04	16.4	1.01	[39]
2024	ITO	IBS	p–*i*–n	C_{60}	12.65[f)]	18.25[f)]	0.906[f)]	69[f)]	1.6	–	–	[30]
2024	IO:H	DC	p–*i*–n	PCBM/BCP	18.4	20.8	1.16	75.9	0.5	19.1	0.96	[51]

[a)]Off-axis RF sputtering; [b)]Values measured under illumination from top TCO side; [c)]Illuminated area is 0.09 cm^2; [d)]Illuminated area is 0.25 cm^2; [e)]Illuminated area is 0.05 cm^2; [f)]Champion PCE, best V_{oc}, J_{sc}, FF values as reported; [g)]Current (mA) of the module; [h)]Parameter presented for the module.

List of abbreviations: spiro, spiro-OMeTAD; ITO, Sn-doped indium oxide (In_2O_3); IZO, indium zinc oxide; IO:H, hydrogenated indium oxide; IZrO, Zr-doped (In_2O_3); IO:GT, gallium and titanium codoped (In_2O_3); IWO, W-doped (In_2O_3); MS, magnetron sputtering; DC and RF, direct current and radio frequency magnetron sputtering, respectively; PLD, pulsed laser deposition; LFTS, linear face target sputtering; RPD, reactive plasma deposition; IBS, ion beam sputtering.

by unique symbols, are fully described in the inset of Figure 7d. MS, whether in a direct current (DC) or RF configuration, emerges as the most prevalent PVD technique. However, a selection of alternative PVD methods, including PLD, linear face target sputtering (LFTS), remote plasma deposition, and IBS, has also been successfully employed for the "soft" deposition of TCO layers, as detailed in Table 1. Interestingly, no single-deposition technique has been identified as superior for fabricating these PSCs; instead, performance seems to hinge more on specific conditions rather than the deposition method itself. Similarly, there is no definitive best choice for the CTLs; various CTLs have been shown to yield favorable results, suggesting that performance is not inherently limited to any specific CTL selection.

In this context, the term "buffer free" is applied to devices that do not incorporate additional layers beyond what is typically found in a reference single-junction process, generally referring to a single ETL or HTL. Notably, certain ETL configurations comprising two layers (e.g., a fullerene derivative like C_{60}/PCBM with an additional BCP layer or a ≈3 nm-thick PEIE layer) are still considered buffer free. This classification is due to the belief that such thin layers (<15 nm) are insufficient to counteract PVD-induced damage. Conversely, double-layer ETLs incorporating a metal oxide layer (e.g., PCBM/ZnO nanoparticles) are excluded from our buffer-free device categorization. Adhering to a stricter definition that includes only single-layer ETLs reduces the count to two very recent successful buffer-free p–*i*–n devices with TCO directly deposited on C_{60}.[29,30]

Four various HTLs have demonstrated resilience to the bombardment associated with subsequent PVD of TCO. The majority of research on n–*i*–p structures has utilized spiro-OMeTAD as the HTL, which also represents the most significant contribution across both device polarities. Alternatively, other organic semiconductors, such as poly(triaryl amine) (PTAA), have been

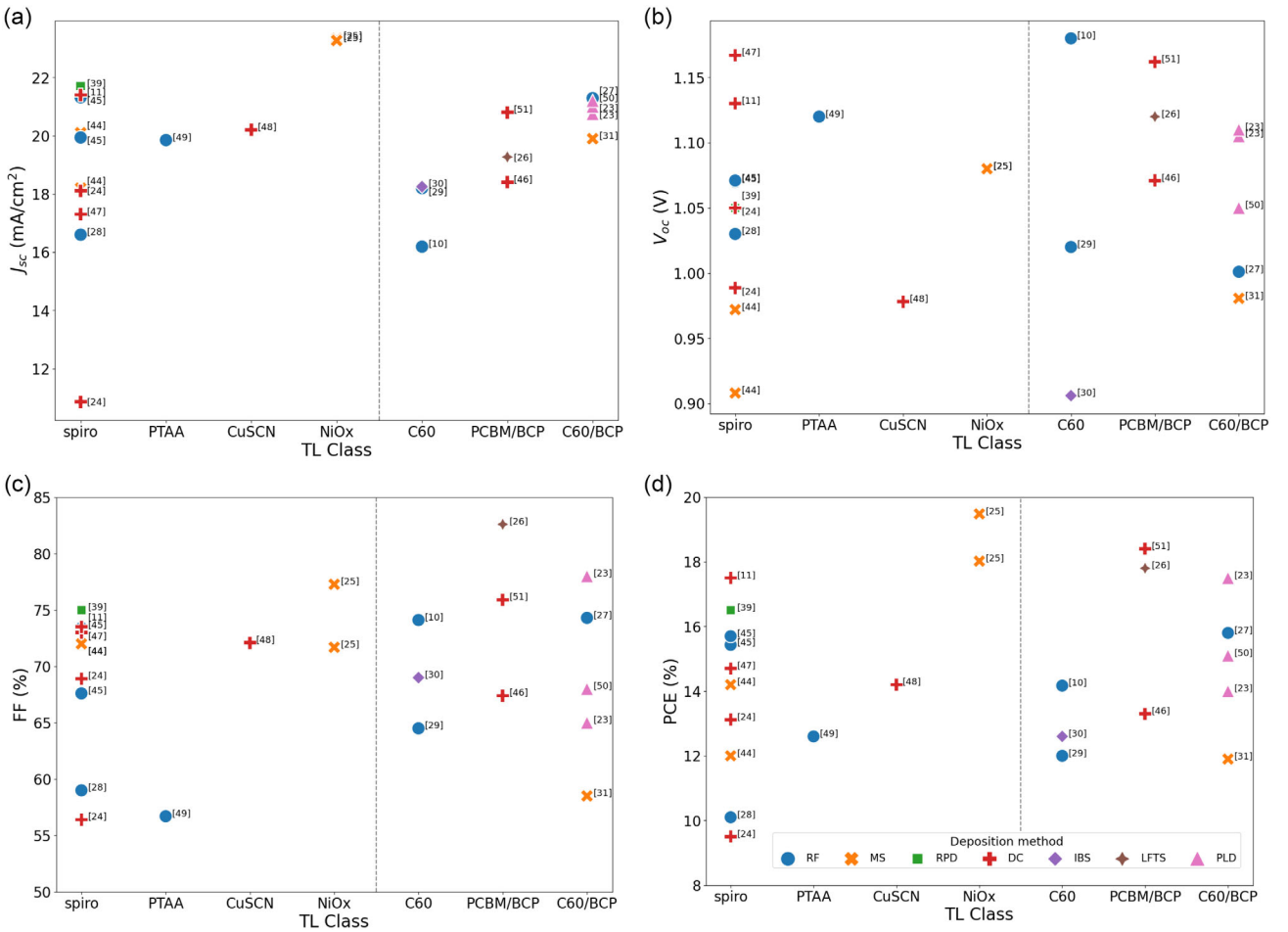

Figure 7. Solar cell parameters of reported buffer-free semitransparent perovskite devices with the corresponding transport layers beneath "soft" TCO deposition. a) short-circuit current density (J_{sc}), b) open-circuit voltage (V_{oc}), c) FF, d) PCE. List of abbreviations: spiro, spiro-OMeTAD; ITO, Sn-doped indium oxide (In_2O_3); IZO, indium zinc oxide; IO:H, hydrogenated indium oxide; IZrO, Zr-doped (In_2O_3); IO:GT, gallium and titanium codoped (In_2O_3); IWO, W doped (In_2O_3); MS, magnetron sputtering; DC and RF, direct current and radio frequency; magnetron sputtering, respectively; PLD, pulsed laser deposition; LFTS, linear face target sputtering; RPD, reactive plasma deposition; IBS, ion beam sputtering.

explored as HTLs in specific studies. Research on inorganic layers like CuSCN and NiO_x HTLs is limited, with only one study reported for each material so far, underscoring the urgent need for expanded investigation into these cost-effective and, possibly, more stable options.

Furthermore, it is important to note that improvements in PCE and stability, largely due to advances in absorber materials, imply that PCE metrics alone are not fully indicative of device performance, given their strong dependence on the properties of the absorber layer. Moreover, pursuing enhanced efficiency may not always be the primary objective of the study, especially for semitransparent cells where a balance between efficiency and transparency is sought. A more revealing metric could be the efficiency ratio between semitransparent and opaque devices, offering a clearer context for efficiency comparisons, albeit with limited statistical data and not universally reported across studies. The efficiency ratio (between semitransparent and opaque cells) is considered and indicated in Table 1 and **Figure 8**a.

Common expectations would predict a lower short-circuit current density (J_{sc}) for semitransparent cells due to the absence of a traditional electrode and potentially compromised FF due to the higher resistance associated with TCOs compared to metal grids making the efficiency ratio <1. Remarkably, one study[25] has reported this efficiency ratio that surpasses the threshold of 1 (as seen in Figure 8a). The study attributes this enhanced performance to the improved alignment of work functions between the TCO and NiO_x. This alignment facilitates more efficient charge carrier extraction, thereby compensating for the anticipated losses in J_{sc} and FF. In the rest of the surveyed literature, efficiency ratios are reported to lie between 0.70 and 0.95, with spiro-OMeTAD exhibiting the uppermost efficiency values within this range. The enhanced performance of spiro-OMeTAD can be partly attributed to its generally sufficient layer thickne ss, which functions beneficially as a buffer layer on its own. Nonetheless, the application of this HTL in the scaling up of ST-PSCs is impeded by its exorbitant cost and low stability.

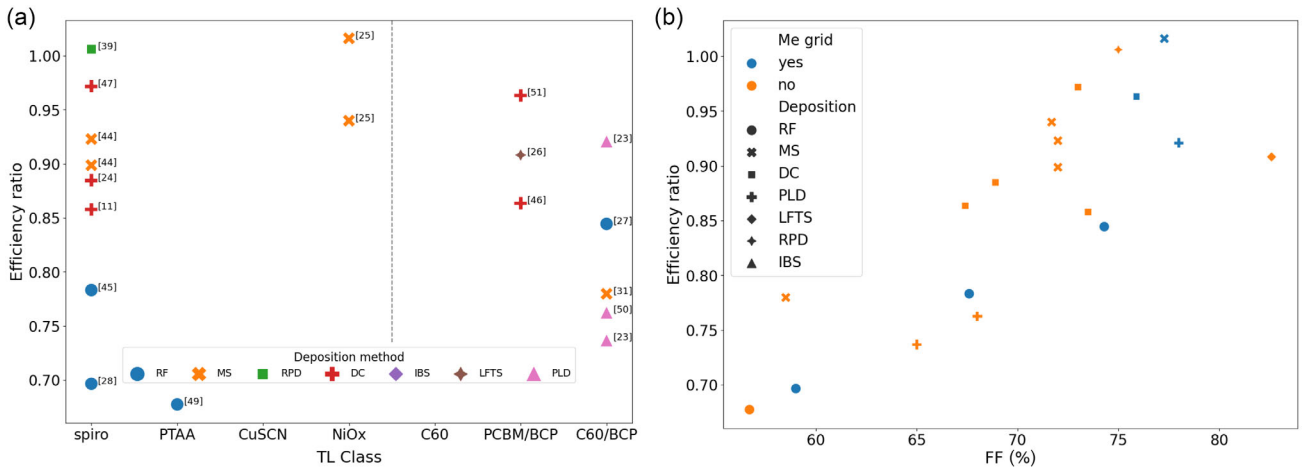

Figure 8. Efficiency ratio of ST-PSCs versus respective opaque devices with identical stacks. a) Displayed with respect to the corresponding transport layers beneath "softly" deposited TCOs. b) Displayed as a function of FF of the semitransparent device. Cells with additional metal grid shown with blue symbols.

Among the main solar cell parameters, FF may offer more profound insights compared to the J_{sc} and V_{sc}, which are heavily reliant on the absorber characteristics. Addressing the issue of FF values, it is important to note a possible room for inconsistency caused by the use of a metallic grid outside the aperture cell area. Any inconsistency in reporting can lead to misleading interpretations of the device efficiency. The incorporation of a metallic grid is known to mitigate the limitations imposed by the R_{sh} of TCO, generally leading to an enhancement in efficiency. For a comprehensive understanding, it would be ideal for studies to report results both with and without the grid, allowing for a clear differentiation of losses attributable to plasma damage from those due to increased series resistance. Despite these complexities, a consistent trend emerges as displayed in Figure 8b: the ratio of PCE is predominantly influenced by FF in samples, regardless of whether they incorporate a grid. This observation underscores the critical role of FF in determining the overall efficiency of PSCs and highlights the importance of optimizing interfacial work function alignment and mitigating series resistance to enhance device performance.

5. Scalability and Stability of Buffer-Free ST-PSC Devices

While scaling up the fabrication of perovskite solar modules is essential for their commercialization, current research predominantly focuses on optimizing small-scale cells, whereas commercial viability depends on capabilities to produce large-area modules. **Figure 9**a demonstrates the PCE trends of cutting-edge buffer-free single-junction PSCs, presenting a correlation between increased cell size and decreased PCE. This trend highlights a prevalent research emphasis on small, laboratory-scale "pixel" devices, further evidenced by the fact that to this point, merely a couple of studies have explored the fabrication of perovskite modules larger than 10 cm^2 that are discussed below.

Rai et al.[24] demonstrated significant progress in the development of large-area semitransparent perovskite-based devices. They presented a buffer-free ST-PSC module with an area of 21 cm^2 (Figure 9b). In an attempt to address the inherent challenges of upscaling, they introduced a series-connected minimodule design aimed at optimizing performance. However, the process of upscaling presents considerable obstacles. One of the primary challenges in scaling up involves the deposition techniques used for the perovskite absorber and HTL, specifically spiro-OMeTAD. These materials are still applied using spin coating, a method that, while effective for small-scale laboratory experiments, is not well-suited for large-scale manufacturing due to its limitations in uniformity over large areas and significant solvent waste. The consequences of upscaling are notably reflected in the efficiency metrics, with a significant reduction in performance observed as the module size increases. Specifically, the PCE experiences a marked decrease from 13.1% in a small 0.09 cm^2 cell to 9.2% in the 21 cm^2 module.

On a larger scale, a report by Merckx et al.[31] stands out as the closest example to full-size module production, achieving a module area of 781 cm^2 (Figure 9c). This significant advancement leverages upscalable fabrication techniques, including slot die deposition for the perovskite layer and a "soft sputtering" process for applying the ITO layer atop a C_{60}/BCP stack. While the specific efficiency loss related to upscaling in ST-PSCs is not detailed, monofacial modules from the same study[31] exhibit a decrease of ≈1.7% efficiency, from 14.8% in a 4 cm^2 cell to 13.1% in a 784 cm^2 module (aperture efficiency). Additionally, in the same work, the thermal stability of perovskite modules was reported by testing unencapsulated minimodules, each 4 cm^2 in size, under conditions of elevated temperature (≈85 °C) in a nitrogen atmosphere. The best-performing minimodule achieved a T_{80} (time to retain 80% of initial performance) of roughly 5000 h. Further stability assessment through damp heat testing (85 °C, 85% RH) on encapsulated minimodules showed that encapsulation effectively safeguards the modules,

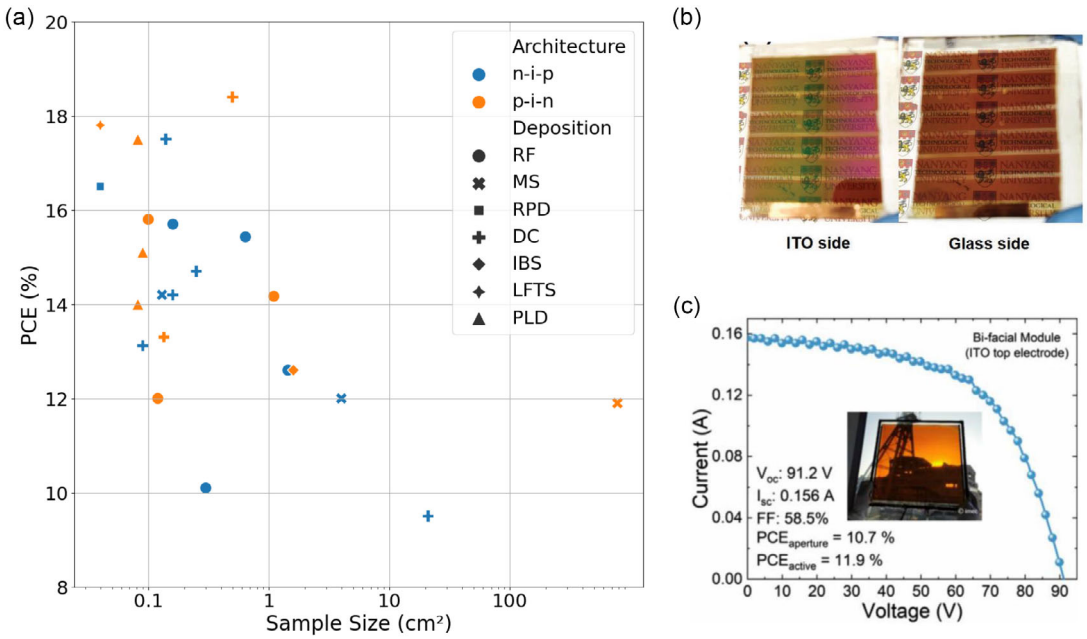

Figure 9. a) PCEs of reported buffer-free semitransparent perovskite devices as a function of device area. b) Image of 21 cm^2 semitransparent n–i–p module with ITO sputtered on spiro-OMeTAD. Reprinted with permission.[24] Copyright 2021, Wiley-VCH. c) Image and corresponding *J–V* curve of 781 cm^2 of p–*i*–n module with ITO sputtered on C_{60}/BCP. Reprinted with permission.[31] Copyright 2023, IEEE Electron Devices Society.

with devices retaining about 92% of their initial PCE after 1000 h. However, it is noteworthy that these stability assessments were limited to buffer-free modules. The study by Rai et al.[24] also delves into operational stability but focuses on smaller cells rather than the 21 cm^2 minimodule. Through maximum power point tracking testing under standard conditions (1 Sun illumination, room temperature, RH of 40–50%), they compared the durability of ST-PSCs with an ITO electrode against opaque devices with an Au electrode. The ITO-based devices turned out to be more stable, maintaining around 80% of their initial PCE for ≈300 h, in stark contrast to the rapid degradation of Au-based devices within a day, likely due to Au diffusion under continuous light exposure.[32] The most insightful studies for advancing durable and efficient large-area PSCs would ideally compare stability across devices both with and without buffer layers. However, the current body of work often focuses on comparisons between opaque and semitransparent devices (**Figure 10**) or exclusively examines buffer-less devices. This highlights several critical challenges in the field, including the scarcity of research on large-module development, the diversity of methodologies used to assess stability (such as operational, dark storage, and temperature tests), and the varied approaches to comparing device stability across different device configurations. The challenge remains to standardize stability assessment methods and to broaden the scope of research to include a wider range of device configurations and module sizes.

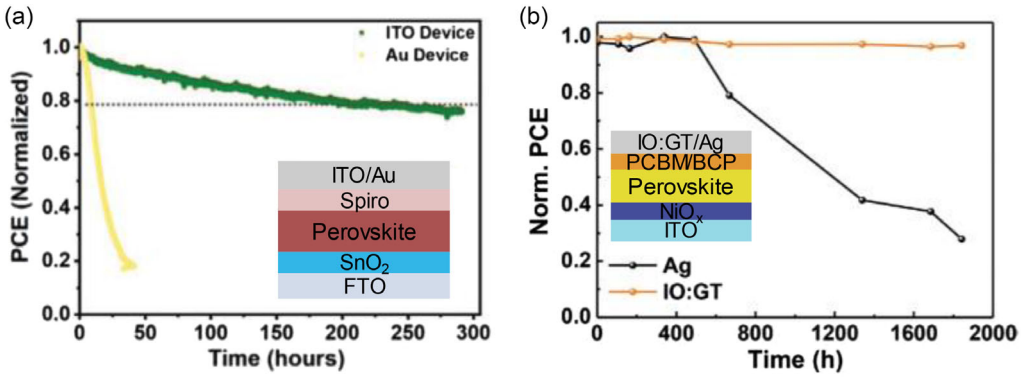

Figure 10. a) Efficiency tracked at maximum power point under continuous illumination in ambient condition with controlled humidity (40–50%). Reprinted with permission.[24] Copyright 2021, Wiley-VCH. b) Normalized PCE stability characteristics for unencapsulated opaque PSC with an Ag cathode and for ST-PSCs with an IO:GT cathode. Devices stored and measured in an atmosphere with a relative humidity of 40–60%. Reprinted with permission.[26] Copyright 2022, Wiley-VCH. Cross sections of respective devices are displayed in insets.

In the context of directly comparing buffered versus buffer-free cells, there are very few studies that offer this specific analysis. One such example is provided by Nakamura et al.[11] who evaluated their performance against cells incorporating a MoO_x buffer layer. Initially, both types of cells showed similar performance, with PCEs of 17.5%. The study found that the buffer-free cell allowed for ≈8% higher near-infrared transmittance, which could potentially enhance the performance of tandem solar cells. Stability tests conducted at 85 °C revealed that cells with the MoO_x buffer layer degraded significantly faster, retaining only 20% of their initial PCE after 6 h, in contrast to the buffer-free cells which maintained 80% of their initial PCE. Despite the rapid degradation of buffer free (and even faster in devices with MoO_x), Nakamura et al. believed that stability can be improved through the use of passivating agents and/or device encapsulation.

In a related study, in a Ph.D. thesis, Härtel[33] presented a comparative analysis of Si/halide perovskite tandem devices with and without the buffer layer beneath TCO. This analysis specifically contrasts devices with identical stacks that differ solely in their ETLs, comparing C_{60}/SnO_2 with C_{60}/PEIE configurations (the latter, at 3 nm thickness, we still consider as buffer-free; refer to the beginning of this section for details). Given that the top ST-PSC is anticipated to be the performance-limiting factor, this comparison is particularly relevant to our review. The C_{60}/SnO_2 tandem devices exhibited a gradual decline in efficiency over time (as shown in **Figure 11**), a trend attributed to the inherent stability characteristics of the solar cell stack. On the other hand, the C_{60}/PEIE devices did not follow a similar pattern of efficiency decline. However, the observations for these devices were complicated by measurement inconsistencies and were ultimately cut short due to technical difficulties related to contacting, leaving a gap in the data that prevents a direct and fair comparison of long-term stability between the two configurations. Nevertheless, the preliminary results suggest that omitting the SnO_2 buffer layer, provided that there is proper optimization of the transparent conductive oxide (TCO) deposition, does not compromise—and may even enhance—the long-term stability of PSCs. These findings indicate that the stability issue stems from certain types of carrier transport layers, suggesting that buffer-free devices could contribute to an enhanced device lifetime in the future. Given the importance of this aspect and the existing gap in stability reports, it requires significantly more thorough investigation.

6. Guidelines for "soft" Physical Vapor Deposition Process Optimization

As demonstrated in Section 3, the tolerance of various CTLs to the PVD of TCOs varies signific antly, influenced by both the choice of CTLs and their fabrication methods. This section will offer guidelines aimed at achieving "soft" deposition practices, facilitating the development of buffer-free ST-PSC. It was highlighted that substrate bombardment by high-energy particles plays a crucial role in contributing to plasma damage during the PVD process. There are several indicators, including in situ

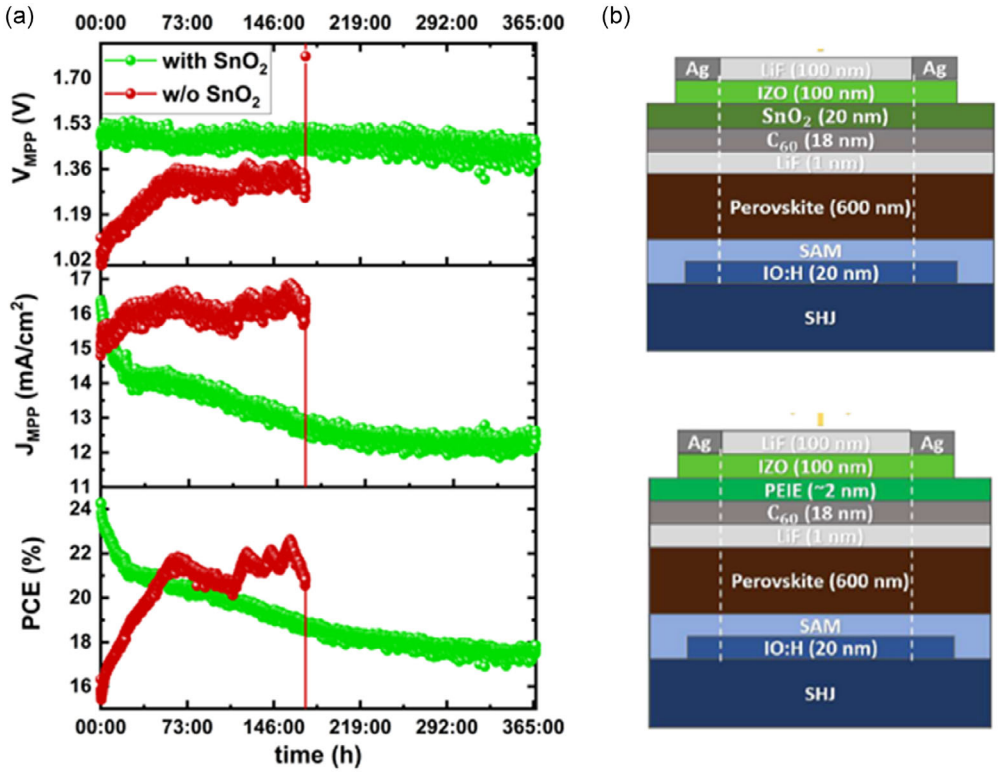

Figure 11. a) Comparison of voltage, current, and PCE tracked at MPP over time (in hours), for tandem devices featuring a 20 nm SnO_2 buffer layer (green) against those without it (w/o SnO_2 refers to devices where thin PEIE interlayer was used instead of SnO_2). b) Cross section of tandem devices under stability examination: top cell includes SnO_2 buffer layer, whereas bottom does not. Reprinted with permission from the author.

options available at the deposition tool, that can monitor these contributing factors. One primary indicator is the voltage difference between the target and the chamber, which provides an estimate of the energy levels of the species arriving at the substrate.

Although this may not yield precise numerical values, target voltage offers a qualitative understanding of how changes in process parameters relate to variations in target voltage. For instance, a study illustrated the dependency of target voltage on pressure at a constant power of 60 W during ITO deposition, as shown in **Figure 12**a. It has been observed that the least damage occurs with ITO sputtering on a CuO_x/PTAA stack at voltages below 280 V for DC sputtering.[19] Similarly, for IZO deposition by RF-MS atop C_{60}, sputtering at voltages below 150 V resulted in no damage.[10] Fabrication processes for TCOs that result in target voltages above these values cause degradation of solar cell performance, as shown in the respective studies. It is important to note that while target voltage serves as an easily attainable indirect indicator of overall PVD process energetics, the critical factor is the energy of the arriving species on the substrate. Although target voltage is indicative of the target energy and related to the particle energy arriving on the substrate, identical target voltages may result in different energies on the substrates due to variations in parameters such as the target-to-substrate distance and deposition pressure. Monitoring the particle energy on the substrates requires using techniques such as the Langmuir probe method, although there are currently no reports available on this in relation to PSCs.

Nevertheless, the trends in target voltage behavior align with the discussion on thermalization distance, suggesting that both increasing the pressure and reducing the energy of plasma particles can aid in thermalization, while also leading to a decrease in target voltage. Therefore, physically increasing the separation between the target and substrate (TS distance) has been suggested to be beneficial. While there is limited data focusing on the correlation of TS distance and target voltage, reports have indicated a positive effect of larger TS distances on overall device performance and reduced damage at the TCO/CTL interfaces, particularly in the context of DC[24] sputtering and LFTS.[34]

In addition to ion bombardment, plasma UV luminescence and heating during deposition further contribute to substrate damage. Implementing plasma diagnostics, such as emission spectroscopy, can be instrumental in identifying these effects. For example, Reddy et al.[14] observed that increasing the sputtering power (Figure 12b) led to the emergence of additional UV luminescence-related peaks ($\lambda \approx 335$ nm), with cells subjected to these conditions exhibiting more pronounced degradation.

Regarding the thermal effects of the sputtering process, even depositions carried out at nominally room temperatures can significantly overheat the cell due to the high energies of the particles involved. This phenomenon can be monitored using thermal stickers, as demonstrated in a study where ITO sputtering resulted in temperatures exceeding 60 °C (Figure 12c), conditions found to be suboptimal and leading to degraded PSC performance compared to isolated plasma deposition, which did not alter the substrate temperature significantly from ambient conditions. Drawing from these insights, alongside the recommended diagnostic tools, we propose modifications to the PVD process aimed at achieving a "softer" deposition approach to mitigate substrate damage and enhance performance of PSCs: 1) Lower the sputter power, which can be indirectly tracked by monitoring the target voltage; 2) Increase the target-to-substrate distance to promote thermalization through enhanced particle collisions; 3) Increase the process gas pressure to lower the mean free path, resulting in target particles thermalizing due to the loss of kinetic energy; and 4) Avoid the target surface directly facing the substrate.

It is important to note that a conventional reference process for TCO/glass would probably be overly aggressive to be directly applied atop of organic CTL. The optimal parameters, including TS distance and target voltage, will vary based on the specific characteristics of the PVD system, such as power source type, tool geometry, and target material composition (metallic or ceramic). The provided guidelines are intentionally broad due to the variability in equipment and materials; exact specifications should be empirically determined.

Moreover, it is crucial to acknowledge that excessively high gas pressures (generally, above 10 mbar) could yield films with suboptimal density. Additionally, there is a lower limit of power below which sustaining a plasma discharge becomes unfeasible. While these guidelines offer a foundational approach for initial optimization, the TCO PVD process development should be carried out in coordination with the adjacent layers following characterization approaches as previously discussed in detail in Section 3.

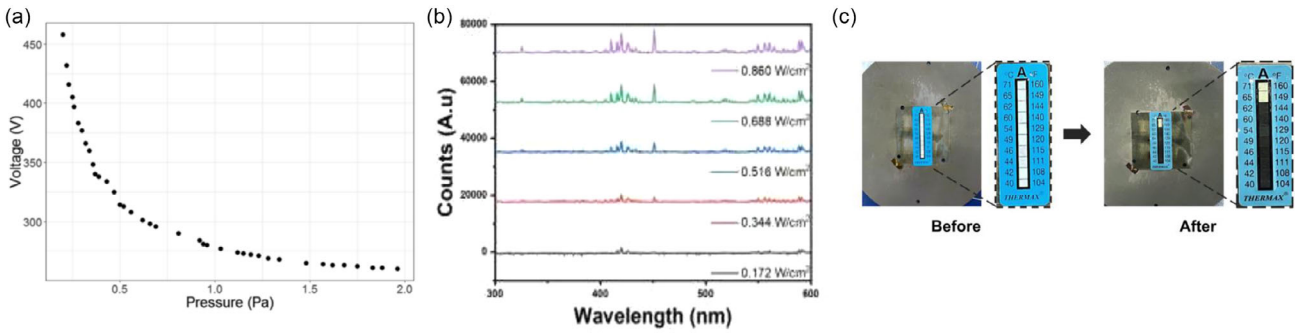

Figure 12. a) Voltage across target and chamber during ITO sputtering at 60 W (4.4 W cm^{-2}) at different pressures. Reprinted with permission.[19] Copyright 2020, American Chemical Society. b) Plasma spectrum during ITO sputtering. With the increase of power, extra UV luminescence-related peaks ($\lambda = 335$ nm) appear. Reprinted with permission.[14] Copyright 2022, American Chemical Society. c) Differences before and after the deposition of an ITO film using the MS process on the thermal strip. Reprinted with permission.[43] Copyright 2023, Elsevier.

7. Summary of Developments Need and Outlook

The exploration of buffer-free ST-PSC benefits significantly from the broader advancements within the PSC domain, yet it presents distinct advantages and challenges. The successful direct integration of TCOs onto CTLs represents a critical breakthrough in PSC fabrication, substantially simplifying the manufacturing process. Nonetheless, current leading semitransparent devices, particularly those used in tandem configurations, still necessitate a buffer layer.

Consequently, there is a need for increased focus on overcoming these challenges. We outline a summarized set of development needs for the soft PVD of TCOs to enhance the efficiency of ST-PSCs: 1) Systematically determine the deposition conditions (e.g., target voltages, gas pressures, power densities) enabling fabrication of efficient buffer-free devices; 2) Explore different PVD techniques and modifications to existing sputtering equipment to minimize damage from PVD to delicate layers, such as adopting gas flow sputtering and investigating indirect/remote plasma deposition methods. Among the reviewed PVD methods, DC sputtering is particularly relevant as it is the most established and cost-effective technology. Additionally, reactive sputtering from metallic targets may be industrially advantageous[35] as it enables better target utilization and potential cost savings due to cheaper targets. This aspect of research, which is crucial for commercialization, is significantly underrepresented; and 3) Investigate strategies to reduce indium usage. This can be achieved by selecting entirely indium-free material systems, such as Al-doped ZnO, or by exploring alternative device designs. Recent developments in Si heterojunction cells[36] have demonstrated significant reductions in indium usage, despite traditionally relying on indium-based front TCOs for both TE and antireflecting function. Adapting similar approaches could lead to more sustainable and cost-effective solutions in the fabrication of PSCs.

As another option, correlated metals[37] with high carrier density and strongly correlated electron effects provide a different route to achieve transparent conducting materials, different from the conventional degenerately doped wide-bandgap TCOs. However, most of the 4*d* correlated metals are grown epitaxially on single-crystal substrates. There have been attempts to grow high-quality $SrMoO_3$ films on fused silica substrates,[38] overcoming the use of expensive and size-limited single-crystal substrates. However, these films still require high-temperature growth, making them currently impractical for commercialization. This area could be worth further investigation.

From a more fundamental research perspective, we identified the following unresolved questions: 1) The influence of the surface morphology of the underlying layer on the performance and quality of the deposited film and subsequent solar cells is yet to be fully understood; and 2) The effect of the oxygen level during the deposition process and its potential for oxidizing the CTL beneath remains an open question.

Based on our research, despite the known instability of many perovskite compositions in the presence of air and moisture, depositing TCO in the presence of O_2 during PVD does not deteriorate solar cell performance. All the studies listed in Table 1 utilized ceramic indium oxide-based targets. While it is sometimes possible to form an oxide film in a pure argon environment with ceramic targets, the addition of small amounts (1–5 vol%) of O_2 is often necessary to achieve the required optoelectrical properties of thin films. Information on whether O_2 reactive gas was added for TCO deposition can be found in Table S1 (Supporting Information). There is no consensus in the community regarding the optimal oxygen levels during TCO deposition. For instance, Hartel et al.[10] and Clausing et al.[29] both independently reported damage-free deposition of IZO atop C_{60}. However, the former group obtained the best results by adding O_2 to the reactive MS process, while the latter group deliberately used an O_2-free process to suppress possible oxidation. Additionally, oxygen tolerance greatly depends on the transport layer below. For example, higher O_2 flux during IWO deposition was found to be effective in reducing the contact resistance of IWO/Spiro-OMeTAD, improving the PCE of the final device.[39] Therefore, more studies are encouraged to be dedicated toward this subject.

Overall, the focus on refining the "soft" PVD process to reduce substrate damage holds the key to unlocking significant improvements in the efficiency and scalability of buffer-free ST-PSCs. Additionally, when TCOs are properly optimized, they contribute to the enhancement of device stability. This is a significant improvement, offering stability advantages even over conventional ETL/noble metal configurations for single-junction PSCs.[14] Such advancements and fabrication process simplifications are particularly relevant as they may address similar challenges faced in the development of perovskite-based tandem cells, bifacial perovskite cells, and all-perovskite tandem cells,[40,41] indicating the onset of further breakthroughs in perovskite photovoltaic technology.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

perovskite solar cells, physical vapor depositions, transparent conducting oxides

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