

ECE Capstone Project Final Report

Project Title	Design and Implementation of a NOMA-Enabled Communication System
Team	Idris Kanyshuly - Hardware engineer Amir Karatay - NOMA RX design Aidana Kenzhebayeva - PCB manufacturing Yerboldy Sagijanov - NOMA TX design
Supervisor	Galymzhan Nauryzbayev
Course/Term	ENG 400 Capstone Project, 2026
Date	11-04-2026

Prepared by:

Idris Kanyshuly,
Amir Karatay,
Aidana Kenzhebayeva,
Yerboldy Sagijanov

Reviewed by: Galymzhan Nauryzbayev

TABLE OF CONTENTS

0. ABET Evidence Map, Final Design Snapshot, and Design Evolution Log.....	4
1. Executive Summary (1 page).....	9
2. Problem Definition, Stakeholders, Context, and Constraints (2–3 pages).....	11
2.3 Context and Operating Environment.....	12
2.4 Constraints and Context Factors.....	13
3. Final Requirements, Acceptance Criteria, and Traceability (2–3 pages).....	14
3.1 Final Requirements Compliance.....	14
3.2 Requirements Traceability.....	15
3.3 Derived, Interface, Environmental, and Regulatory Requirements.....	16
4. Engineering Standards, Regulations, and Compliance Evidence (1–2 pages).....	18
5. Concept Generation, Trade-off Study, and Selected Concept (3 - 4 pages).....	21
5.1 Candidate Concepts.....	21
5.2 Weighted Trade-off Study.....	23
5.3 Selected Concept and Rationale.....	24
6. Design Iterations and Decision History (1-2 pages).....	25
7. Final System Architecture (4-5 pages).....	27
Transmitter subsystem.....	28
Receiver subsystem.....	29
Integration philosophy.....	29
8. Detailed Design and Implementation (2–4 pages).....	31
8.1 Hardware design.....	31
8.2 Software / firmware design.....	37
Bit Sequencing and Sample-Rate Control.....	37
Carrier Generation.....	38
BPSK Modulation with Power Scaling.....	38
NOMA Superposition and DAC Output.....	39
Superimposed Signal Constellation.....	39
Receiver Implementation.....	39
Frame Synchronization.....	39
Amplitude Estimation.....	40
Stage 1: Direct Decoding (Far User).....	40
Stage 2: Successive Interference Cancellation (Near User).....	40
Error Propagation in SIC.....	41
BER Computation.....	41
End-to-End Pipeline Summary.....	42
Key Design Parameters.....	42
8.3 Prototype realization and integration.....	43

8.4 Final BOM and design-for-manufacture / assembly notes.....	46
9. Verification, Validation and Experimental Results (2-4 pages).....	49
10.1 Final Risk Register.....	57
10.3 Budget, Procurement, and Substitutions.....	59
11. Professional Responsibilities and Broader Impacts (2–3 pages).....	64
11.1 Public Health, Safety, and Welfare.....	64
11.2 Ethical and Professional Responsibilities.....	64
11.3 Security and Privacy.....	65
11.5 Environmental, Economic, Social, Global, and Cultural Factors.....	66
12. Team Organization, Collaboration, and Individual Contributions (2–3 pages).....	68
13. Use of Prior Course Work and New Knowledge Acquired (1–2 pages).....	71
14. Conclusions and Recommendations (1 page).....	73
15. References.....	74
Appendix A. Engineering Standards Evidence.....	77
Appendix B. Multiple-Constraints Matrix.....	80
Appendix C. Team Organization and Contributions.....	82
Appendix D. Design Evidence.....	86
Appendix E. Verification Evidence.....	90
Appendix F. Project Management Evidence.....	93

0. ABET Evidence Map, Final Design Snapshot, and Design Evolution Log

Table 0-A. Report Evidence Guide.

ABET item / SO	What must be demonstrated	Primary report section	Supporting appendix / evidence ID
<i>SO1</i>	Identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.	§2.1 Problem Definition: spectrum scarcity and Non-Orthogonal Multiple Access (NOMA) hardware gap identified and formulated; §5 Trade-off study: mathematical scoring of four multiple access schemes; §8.2 Software/firmware design: DDS carrier generation, fixed-point BPSK arithmetic, Successive Interference Cancellation (SIC) algorithm derivation; §8.1 Hardware design: 50 Ω microstrip impedance calculation, power budget, timing analysis	Table 5-A; Table 5-B; Figs 1-7; Figs. D1-D5; Figs. 11-14; Figs. E2-E4
<i>SO2</i>	Apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.	§3 Requirements and acceptance criteria: measurable Toll-like receptors (TLRs) mapped to verification; §5.3 Selected concept and rationale: trade-offs consciously accepted; §6 Design iterations: five documented iterations with evidence; §11 Professional responsibilities : safety controls, Industrial, Scientific, and Medical (ISM) band compliance, environmental and economic factors	Table 8-B; Table F-B; Table 9-B; Table 10-B; Table F-A; Table F-C
<i>SO3</i>	Communicate effectively with a range of audiences	§1 Executive summary: written for mixed technical and non-technical audience; §7 System architecture: block diagrams and interface tables; §8 Detailed design: schematics, pseudocode, and signal path descriptions; §9 Verification results: plots, tables, Bit Error Rate (BER) charts, and engineering judgment narrative	Figs. 1-2; Figs. 19-20; Fig. D6
<i>SO4</i>	Recognize ethical and professional responsibilities in	§11.1 Public health, safety, and welfare: hazard identification and controls; §11.2 Ethical and	Figs. 3-6; Fig. E4; Fig. 21; Table C-2; Table F-C

ABET item / SO	What must be demonstrated	Primary report section	Supporting appendix / evidence ID
	engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.	professional responsibilities: academic integrity, responsible AI use, dual-use considerations; §11.3 Security and privacy; §11.5 Environmental, economic, social, global, and cultural factors	
SO5	Function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.	§12 Team organization and contributions: roles, responsibility matrix, individual contribution log; §10.2 Milestones planned vs actual — task ownership and delivery evidence; §0 Design evolution log — team decisions documented with approvals	Table F-A; Table F-C; Table C-1
SO6	Develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.	§9 Verification and experimental results: 13-test campaign covering BER at three distances, SIC verification, throughput, antenna Vector Network Analyzer (VNA), spectrum; Table 9-A requirements-to-test matrix; Table 9-B test campaign summary with engineering judgment notes	Fig. 15; Fig. 20; Fig. D6
SO7	Acquire and apply new knowledge as needed, using appropriate learning strategies.	§13 Use of prior course work and new knowledge: Table 13-A (prior courses applied) and Table 13-B (new knowledge acquired); §8.1 Hardware design: IPC-2221 RF PCB design learned and applied; §8.2 Firmware design: Direct Digital Synthesis (DDS), fixed-point arithmetic, SIC algorithm; §8.3 Prototype realization:	Figs. E2-E4; Figs. 3-4; Fig. 6

ABET item / SO	What must be demonstrated	Primary report section	Supporting appendix / evidence ID
		EasyEDA, Quartus, GNU Radio, Python NumPy	
<i>Criterion 5 design evidence</i>	The culminating design shows standards, multiple constraints, iteration, and use of prior course work.	§4 Engineering standards: International Telecommunication Union (ITU) RR No. 5.150, Inter-Process Communication (IPC)-2221, International Electrotechnical Commission (IEC) 61010-1, International Mobile Telecommunications (IMT)-2020, IEEE 1800/1364 applied with clause-level justification; §2.4 Constraints matrix: eight quantified constraint categories; §6 Design iterations: five documented iterations (DE-01 through DE-05) with evidence of improvement; §13 Prior course work: digital systems, Radio Frequency (RF) theory, signals, PCB design all applied	Table A.1; Table 3-B; Table B.1; Figs. D1-D14

Table 0-B. Final Design Snapshot.

Field	Final value / summary
Final prototype / revision	Discrete Intermediate Frequency (IF) - based power-domain NOMA Transmitter (TX): DE1-SoC Field-Programmable Gate Array (FPGA) + custom two-layer PCB (AD9742 DAC, ADT1-1WT balun, LPF, HMC213 mixer, ADF4351 LO synthesizer, custom patch antenna). RX: USRP-2932 SDR + 10 dB Low-Noise Amplifier (LNA) + GNU Radio receiver (substituted for custom Receiver (RX) PCB per DE-04). Three prototype antennas at 2.426 GHz.
Main need addressed	Demonstrate a practical two-user NOMA prototype on hardware, including RF-FPGA integration challenges. Show the transparent academic NOMA hardware implementations in the literature.
Requirements met	All 6 requirements met. TLR-1: system throughput 6.125 Mbps (target ≥ 5 Mbps). TLR-2: far user BER = 3.06×10^{-4} (target $\leq$

Field	Final value / summary
	10^{-3}). TLR-3: near user BER = 10^{-6} (target $\leq 10^{-3}$). REQ-D1: working frequency 2.47 GHz within the stated ISM band. REQ-D6: FPGA and Analog-to-Digital Converter (ADC) and Digital-to-Analog Converters (DAC) components must be compatible with each other supporting 3.3V voltage level. REQ-D8: PCB design followed the IPC-2221 and DRC verification in the software .
Primary standards applied	ITU Radio Regulations Edition 2024, Article 5, Footnote No. 5.150 (ISM band allocation 2.400–2.4835 GHz); IPC-2221 Generic Standard on PCB Design (conductor width, RF routing, grounding); IEC 61010-1:2010+AMD1:2016 (lab measurement equipment safety); IMT-2020 / ITU-R M.2083 (5G massive connectivity — informed NOMA concept selection); IEEE 1800/IEEE 1364 HDL Design Standards (Verilog RTL implementation).
Key constraints satisfied	Budget: 208,409 KZT was spent of 331,000 KZT that was approved. PCB manufacturability: two-layer design and FR-4 throughout. Schedule: must be completed within a 13-week semester. Hardware availability: only DE1-SoC FPGA was available in the university, so it was used exclusively. Power: circuits must operate at 3.3 V level. S_{11} must be less than -10 dBi. Safety: low-power indoor tests only, under supervisor's approval.
Most important trade-off	Custom RX-PCB was replaced by the Universal Software Radio Peripheral (USRP) 2932 (DE-04) due to component delivery failure. This limited hardware completeness in term of custom design but led to produce system-level NOMA validation within the semester. The substitution also provided a receiver platform that allowed the RX parameters more flexible such as filtering, power gain and phase shift.
Overall result	Functional NOMA prototype was demonstrated over the air at 2.47 GHz frequency. Both users decoding algorithm was implemented successfully, obtaining both users data. All performance, regulatory, interface, and PCB requirements were met. System delivered on time and under budget limitations. Prototype constitutes an implementation for future NOMA hardware research at Nazarbayev University.

Table 0-C. Design Evolution Log.

Iteration ID	What changed	Why changed it	Evidence that the triggered change	Impact on performance / cost / schedule / risk	Date
DE-01	Transition from integrated RF transceiver to discrete IF-based architecture (DAC, ADC, mixer, Local Oscillator (LO))	Integrated RF solutions were unavailable or incompatible with available FPGA boards	Component availability issues and interface mismatch identified during early design	Improved flexibility and control; increased system complexity; moderate schedule impact	Week 3
DE-02	Reselection of external DAC, ADC, mixer, and LO synthesizer	Need for compatibility with FPGA input/output (I/O) and discrete RF architecture	Hardware interface requirements and FPGA constraints	Increased PCB design effort; improved controllability of RF chain	Week 3
DE-03	Change from Type-C power supply to DC power source	Type-C cables could not provide stable power for ADC and RF components	Observed unstable power behavior and evaluation of cable limitations	Improved power stability and ADC performance; reduced portability	Week 9
DE-04	Changed to USRP as substitute receiver for system validation	Receiver hardware not fully assembled (missing critical component)	Inability to complete receiver chain and proceed with planned testing	Enabled system-level validation; reduced hardware completeness but avoided major delays	Week 11–13
DE-05	Added a 10-dB amplifier in the receiver chain to improve	The initial received signal at the receiver was too weak for reliable detection	Receiver measurements showed approximately -50 dBm signal	Improved received signal power and detectability; small increase in component cost and analog front-end	Week 11-13

Iteration ID	What changed	Why changed it	Evidence that the change triggered	Impact on performance / cost / schedule / risk	Date
	received signal level		level before amplification	complexity; no major schedule impact	

1. Executive Summary (1 page)

Background and Motivation

The wireless network environment is increasingly facing challenges as more and more devices become connected. For instance, in Kazakhstan, there were 27.3 million mobile subscriptions in 2025, exceeding the entire population. It is projected that in the coming decade, the world will see tens of billions of devices being connected. However, the available amount of the radio frequency spectrum is limited. Traditional techniques like Time Division Multiple Access (TDMA), Frequency Division Multiple Access (FDMA), Code Division Multiple Access (CDMA) allocate unique slots either in the frequency domain or time domain for each and every user resulting in the inherent limitations of high-density environments. NOMA technology can be seen as an emerging technique to solve these challenges in 5G and beyond by enabling transmission of multiple users through the same channel but at varying power levels using SIC technique.

Problem Statement and Need

Despite a large theoretical base of study, the practical hardware implementations of NOMA remain rare in academia. Most research exists only as simulations and cannot capture real-world impairments such as RF distortion, timing mismatches, and PCB-level signal integrity effects. There is a clear need for a transparent NOMA hardware prototype that shows and solves these practical challenges and can demonstrate as a reusable reference for future researchers and engineers.

Final Design Solution

The team designed and implemented a power-domain NOMA prototype operating in the 2.4 GHz ISM band using a discrete IF-based RF architecture. The transmitter consists of a DE1-SoC FPGA performing real-time NOMA baseband processing, an AD9742 DAC, an RF transformer, a low-pass filter, an HMC213 mixer, and an ADF4351 frequency synthesizer, all mounted on a custom two-layer PCB. The receiver was implemented using an NI USRP-2932 software-defined radio with a 10 dB LNA, running a GNU Radio receiver chain that performs carrier recovery, timing recovery, and SIC in software. Three custom patch antennas were designed, simulated in Advanced Design System (ADS), and fabricated in-house for operation at 2.47 GHz.

Final Performance Achieved

- Over-the-air NOMA transmission demonstrated at 2.47 GHz with two simultaneous users on the same frequency channel
- Near user BER = 1×10^{-6} (9 errors in 18.4 million bits) at short range
- Far user BER = 3.06×10^{-4} at short range — after successful SIC
- Total system throughput = 6.125 Mbps (two BPSK users at 3.125 Mbit/s each)
- SIC confirmed working: 4-peak composite symbol histogram collapses to two-peak after interference cancellation
- Antenna VNA measurement: $S_{11} = -35.20$ dB at 2.47 GHz — excellent impedance matching
- A_1/A_2 power ratio = 2.73 stable across all captures — consistent NOMA power allocation
- Project delivered under budget: 208,409 KZT spent of 331,000 KZT approved

Requirements Met / Partially Met / Unmet

- TLR-1: System throughput ≥ 5 Mbps — achieved 6.125 Mbps
- TLR-2: Far user BER $\leq 10^{-3}$ — achieved 3.06×10^{-4} at short range
- TLR-3: Near user BER $\leq 10^{-3}$ — achieved 1×10^{-6} at short range
- REQ-D1: ISM band operation — system operating at 2.47 GHz within 2.40–2.48 GHz
- REQ-D6: FPGA hardware interface compatibility — 3.3 V interfaces, no level shifting required
- REQ-D8: PCB design compliance — IPC-2221 rules applied, design rule check (DRC) passed before fabrication

Main Limitation and Recommended Next Step

The major limitation is the lack of synchronization in terms of timing between the FPGA-based transmitter and the USRP-based receiver, thus making it impossible to perform end-to-end frame synchronization decoding even when the physical layer BER is virtually zero. The next action step suggested is to design a preamble correlator for performing frame synchronization through detection of the known 8-bit training sequence in the incoming bit stream and correctly setting the frame boundary prior to data decoding. Furthermore, the custom-built RX PCB needs to be built once the delayed parts arrive.

2. Problem Definition, Stakeholders, Context, and Constraints (2–3 pages)

2.1 Problem Definition and Need Statement

Wireless communication networks come under growing pressure due to the fast development of users' number and connected devices. As the population grows and technology advances, every person uses multiple connected devices including smartphones, computers, and Internet of Things. Thus, in Kazakhstan, in 2025, there were 27.3 million cellular mobile connections which amounted to 131% of the population, which means multiple devices per one person. Moreover, 93.4% (19.5 million people) used internet and 80.8% (16.9 million people) communicated via social networks. Thus, Kazakhstani citizens make wide use of wireless devices [1]. Global estimates suggest that by 2022, the amount of connected devices will amount to several billion units. The need for wireless connection, hence, will grow significantly [2].

On the other hand, the spectrum of radio frequencies remains restricted. Traditional approaches to multiple access are based on allocation of different time periods or frequencies for every client's data transfer, thus implying the employment of TDMA, FDMA, CDMA, etc. These solutions are effective but at the same time impose restrictions as to the maximum number of simultaneously served clients.

As a result, one faces another important problem of high connectivity, meaning a possibility to connect many users to the common channel for communication. This problem consists not only in the improvement of transmission rates, but also in providing a possibility for more users to be connected using the same spectrum.

In order to solve this problem, new multiple access schemes, such as NOMA, have been suggested. As opposed to existing schemes, the NOMA technology provides for connecting several users to the same frequency resources at the same time.

2.2 Stakeholders

Aspects of this research require consideration of many parties who affect the outcome of the process through their interests, obligations, and limitations. Table 2-A gives a summary of some of the most important stakeholders of this project.

Table 2-A. Stakeholder Analysis.

Stakeholder	Role/Interest	Needs/Success criteria	How engaged (meetings/inputs)	Impact of project
Project team (students)	Design, implementation,	Functional hardware	Weekly internal meetings; joint design	Gains hands-on experience in RF

	testing, and documentation of the NOMA system	prototype; successful demonstration of NOMA with measurable BER and throughput; completion within semester	reviews; task division across PCB, RF, FPGA, and antenna work	systems, FPGA design, PCB layout, and system integration
Academic supervisor	Technical guidance, academic quality control, risk oversight	Correct engineering methodology; feasibility within constraints; alignment with learning objectives	Regular supervisor meetings, review of architecture, component selection, and report drafts	Ensures academic rigor and guides project toward realistic, testable outcomes
Department / University	Provider of infrastructure, labs, and fabrication resources	Safe use of facilities; compliance with lab rules; successful capstone outcomes	Access to RF lab, FPGA boards, PCB manufacturing tools, and safety training	Receives a reusable prototype and documentation for future teaching or research
Future students / researchers	Potential users of the prototype as a reference or test platform	Clear documentation; modular and understandable system design	Indirect engagement through final report	Benefit from a practical reference implementation of NOMA hardware
Wireless industry (indirect)	Interest in practical validation of NOMA concepts	Insight into implementation challenges and trade-offs	No direct engagement	Demonstrates real-world constraints often hidden in simulations

2.3 Context and Operating Environment

This project is developed within the RF laboratory at Nazarbayev University as part of the ENG 400 Capstone course. The system operates in the 2.4 GHz ISM band, which requires no transmission license and is suitable for low-power indoor academic experimentation. All testing is conducted indoors under controlled conditions to minimize interference and ensure measurement repeatability.

The design is built on the DE1-SoC FPGA development board, with RF frequency conversion that was handled by external components such as DAC, ADC, mixer, and frequency synthesizer. All were mounted on a custom PCB. The PCB fabrication is limited to two copper layers, which constraint routing, grounding, and RF impedance matching decisions. A key assumption is that the laboratory environment provides sufficient isolation for valid over-the-air measurements between the transmitter and receiver chains.

2.4 Constraints and Context Factors

The design is based by eight constrains summarized in Table 2-B.

Table 2-B. Constraints Matrix.

Constraint category	Metric / target	Final estimate or measurement	Gap residual risk /	Owner	Evidence next action /
Budget	BOM $\leq$ 393,200 KZT	208 409.35 KZT spent on active components	Low	Team	Table 8-B; Table F-B;
Manuf- curability	Number of PCB layers ≤ 2	TX layout complete; RX in progress	Medium (routing density, RF isolation)	Idris Aidana	Figs. D2-D5; Figs. D11-D14;
Schedule / Delivery	Completion ≤ 12 weeks	Core tasks on track; integration pending	Medium (assembly time)	Team	Table 9-B; Table 10-B; Table F-A; Table F-C;
Hardware availability	DE1-SoC FPGA only	Architecture finalized to match available components	Low	Yerboldy Aidana	Fig. E2; Fig. E3;
Input voltage	3.3 V I/O; lab bench supplies	Design based on FPGA-compatible voltage levels	Low	Amir Yerboldy	Figs. 3-6; Fig. E4;
RF / Regulatory	Operation within 2.4 GHz ISM band	Architecture supports compliant operation	Low	Idris	Fig. 9; Fig. 15; Fig. 21;
Antenna design	Gain ≥ 5 dBi	Designed antenna gain ≈ 10 dBi	Low	Idris	Figs. 18-19; Fig. D6;
Safety	Follow lab and RF safety rules	Low-power indoor testing only	Low	All	Fig. 21; Table C-2.

3. Final Requirements, Acceptance Criteria, and Traceability (2–3 pages)

3.1 Final Requirements Compliance

Table 3-A. Final Requirements Compliance Matrix.

Req. ID	Requirement statement	Source	Verification method	Target threshold	Measured result	Verdict	Evidence ID
TLR-1	Number of supported users = 2	Project objective	System demonstration, waveform inspection, and end-to-end decoding test	Successful dual-user decoding	Two users successfully connected	✓	Section 8.2; Table 8-A; Table 8-B;
TLR-2	The near-user BER under NOMA operation at BER $\leq 10^{-3}$ at SNR ≤ 40 dB.	Performance requirement from the progress report	BER measurement by laboratory test	BER $\leq 10^{-3}$	1×10^{-6}	✓	Fig. 20
TLR-3	The far-user BER under NOMA operation at BER $\leq 10^{-3}$ at SNR ≤ 40 dB	Performance requirement from the progress report	BER measurement by laboratory test	BER $\leq 10^{-3}$	3.06×10^{-4}	✓	Fig. 20
TLR-4	The implemented NOMA system must provide higher sum throughput (≥ 5 Mbps).	Stakeholder need for a meaningful NOMA advantage	Throughput comparison using logged frames	Throughput ≥ 5 Mbps	6.125M bps	✓	Fig. D6; Fig. 19;
REQ-D1	The RF front-end operates only within the 2.400 – 2.4835 GHz ISM band during testing.	Regulatory requirement	Configuration inspection and spectrum verification	All transmissions remain inside ISM band	Working frequency = 2.47 GHz	✓	Fig. 9; Fig. 15; Fig. 21;
REQ-D6	The FPGA interfaces must be electrically compatible with	Hardware interface requirement	Schematic inspection and interface validation	3.3 V logic compatibility	Schematic-level compatibility	✓	Figs. 3-6; Fig. E4; Fig. D9-D10

	the DAC, ADC, and LO synthesizer without external level shifting.			maintained	achieved		
REQ-D8	The PCB should comply with the selected PCB design rules for trace width, spacing, grounding, and RF routing appropriate for a two-layer academic prototype.	Manufacturability and standards requirement	PCB DRC and supervisor review	No critical DRC violations before fabrication	DRC passed before fabrication	✓	Fig. 5; Fig. 7; Table C-2

3.2 Requirements Traceability

Table 3-B. Requirements Traceability Matrix.

Stakeholder need	Requirement(s)	Constraint(s)	Standard clause(s)	Design feature(s)	Test ID(s)	Result section
Demonstrate a practical two-user NOMA communication system in hardware	TLR-1, TLR-2, TLR-3	Hardware availability, schedule, and budget	IMT-2020 (massive connectivity, spectral efficiency)	FPGA-based superposition coding, SIC-capable receiver, discrete TX/RX chain	T1, T2	Fig. 11-14; Fig. 21; Fig. C3; Fig. C5; Fig. D2-D6; Fig. D9-D10;
Keep the design feasible for a student capstone project	REQ-D6, REQ-D8	Two-layer PCB only, DE1-SoC only, budget	IPC-2221	3.3 V-compatible interfaces, controlled RF routing, ground-plane-based layout	Inspection, DRC review	Fig. 3-7; Fig. E4; Fig. D9-D10;
Ensure safe and working RF operations	REQ-D1, environmental and safety	RF / regulatory, safety, indoor-lab operation	ITU-5.150 ISM band requirement; IEC 61010-1;	2.4 GHz frequency operation, supervised	T4, inspection	Fig. 21; Table C-2; Fig. 9; Fig. 15;

Stakeholder need	Requirement(s)	Constraint(s)	Standard clause(s)	Design feature(s)	Test ID(s)	Result section
	requirements		university lab rules	measurement setup		
Produce reusable academic design documentation	TLR-1, REQ-D5, REQ-D8	Time, documentation quality and manufacturability	IPC-2221, course report requirements	Documented schematics, PCB files, logs	Documented schematics, PCB files, logs, architecture processing	Fig. 3-4; Fig. 6-7;
Support real-time FPGA-based implementation rather than offline-only processing	REQ-D6, REQ-D7	FPGA timing, I/O compatibility, symbol-rate limit	IEEE 1800 (SystemVerilog) / IEEE 1364 (Verilog HDL)	Dedicated TX/RX RTL blocks, DAC/ADC parallel interface, real-time frame processing	Dedicated TX/RX RTL blocks, DAC/ADC parallel interface, real-time frame processing	Fig. 13; Fig. D9; Fig. E2-E4; Table 7-A; Fig. 3-6; Table 8-A.

3.3 Derived, Interface, Environmental, and Regulatory Requirements

The top-level requirements are supported by traditional standard requirements that are needed for real implementation in the laboratory.

Derived requirements

- **REQ-D1: ISM band operation.** The RF front-end must operate only within the stated **2.400–2.4835 GHz ISM band**. This requirement is needed because the prototype must be compatible with the low-power laboratory setup and supports TLR-1.
- **REQ-D2: Controlled indoor test environment.** All over-the-air experiments must be conducted only in an indoor laboratory environment. This requirement reduces external interference and improves repeatability of BER and throughput testings, supporting TLR-2 through TLR-5.
- **REQ-D3: Power-allocation control.** The system must allow adjustment of the NOMA power-allocation coefficients for both of the users. This requirement is needed to evaluate the system performance under different power allocations, supporting TLR-1, TLR-2, and TLR-3.
- **REQ-D4: Pilot and preamble structure.** Each transmitted frame should include preamble symbols for synchronization. This supports accurate decoding and proper working of SIC operation.

Interface requirements

- **REQ-D5: Measurement and logging capability.** The FPGA should log transmitted bits and throughput analysis. This is required to verify TLR-2, TLR-3, TLR-4, and TLR-5.
- **REQ-D6: Hardware interface compatibility.** The FPGA I/O levels and timing should be compatible with the selected DAC, ADC, and LO interfaces. This supports integration of the TX and RX hardware.
- **REQ-D7: Real-time processing limit.** The FPGA implementation must transmit frames at the selected symbol rate without buffer overflow or underflow.

Environmental and regulatory requirements

- **REQ-D8: PCB design compliance.** The PCB must follow selected design requirements for trace spacing, grounding, and width that are compatible with the two-layer manufacturing. This must be done in order to produce reliable prototype under the the two-layer limitations.
- **REQ-D9: Low-power laboratory operation.** The prototype should be tested only at low transmit power levels approved for laboratory use. This requirement supports safety, prevents unintended interference, and aligns the project with university laboratory procedures.
- **REQ-D10: Safe measurement practice.** All laboratory work must be done with grounding, current-limited laboratory equipment and under the supervision of the supervisor. This supports safe laboratory measurements.

4. Engineering Standards, Regulations, and Compliance Evidence (1–2 pages)

Table 4-A. Standards Application Matrix.

ID	Stand ard / regula tion	Clause used	Why applicable	Design decision affected	Verification / inspection method	Evidence produced	Compl iance status
STD-1	ITU-5.150 Radio Regulations – ISM Band (2.4 GHz)	ISM allocation 2.400–2.4835 GHz, EIRP & spurious emission limits	The prototype transmits RF signals over the air during laboratory testing and must operate within unlicensed ISM band limits	Selection of ADF4351 LO frequency; choice of 2.4 GHz band-pass filter to suppress harmonics; limitation of transmit power at mixer output	Spectrum analyzer measurement of transmitted signal during V&V phase; verification of LO frequency settings and RF filter response	LO configuration screenshots; planned spectrum analyzer plots	✓
STD-2	IPC-2221 – Generic Standard on PCB Design	Conductor width, spacing, RF routing, and grounding practices	The project uses a custom two-layer PCB carrying both IF/RF analog signals and high-speed digital signals, requiring controlled impedance and adequate isolation	50-Ω microstrip trace geometry calculated; solid ground plane on Layer 2 for return path integrity; physical separation of RF and digital sections;	PCB design rule check (DRC) in CAD tool; layout review by supervisor prior to fabrication submission	DRC reports; PCB layout screenshots; microstrip impedance calculation (Fig. 5 in progress report)	✓
STD-3	IEC 61010-1 – Lab Measurement	Equipment grounding, safe operation of	The project involves oscilloscopes, bench power	Use of current-limited bench power supplies	Lab equipment safety checklist; measurement	Completed safety training records; pre-test	✓

	Equip ment Safety	measure ment devices	supplies, and spectrum analyzers during bring-up and testing, all of which must be operated safely	during bring-up; grounding of all measureme nt equipment; ESD precautions during PCB assembly	setup inspection by supervisor before RF testing	checklists ; superviso r approval	
STD- 4	IMT-2 020 (ITU-R M.208 3) - 5G Requir ements	Massive connecti vity (10^6 devices/ km ²); high spectral efficienc y targets	The project targets multi-user access and improved spectrum efficiency, aligned with next-genera tion wireless system goals	Adoption of power-dom ain NOMA; support for simultaneo us multi-user transmissio n; system-leve l architecture choice	System-level validation: dual-user transmission and decoding	Over-the- air (OTA) system test: simultane ous transmissi on and decoding of two users	✓
STD- 5	IEEE 1800 / IEEE 1364 – HDL Design Standar d (Syste mVerilog / Verilog)	RTL design, timing behavior , and synthesi zable construc ts	The system is implemente d on FPGA using HDL, requiring standardize d hardware description and synthesis practices	Design of TX/RX RTL modules; implementa tion of superpositi on coding and SIC logic; DAC/ADC interface design	Functional simulation (ModelSim); synthesis and timing analysis (Quartus); on-board FPGA testing	FPGA functional testing; on-board signal verificati on; timing analysis	✓

5. Concept Generation, Trade-off Study, and Selected Concept (3 - 4 pages)

This section demonstrates alternative concepts that were considered for the multiple access schemes of the capstone system and show reasons why the final concept was chosen. Since the main engineering goal of the project was to build a practical multi-user wireless prototype under course requirements and existing constraints, the team first compared several multiple-access approaches before choosing the NOMA-based design. The comparison was not only limited to theoretical performance. It also considered receiver complexity, hardware cost, and suitability for a FPGA and two-layer PCB.

5.1 Candidate Concepts

Four concepts were considered: FDMA, TDMA, CDMA, and NOMA. These candidates were selected because they can support multi-user communication, but give different results in term of implementation complexity, synchronization requirements, throughput and BER. The team has considered these concepts as practical options for implementation within the available resources.

Table 5-A. Candidate Concepts.

Concept	Description	Strengths	Weaknesses	References / evidence
FDMA	FDMA separates the overall bandwidth into numerous small subcarriers and allocates various subcarriers to various users to avoid any interference. It has good flexibility and does not interfere with channels. It involves very rigid timing and frequency coordination; however, small synchronization errors can be a problem for loss of subcarrier orthogonality and deterioration of system performance [3]. It is relatively easy to enforce strict isolation between channels with the help of adequate filters and tuners. Frequency bands of FDMA channels are very small (25-30 kHz) because a channel can only accommodate a single call at a time [4].	Simple channel separation, predictable operation, relatively straightforward receiver design, mature concept [3], [4].	Requires more bandwidth, lower spectral efficiency, tighter filter planning, less attractive for demonstrating advanced multi-user transmission [3], [4].	[3], [4]
TDMA	Time multiplexing is done for the users. The receiver is very simple, and the delay is predictable because the schedule is fixed. But if there are many users, the delay can grow, and if traffic is bursty, users may experience higher latency. Works well for simple and low-cost systems. These are benefits in that only one radio frequency section is needed, as the characteristics of all channels are the same frequency [3].	Simple receiver structure, easy to understand and implement, and deterministic	Higher latency with multiple users, synchronization overhead, burst timing complexity, and inefficient for	[3], [5]

Concept	Description	Strengths	Weaknesses	References / evidence
	Transmission of data to users of a TDMA system is not constant but bursting. In TDMA systems, synchronization overhead is required because of burst transmission. The complexity of TDMA mobile systems is higher compared with FDMA systems [5].	c scheduling [5].	demonstrating simultaneous user service [3].	
CDMA	Any user is able to transmit simultaneously and at the same frequency band. It is achieved by assigning every user with a code that distinguishes them among others. Any user is able to transmit simultaneously and at the same frequency band. It is achieved by assigning every user with a code that distinguishes them among others [5]. CDMA systems offer more radio channel capacity as compared to FDMA systems and TDMA systems. The capacity of radio channels is the efficiency of the spectrum of a wireless system [3].	Better spectral reuse than basic FDMA/TDMA, simultaneous access possible, and well-established theory [3].	More difficult code management, higher receiver complexity than FDMA/TDMA, less suitable for a simple low-cost prototype [3], [5].	[3], [5]
NOMA	The multiple access scheme allowing users to simultaneously use resources in a non-orthogonal manner on a subcarrier, allowing the transmission of information on the same frequency at the same time, is called NOMA, which offers both high spectral/energy efficiency and user capacity, at the expense of receiver complexity and SIC performance in the presence of imperfect CSI [6]. As opposed to OMA, NOMA can allocate a single frequency channel to more than one user simultaneously within the same cell and has several advantages, such as spectral efficiency (SE) and cell-edge throughput, channel feedback is relaxed, and transmission latency is low (no user to base station scheduling request is necessary) [7].	Highest spectral-efficiency potential among the considered concepts, directly aligned with the project objective, suitable for demonstrating simultaneous two-user service [6].	Higher receiver complexity due to SIC, more sensitive to power allocation and interference cancellation quality, and implementation is more challenging in hardware [7].	[6], [7]

Among these concepts, NOMA was most aligned with the educational and technical goals of the project. The purpose of the capstone was not only to create any working wireless link, but to demonstrate a modern multi-user communication technique that offers a measurable performance advantage over traditional orthogonal access methods.

5.2 Weighted Trade-off Study

The five constraints were used (weights sum = 1.0). Targets were chosen to be realistic for a capstone project:

1. **BER:** unitless, the target is to build a reliable communication with minimal errors.
2. **Throughput:** bits per second, the target is to maximize the data transmission for both near and far users.
3. **Receiver implementation complexity:** is measured qualitatively but mapped to 0–10.
4. **BOM / Hardware cost (KZT):** must be ≤ 25 monthly calculation index (MCI) for each student, which is = 108,125 KZT.
5. **Manufacturability / Schedule & Risk:** lower schedule/risk is better

In the trade-off matrix, as constraints, BER (= 0.25), throughput (= 0.25), receiver complexity (= 0.20), BOM cost (= 0.15), and manufacturability / schedule risk (= 0.15) were taken. BER and throughput are chosen as the top priorities, while BOM cost and manufacturability/schedule are less significant. It is shown in the table that NOMA has the highest score among other multiple schemes and provides a performance and implementation constraints.

Table 5-B. Weighted Trade-off Matrix

Criterion	Metric target /	Weight	FDMA	TDMA	CDMA	NOMA	Evidence source
BER	Unitless (lower is better)	0.25	8 [6]	6 [7]	7 [5]	8 [4]	[4-6]
Throughput	bps (higher is better)	0.25	6 [5]	5 [9]	6 [8]	8 [7]	[5], [7], [8], [9]
Receiver complexity	lower is better	0.2	6 [11]	8 [12]	7 [13]	6 [10]	[10-13]
BOM / hardware cost	($\leq 331,000$ KZT target)	0.15	6 [16]	7 [15]	6 [14]	5 [17]	[14-17]
Manufacturability/schedule & risk	lower risk = higher score	0.15	6 [16]	7 [15]	6 [14]	5 [17]	[14-17]

The weight of throughput was increased from 0.25 to 0.30, while the BER weight was reduced from 0.25 to 0.20. The total score values for all methods were calculated again.

New totals (weighted sums):

- FDMA = 6.40
- TDMA = 6.30

- CDMA = 6.35
- NOMA = 6.80

As it can be seen, NOMA remains the winner with 6.80 points. It is mainly because of NOMA's strong throughput advantage. However, it is compensated with complexity implementation. Nevertheless, if BER becomes more critical or implementation constraints would dominate, OMA schemes such as FDMA or TDMA might become more preferable.

5.3 Selected Concept and Rationale

Based on the weighted trade-off study, NOMA was selected as the main communication concept. This choice was based on both the technical objectives and existing limitations of the project. The team accepted several trade-offs. The receiver complexity increased due to SIC. Additionally, implementation risk was higher due to a custom student design, rather than a building existing NOMA projects. These trade-offs were considered acceptable as they allowed the project to address a more meaningful engineering challenge.

To implement this concept, a digital architecture was chosen with the DE1-SoC FPGA, DAC/ADC chips, mixers, a local oscillator, and a custom PCB. This approach has a practical design challenges such as PCB routing, impedance matching, FPGA code implementation. Overall, the final concept is a NOMA prototype suitable for capstone-level implementation.

6. Design Iterations and Decision History (1-2 pages)

The final NOMA prototype was not a fixed design from the beginning. Instead, it evolved through numerous iterations and trials made by students to improve the performance of the whole system. These changes were based on hardware limitations, 2-layer PCB constraints, schedule deadlines, components compatibility, and system performance. Each major change was made due to a concrete issue during the project implementation and was evaluated for its impact on performance, time requirements for processing and existing limitations. This iterative process was important because it helped students to find better possible solution for this project.

Initially, the team considered architectures that are based on existing solutions. However, this approach was revised once it became clear that the available solutions hardware are not suitable for educational purposes. As a result, a new design was built to meet the ethical requirements. This increased the engineering complexity of the project, but it also made the final system more suitable for capstone targets.

Table 6-A. Major Design Iterations

Iteration / version	Issue discovered	Alternatives considered	Decision made	Trade-off accepted	Evidence of improvement
Proposal Design (RF IC AT86RF215)	IC has limited flexibility and compatibility issues with FPGA and system requirements	Use integrated RF transceiver; Switch to discrete RF components	It was transitioned to discrete IF-based architecture (DAC, ADC, mixer, LO)	Increased system complexity and PCB design effort	Greater control over RF chain; successful schematic design and hardware compatibility
Initial Power Design (Type-C)	It was realized that many Type-C cables and connectors cannot provide stable power	Use higher-quality Type-C cables; Use DC power source	It was decided to power everything through a DC power source, because the ADC requires a stable power supply.	Reduced portability and convenience	Stable power supply achieved; improved ADC performance and reduced noise
Project Scheduling	Component delivery delays and fabrication	Keep original schedule; Adjust timeline	PCB timeline and parallelized tasks was extended	Slight compression of testing phase	Maintained overall project progress and avoided major delays

Iteration / version	Issue discovered	Alternatives considered	Decision made	Trade-off accepted	Evidence of improvement
	time affected timeline				
Receiver Implementation / Validation	One critical receiver component was not delivered on time, so the RX PCB could not be fully assembled and tested.	Waiting for the missing component and delay testing; redesign the receiver; use alternative receiver hardware.	USRP was used as a substitute receiver for system-level validation while keeping the RX PCB ready except for the missing component.	Completeness of the custom RX hardware demonstration was reduced; integration effort with USRP was added.	Testing and validation continued without major delay; system-level NOMA functionality was still demonstrated.
Receiver Signal Strength Improvement	Initial received signal level was too low (~ 50 dBm), limiting reliable detection.	Increase transmit power; improve antenna; add amplifier.	A 10 dB amplifier in the receiver chain was implemented.	Additional component cost and increased system complexity.	Received signal power increased significantly, improving signal detectability and system performance.

7. Final System Architecture (4-5 pages)

The final prototype architecture was built to be practical downlink power-domain NOMA communication system. The design includes one FPGA-based transmitter and a USRP-based receiver connected to the antenna. The transmitter performs baseband NOMA signal generation and RF upconversion, while the receiver performs SIC to decode the near-user signal.

Initially, the system was designed with a custom PCB-FPGA receiver chain. However, due to the unavailability of a critical component, the receiver hardware could not be fully completed before the final submission deadline. To solve this issue, the design was changed by replacing the custom student solution with an available USRP platform. This change allowed to finish the project on time and meet all the targets.

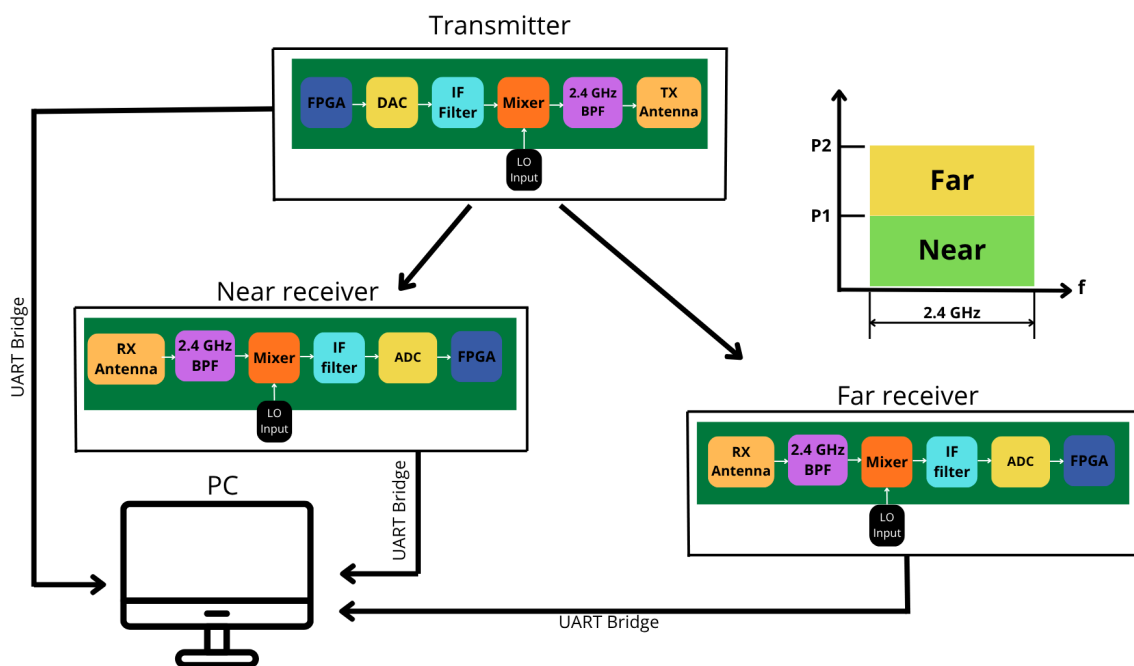


Fig. 1: Initial System Block Diagram (PCB-based RX)

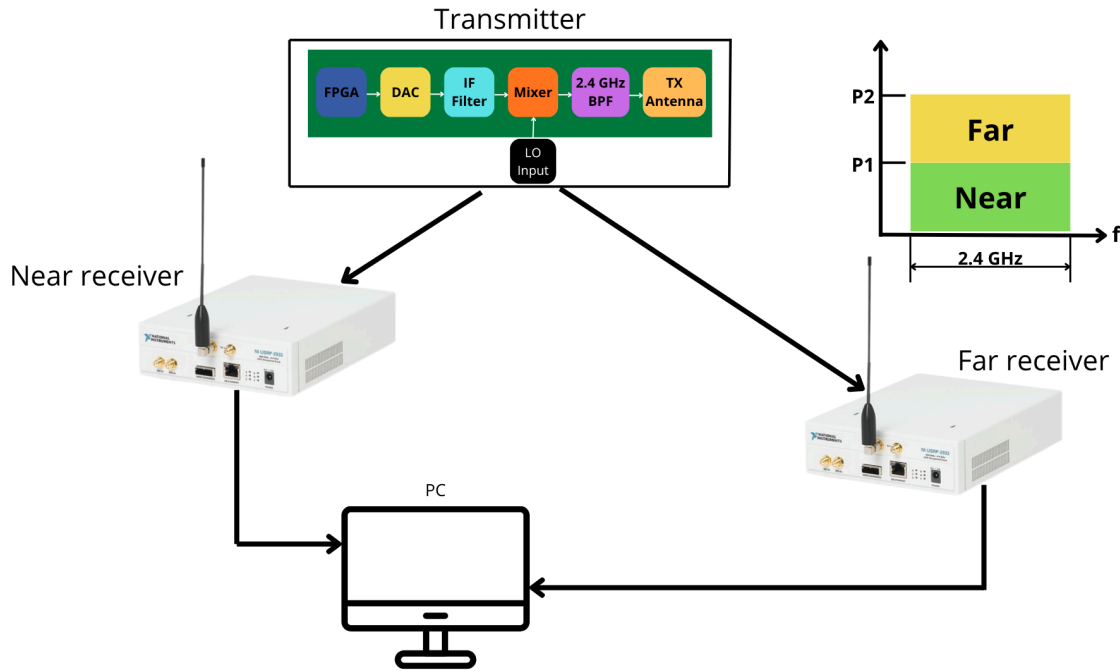


Fig. 2: Final System Architecture (USRP-based RX)

The signal flow is divided into three main layers:

1. Digital baseband layer – implemented in the FPGA. It includes signal generation, BPSK modulation, NOMA superposition coding, and demoduation on the receiver side.
2. Mixed-signal interface layer – implemented using DAC and ADC integrated chips that are connected with the FPGAs.
3. RF front-end layer – implemented using RF transformers, filters, mixers, LO generation, and antennas for 2.4 GHz.

Architecture Description

Transmitter subsystem

The transmitter begins in the FPGA, where the digital data streams for two users are generated, modulated, and combined using superposition coding. The superimposed signal is sent to the DAC that converts the data into an analogue signal. This analogue signal goes through the RF transformer. Then goes to a filter to exclude unwanted frequencies before entering the RF mixer. The mixer is connected to the ADF4351 local oscillator, which upconverts the signal to the required 2.4 GHz ISM band. After band-pass filtering to reduce unwanted frequency components and noise, the RF signal is send through the transmit antenna.

Receiver subsystem

In the beginning, the system was planned to have two separate receivers, each representing one user in the NOMA scenario. In that design, the received RF signal would first be captured by the antenna and passed through a 2.4 GHz band-pass filter to suppress out-of-band interference. The filtered signal would then be downconverted by the mixer using the local oscillator signal. The resulting intermediate-frequency IF signal would be conditioned and sampled by the ADC, and the digitised data would then be processed for synchronization, demodulation, and decoding. For the near-user path, SIC would be applied to estimate and remove the stronger interfering user before recovering the desired signal, while for the far-user path, direct detection would be performed without SIC. However, in the final implementation, instead of using the custom FPGA-based receiver chain, the receiver side was realized using an NI USRP-2932, which was used to capture the transmitted signal and perform the receiver-side processing during validation.

Integration philosophy

The system was integrated step by step, not all at once. The best solution was searched under the limitations of budget, availability of materials and our personal skills. After each iteration, team got better results. The purpose of this was to find an optimal and working solution for our project.

Table 7-A. Interface Summary.

Interface	Direction	Protocol signal type	Rate timing	Voltage power	Owner subsystem*	Notes
Baseband Data	DE1-SoC FPGA → AD9708 DAC	Parallel CMOS	IF sample rate ≤ 100 MSPS	3.3 V I/O [18]	TX subsystem	Digital baseband samples
IF Analog	AD9708 DAC → IF Filter / Driver	Analog IF	Baseband / IF	DAC, IOUTFS = 2 mA to 20 mA, nominal 20 mA; output compliance up to about 1.25 V [19]	TX subsystem	Image suppression and signal conditioning
IF to RF	IF Filter / Driver → ADL5801 Mixer	Analog IF	IF frequency	IF level is limited by DAC compliance [20]	TX subsystem	Mixer IF input
Local Oscillator	ADF4351 LO Synth →	RF LO	~2.4 GHz	−4 to +5 dBm LO output [21]	TX / RX subsystem	LO input for up/down conversion

	ADL5801 Mixer					
RF Output (TX)	ADL5801 Mixer → 2.4 GHz BPF	RF	2.4 GHz band	Up to ~9.9 dBm	Receiver	Harmonic suppression
Antenna Feed (TX)	2.4 GHz BPF → TX Antenna	RF	2.4 GHz band	-10dBi	Transmitter	Over-the-air transmission
RF Input (RX)	RX Antenna → 2.4 GHz BPF	RF	2.4 GHz band	1.024 Vp-p nominal toward ADC chain [22]	Receiver	Out-of-band rejection
IF Analog (RX)	ADL5801 Mixer → IF Filter / Driver	Analog IF	IF frequency	Signal-dependent RF level	Receiver	Downconverted signal conditioning
ADC Sampling (RX)	IF Filter / Driver → AD9283 ADC	Analog IF	≤ 100 MSPS	1.024 Vp-p nominal, 1.25 V reference	Receiver	ADC input
Baseband Data (RX)	AD9283 ADC → DE1-SoC FPGA	Parallel CMOS	IF sample rate ≤ 100 MSPS	3.3 V I/O [3]	Receiver	Digitized RX samples
LO Configuration	DE1-SoC FPGA → ADF4351	serial peripheral interface (SPI)	≤ 25 MHz	3.3 V [3]	Receiver	LO frequency programming

The most critical interfaces in the design are the FPGA-to-DAC, ADC-to-FPGA, and LO-to-mixer connections, because they directly affect signal integrity, timing stability, and successful frequency conversion in the NOMA transceiver chain.

Timing / latency budget:

The most timing-sensitive part of the system is the FPGA to DAC path in the transmitter. The AD9708 has a rate up to 125 Mega Samples Per Second (MSPS), while the project has to operate below 100 MSPS. Its output time is about 35 ns. The AD9283 works up to 100 MSPS and has a nominal input of 1.024 V peak-to-peak (p-p). The LO is configured through a 3-wire serial interface, so its timing is not critical during normal transmission [7].

Power / resource budget:

The DE1-SoC FPGA provides 3.3 V I/O. On the transmitter side, the AD9708 runs from 2.7 V to 5.5 V and provides an output current of 20 mA. On the receiver side, the AD9283 operates from 2.7 V to 3.6 V with a nominal analog input of 1.024 V (p-p). The ADF4351 requires 3.0 V to 3.6 V supply and uses 1.8 V logic. [9].

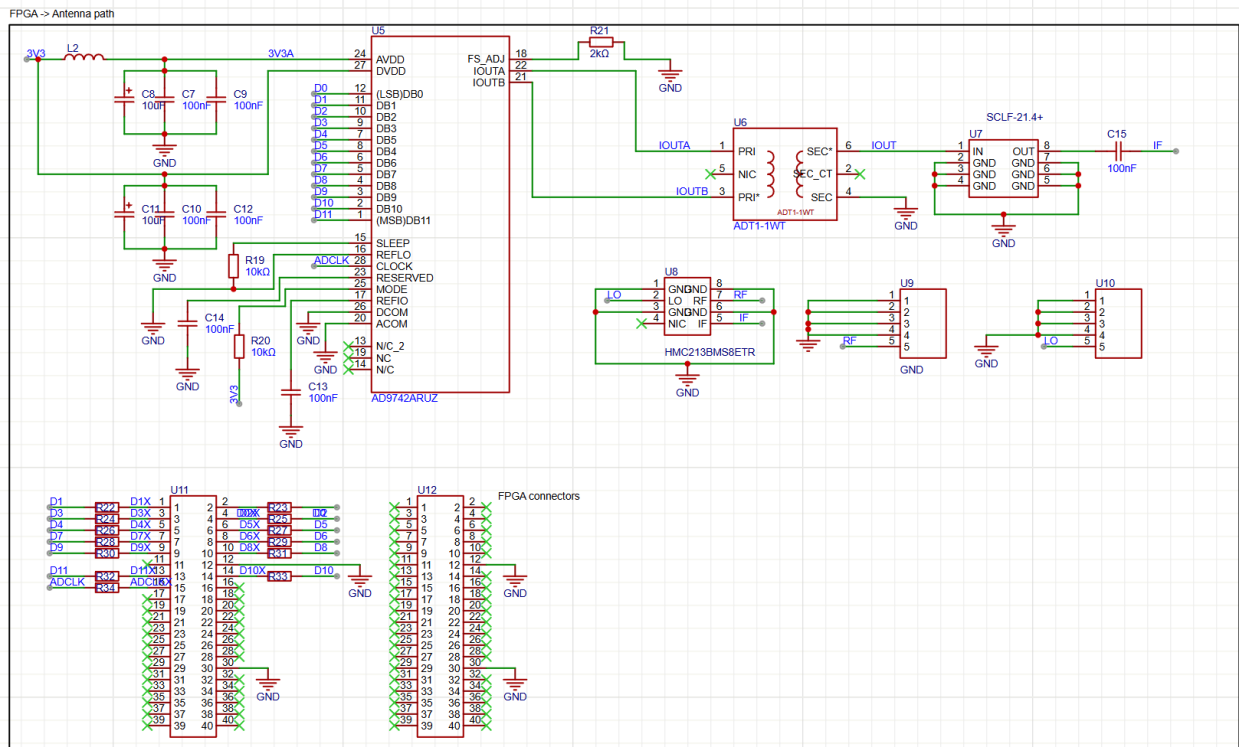
8. Detailed Design and Implementation (2–4 pages)

This section describes how the selected NOMA concept was translated into a practical hardware prototype.

8.1 Hardware design**Transmitter Design**

The FPGA board transmits digital signals from pins D0-D11 to the AD9742ARUZ digital to an analog converter, where sampled signal transforms into an analog current wave. After this, the signal goes to the RF transformer ADT1-1WT, and then to the low pass filter, to exclude unnecessary frequencies and noise. Further, the output of the filter is connected to the mixer that works with local oscillator to upconvert the frequencies up to 2.4 GHz. Then, message could be transmitted further via the antenna. Initially it was planned to power the PCB board from a type-C connector. The input signal is 5V and is transformed into 3.3 V by TPS82130SILR voltage converter. This is done because the ICs in the system works with 3.3V. However, after printing the initial board and soldering the schematic, it was discovered that the type-C connector was unstable and fragile. Instead of type-C connector was decided to use dc power supply with 5V voltage level. This made system solid.

The system has a switch that turns on and off the system. A 20x2 header is used to connect the FPGA board to PCB. Only those pins that are used for transmitting digital signals from the FPGA were connected.



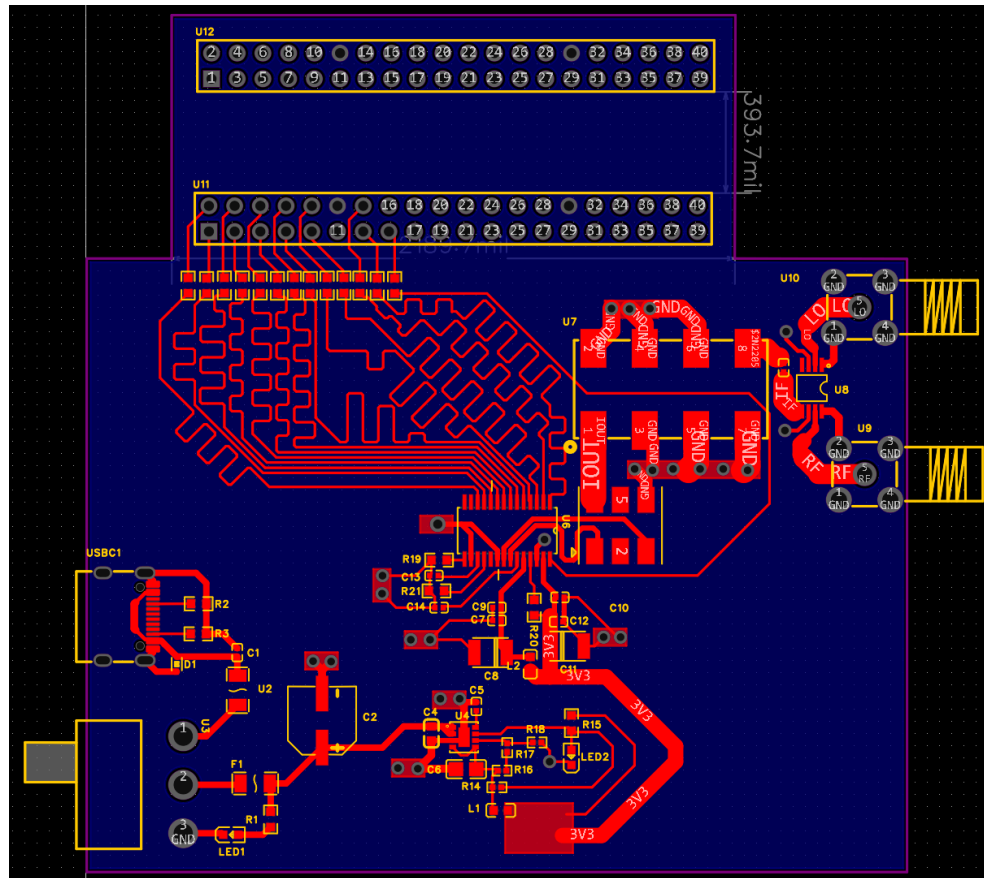


Fig. 5: PCB design of the transmitter in EasyEDA

Receiver design

At the top of the schematic, the USB-C input provides the 5 V DC voltage. Protection elements such as the ESD diode, fuse, switch, and filtering capacitors help protect the board and stabilize the incoming voltage. The 5 V is then converted into 3.3 V by the TPS82130 buck converter, which was required by the RF and ADC circuitry. Indicator LEDs show the presence of both the 5 V and 3.3 V rails. In the lower part of the schematic, the receiver signal path begins at the RF input, where the incoming radio-frequency signal is first AC-coupled and then amplified by the PSA4-5043+ amplifier. The amplified RF signal is then fed into the mixer, while a separate local oscillator signal is applied to the LO port. The mixer performs frequency downconversion, producing an intermediate-frequency signal that is much easier to work with than the original RF signal. This IF signal is then passed through the SCLF-21.4+ filter to avoid noise appeared after the mixer. After filtering, the signal is applied to the ADT1-1WT RF transformer, which helps adapt the signal into a suitable form for the ADC input. The AD9283 ADC then samples this analog signal and converts it into digital output bits. These digital outputs, together with the sampling clock, are routed through the header connectors toward the FPGA, where further digital processing such as synchronization, demodulation, and NOMA decoding can be performed.

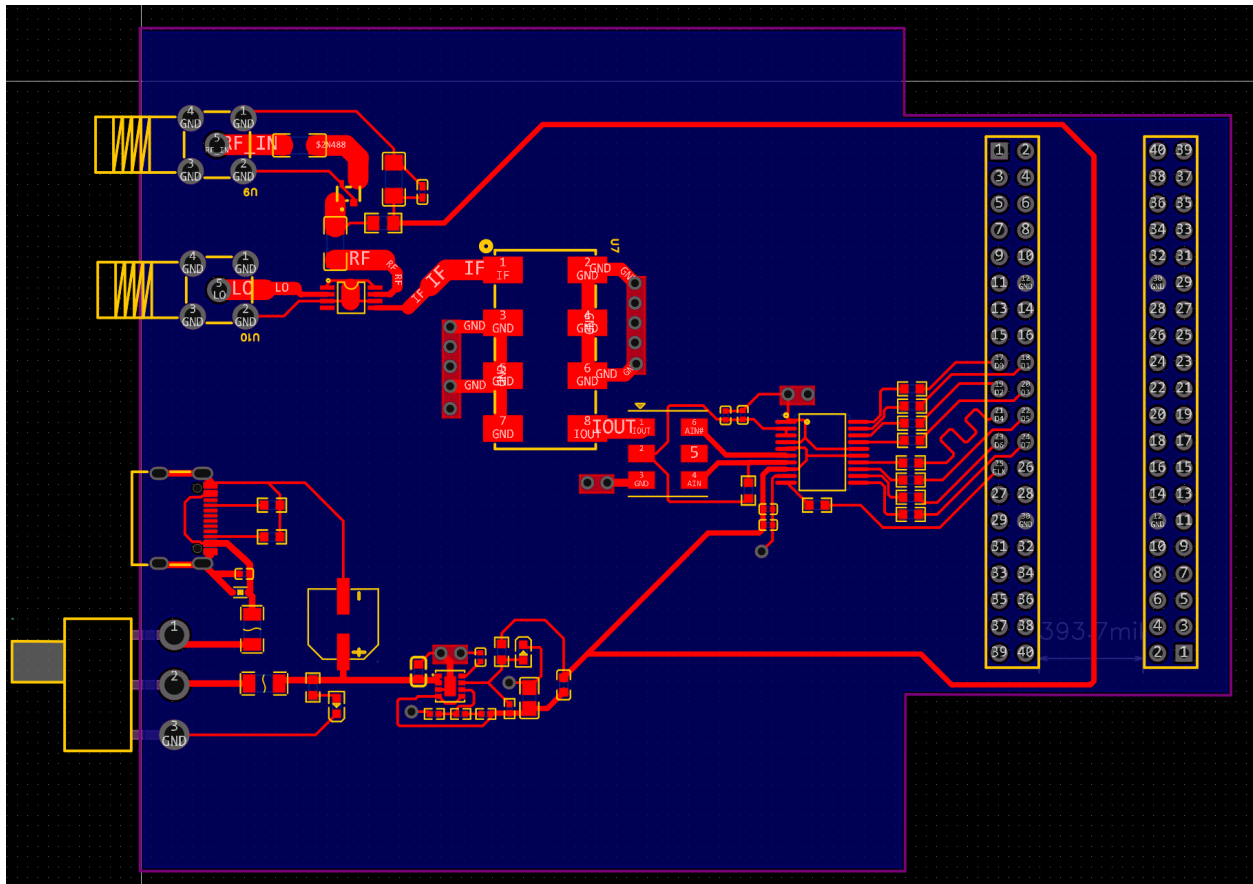


Fig. 7: PCB design of the receiver in EasyEDA

The antennas were designed separately using ADS Keysight. Three identical microstrip patch antennas were designed to resonate at 2.426 GHz within the 2.4 GHz ISM band. The geometry was optimized in simulation to achieve acceptable return loss and a broadside radiation pattern. Figs. 9 and 10 show the simulated antenna structure and radiation pattern in ADS. All three antennas were fabricated in-house on the PCB printing machine in Fig. 8 using copper-clad substrate and fitted with SubMiniature version A (SMA) connectors - one for the transmitter and two for the near and far receiver positions.

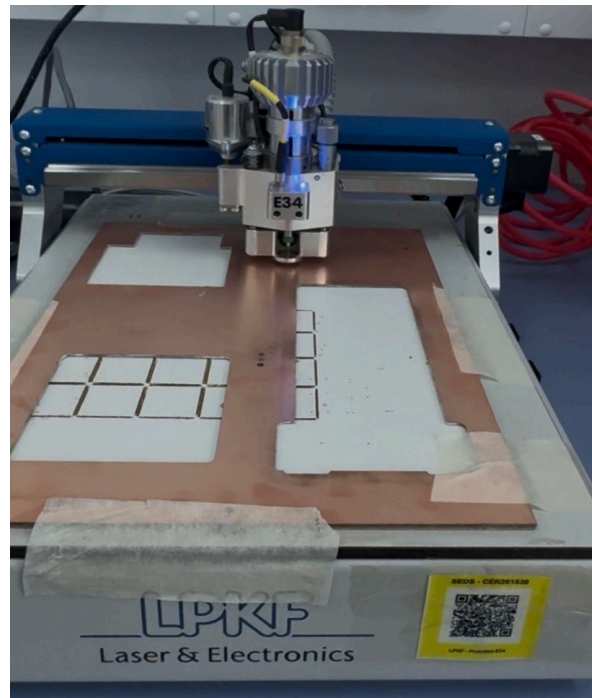


Fig. 8: PCB drilling machine

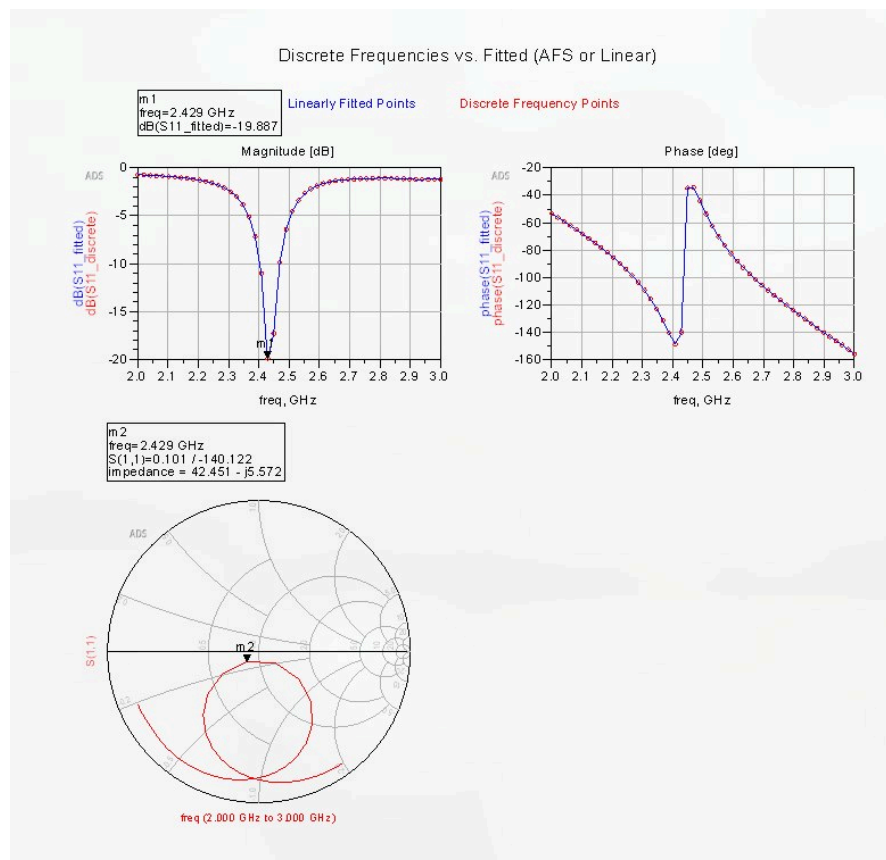


Fig. 9: Antenna parameters in ADS

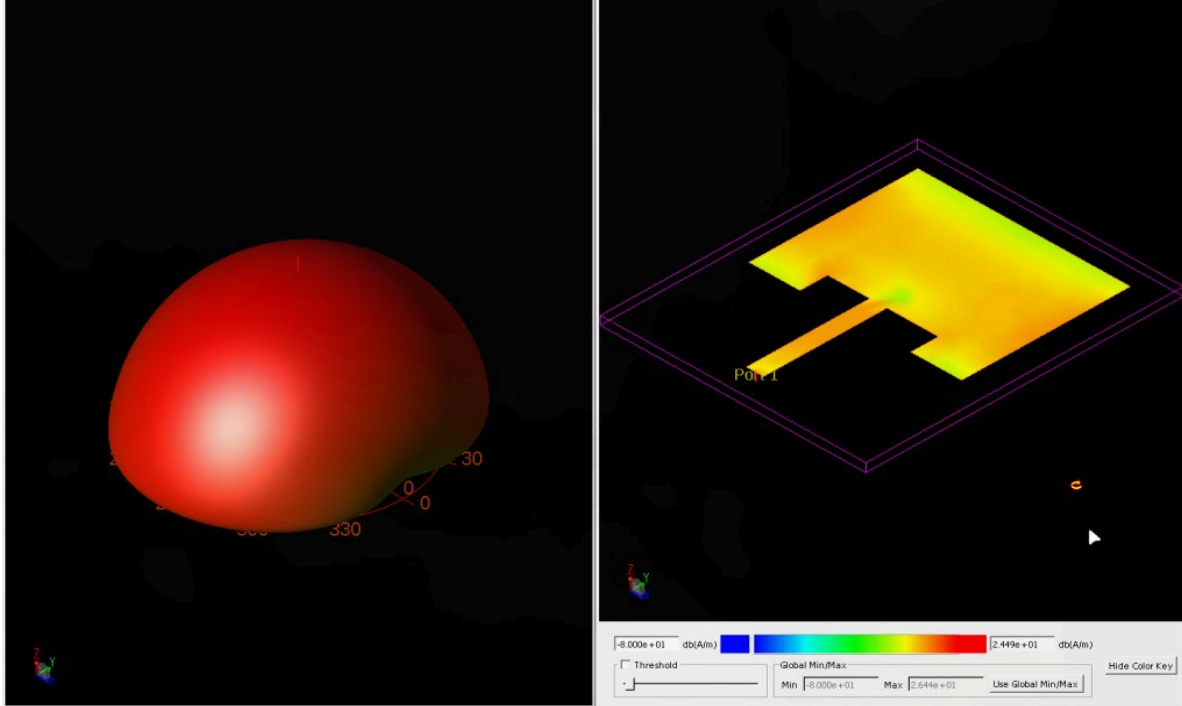


Fig. 10: Antenna design in ADS Keysight

8.2 Software / firmware design

This chapter describes the complete code implementation for both transmitter and receiver modules.

The transmitted data is organized into repeating frames of 16 bits. Each frame consists of an 8-bit preamble (alternating 10101010) shared by both users, followed by 8 data bits that differ between users:

User	Preamble [15:8]	Data [7:0]
U1 (near)	10101010	11110000
U2 (far)	10101010	11001100

The shared preamble enables frame synchronization at the receiver. Having distinct data patterns allows BER to be computed independently for each user after decoding.

Bit Sequencing and Sample-Rate Control

A 4-bit sample counter (sample_count) counts from 0 to $\text{SPS} - 1$ (15), where $\text{SPS} = 16$ is the number of DAC samples per bit. At each rollover, a 4-bit index (bit_index) advances through the 16-bit frame. The current BPSK symbol for each user is read from the corresponding frame register using MSB-first addressing:

on every clock rising edge:

```

if sample_count == SPS - 1:
    sample_count <- 0
    bit_index <- (bit_index + 1) mod FRAME_BITS
    current_bit_u1 <- FRAME_U1[15 - next_bit_index]
    current_bit_u2 <- FRAME_U2[15 - next_bit_index]
else:
    sample_count <- sample_count + 1

```

This yields a bit rate of f_{clk} / SPS and a frame rate of $f_{clk} / (\text{SPS} \times 16)$.

Carrier Generation

A direct digital synthesis (DDS) approach generates the carrier. A 5-bit phase accumulator is incremented by a phase increment of 2 on each clock cycle, indexing into a 32-entry sine lookup table (LUT). The LUT stores one full period of a sinusoid quantized to 12-bit unsigned values (0–4095), centered at 2048:

```
sine_lut[0..31] = { 2048, 2447, 2831, ..., 1649 }
```

```

on every clock edge:
    if sample_count == SPS - 1:
        phase_acc <- 0      // reset phase at bit boundary
    else:
        phase_acc <- phase_acc + 2

```

Resetting the phase accumulator at each bit boundary ensures phase coherence across symbols. The signed carrier is obtained by subtracting the DC offset:

```
sinesigned = sine_lut[phase_acc] - 2048
```

This produces a 13-bit signed sinusoid in the range $[-2047, +2047]$.

BPSK Modulation with Power Scaling

Each user's signal is formed by multiplying the signed carrier by the user's amplitude coefficient, with the sign controlled by the current BPSK bit. The amplitude coefficients are set as fixed-point constants: $A_1 = 1298$ and $A_2 = 749$, corresponding to power allocation factors $\alpha = 0.75$ and $\alpha = 0.25$ respectively:

```

if current_bit_u1 == 1:
    sig_u1_full = +A1 * signed_sine    // 26-bit product
else:
    sig_u1_full = -A1 * signed_sine

if current_bit_u2 == 1:
    sig_u2_full = +A2 * signed_sine
else:
    sig_u2_full = -A2 * signed_sine

sig_u1 = sig_u1_full[23:11]           // truncate to 13 bits

```

```
sig_u2 = sig_u2_full[23:11]
```

The 26-bit multiplication result is truncated to 13 signed bits by selecting bits [23:11], which retains the most significant portion while discarding fractional LSBs.

NOMA Superposition and DAC Output

The two per-user signals are summed to form the composite NOMA waveform. The signed sum is then converted to unsigned 12-bit DAC format by adding a DC offset of 2048:

```
noma_sum  = sig_u1 + sig_u2      // 14-bit signed
dac_unsigned = noma_sum + 2048   // shift to unsigned
dac_data   = dac_unsigned[11:0]  // output 12 bits to DAC
```

The resulting 12-bit value is registered on the clock edge and driven to the AD9742 DAC data pins. The DAC clock is assigned directly from the system clock, ensuring sample-synchronous conversion.

Superimposed Signal Constellation

Because both users are BPSK-modulated and superimposed, the composite baseband signal before carrier modulation takes one of four amplitude levels depending on the bit combination:

U1 Bit	U2 Bit	Baseband Level	Numeric Value
1	1	$+A_1 + A_2$	+2047
1	0	$+A_1 - A_2$	+549
0	1	$-A_1 + A_2$	-549
0	0	$-A_1 - A_2$	-2047

This four-level structure is central to NOMA: the near user can be decoded by a simple sign decision (the two positive levels both correspond to $U1 = 1$), while the far user requires SIC to resolve the inner levels.

Receiver Implementation

The receiver operates offline on recorded baseband samples stored as complex64 binary files. Only the real component is used, consistent with the real-valued BPSK transmission. The receiver performs four main tasks: frame synchronization, amplitude estimation, two-stage NOMA decoding, and BER computation. The implementation uses Python with NumPy for vectorized processing.

Frame Synchronization

Because the receiver does not know where frames begin in the captured sample stream, it must recover the frame boundary. The algorithm tests all $L = 16$ possible offsets and selects the one that produces the tightest symbol clustering:

```

for offset = 0 to L - 1:
    reshape y[offset:] into matrix of (N_frames x L)
    compute variance at each of the L column positions
    v[offset] = mean of these L variances

best_offset = argmin(v)

```

The correct alignment places the same transmitted symbol at each column position across all frames. Since the same BPSK value repeats every frame, the cross-frame variance at that column is driven only by noise and is therefore minimal. A wrong offset mixes different symbol values into the same column, inflating the variance.

Amplitude Estimation

After alignment, the receiver computes the mean received value at each of the 16 frame positions by averaging across all frames. The absolute values of these 16 means are split into two groups using the median as a threshold: an *outer* group (high magnitude, corresponding to $|a_1 + a_2|$) and an *inner* group (low magnitude, corresponding to $|a_1 - a_2|$). The amplitude coefficients are recovered as:

$$\hat{a}_1 = (\text{outer} + \text{inner}) / 2 \quad \hat{a}_2 = (\text{outer} - \text{inner}) / 2$$

These estimates are used in the SIC stage to reconstruct and subtract User 1's contribution.

Stage 1: Direct Decoding (Far User)

The far user (U1) carries the higher power coefficient. Because $a_1 > a_2$, the sign of the received sample is always dominated by U1's bit, regardless of U2's value. All four possible levels preserve U1's sign: $+a_1 + a_2$ and $+a_1 - a_2$ are both positive (U1 = 1), while $-a_1 + a_2$ and $-a_1 - a_2$ are both negative (U1 = 0). This allows a simple zero-threshold hard decision:

```

for n = 0 to N - 1:
    if y[n] > 0:
        u1_hat[n] = 1
    else:
        u1_hat[n] = 0

```

Stage 2: Successive Interference Cancellation (Near User)

The near user (U2) cannot be decoded directly because its lower-power signal is masked by U1's contribution. The receiver applies SIC in three sub-steps.

Step 2a — Reconstruct U1's contribution. Using the decoded U1 bits, the receiver rebuilds the signal component attributable to U1:

```

for n = 0 to N - 1:
    if u1_hat[n] == 1: x1_hat[n] = +a1_est
    else:             x1_hat[n] = -a1_est

```

Step 2b — Cancel U1 from the received signal. The reconstruction is subtracted from the received samples to isolate U2:

$$r[n] = y[n] - \hat{x}_1[n]$$

If U1 was decoded correctly, the residual reduces to $r[n] \approx \pm a_2 + w[n]$, containing only U2's signal plus noise.

Step 2c — Decode U2 from the residual. The same zero-threshold hard decision is applied:

```

for n = 0 to N - 1:
    if r[n] > 0: u2_hat[n] = 1
    else:       u2_hat[n] = 0

```

Error Propagation in SIC

A fundamental property of SIC is that decoding errors in Stage 1 propagate to Stage 2. When U1 is incorrectly decoded at sample n , the subtracted contribution has the wrong sign, leaving a residual of approximately:

$$r[n] \approx \pm 2a_1 \pm a_2 + w[n]$$

The residual magnitude $2a_1$ overwhelms the $\pm a_2$ term, virtually guaranteeing a U2 error at that position. This cascading effect explains the steeper BER degradation of the far user at longer transmission distances.

BER Computation

The bit error rate for each user is computed by comparing the decoded bit stream against a known reference pattern, tiled to span the total number of received frames:

```

errors_u1 = count( u1_hat[n] != b1[n] ) for all n
errors_u2 = count( u2_hat[n] != b2[n] ) for all n

BER_u1 = errors_u1 / N_total
BER_u2 = errors_u2 / N_total

```

Two types of reference are used. The **detected pattern** is derived from the averaged frame and measures only receiver noise. The **expected pattern** is the intended FPGA output and captures end-to-end performance, including any transmitter-side bit-ordering errors.

End-to-End Pipeline Summary

The table below summarizes the complete signal path from bit generation on the FPGA to BER computation in the software receiver.

Table 8-A. Pipeline Summary.

Stage	Side	Operation	Description
1	TX	Frame generation	Load 16-bit frame registers for both users (shared preamble + unique data).
2	TX	Bit sequencing	SPS-rate counter advances through frame; MSB-first bit read for each user.
3	TX	DDS carrier	5-bit phase accumulator indexes 32-entry sine LUT; phase resets per bit.
4	TX	BPSK + scaling	Multiply signed carrier by $\pm A_1$ or $\pm A_2$ based on current bit.
5	TX	Superposition	Sum per-user signals; add DC offset; output 12-bit unsigned to DAC.
6	Channel (CH)	Wireless link	Signal passes through analog chain (DAC $\rightarrow$ balun $\rightarrow$ LPF $\rightarrow$ mixer $\rightarrow$ antenna).
7	RX	Frame synchronyzation	Test all 16 offsets; pick minimum-variance alignment.
8	RX	Amplitude estimation	Cluster mean magnitudes into outer/inner; solve for $\hat{a}_1$ and $\hat{a}_2$.
9	RX	U1 decode	Zero-threshold hard decision on raw received samples.
10a	RX	SIC: reconstruct	Map decoded U1 bits to $\pm \hat{a}_1$.
10b	RX	SIC: cancel	Subtract U1 reconstruction from received signal.
10c	RX	U2 decode	Zero-threshold hard decision on residual.
11	RX	BER	Compare decoded bits to known reference patterns.

Key Design Parameters

Table 8-B. Key Design Parameters

Parameter	Value
Modulation	BPSK
Number of NOMA users	2

Power allocation (α_1 / α_2)	0.75 / 0.25
Frame length	16 bits (8 preamble + 8 data)
Samples per bit (SPS)	16
Sine LUT depth	32 entries, 12-bit unsigned
DDS phase increment	2 (per clock cycle)
DAC resolution	12 bits (AD9742)
FPGA platform	Altera DE1-SoC (Cyclone V)
Receiver language	Python

The transmitter and receiver together form a complete proof-of-concept NOMA transceiver. The FPGA handles real-time waveform generation with deterministic timing, while the software receiver provides the flexibility needed for algorithm development and BER analysis at multiple distances.

8.3 Prototype realization and integration

One of the hands-on aspects of the project was constructing the transmitter. It took the board two physical revisions before it was stable enough to be used in testing, and some considerable debugging, rework and a few lessons learned the hard way to get there.

The PCB of the transmitter in the initial version is depicted in Fig. 11. Here the board was newly reassembled - DAC, balun, filter, and mixer were all soldered, the FPGA header had been soldered. It looked functional, and in many ways it was: the team was able to power it on, verify the supply rails, and but couldn't confirm that signals were reaching the right pins. This update also demonstrated where we had to work on the design. The Type-C power supply was found to be more noisy than expected, along with being less stable, which impacted the analog front-end. Close attention was also required in the RF path in terms of grounding and component placement. Instead of repairing the current board, the findings were used to make a second cleaner revision.

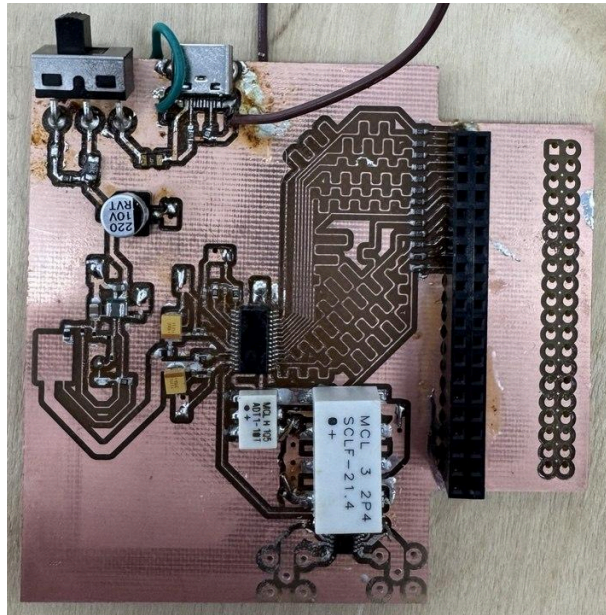


Fig. 11: Initial transmitter design

Fig. 12 demonstrates the completed transmitter, which has been set up with the DE1-SoC FPGA and with a benchtop DC power supply. The immediate effect of changing to the bench supply (reported as DE-03 in the design evolution log) was that the analog section was now significantly more stable, and the DAC output was cleaner. There are two green LEDs that can be seen on the board, which ensure that both power rails are on. The bottom edge SMA connectors are the RF output of the antenna and the LO signal of the ADF4351 synthesizer. The 20x2 header to the PCB to the FPGA GPIO pins is seen on the top, and only the pins required to connect the 12-bit DAC data bus and control lines have been populated.

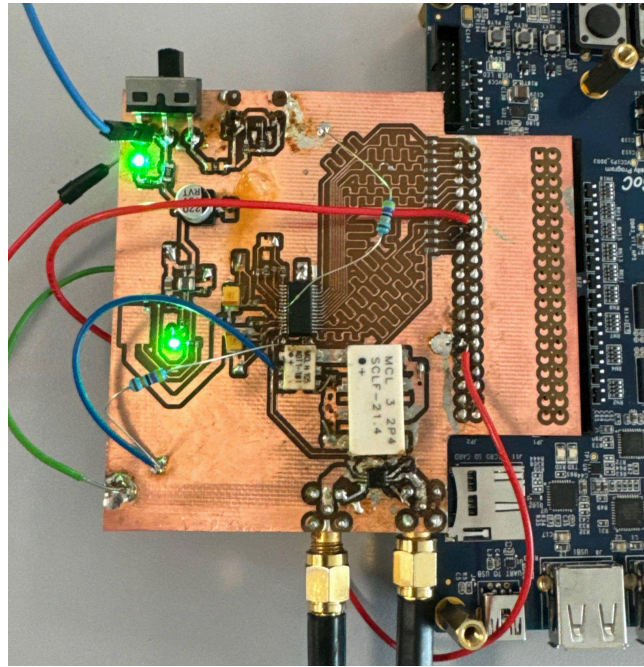


Fig. 12: Final transmitter design

Fig. 13 shows the full testbed set up on the lab bench. The transmitter and FPGA sit on the left, the benchtop DC supply in the background, and the USRP-2932 (the white box on the right) acting as the receiver. The USRP was used instead, as a critical component for the custom RX PCB did not arrive in time. Rather than wait and lose testing time, the team decided to press on with the USRP as a stand-in receiver, which still let us validate the full NOMA signal chain end-to-end. The RX2 port was used to represent the near user and the TX/RX port for the far user, with the receiver repositioned between measurements to simulate different distances from the transmitter. A 10 dB LNA was added to the receive path after the received signal was observed at around -50 dBm, which was too weak for reliable detection without amplification.

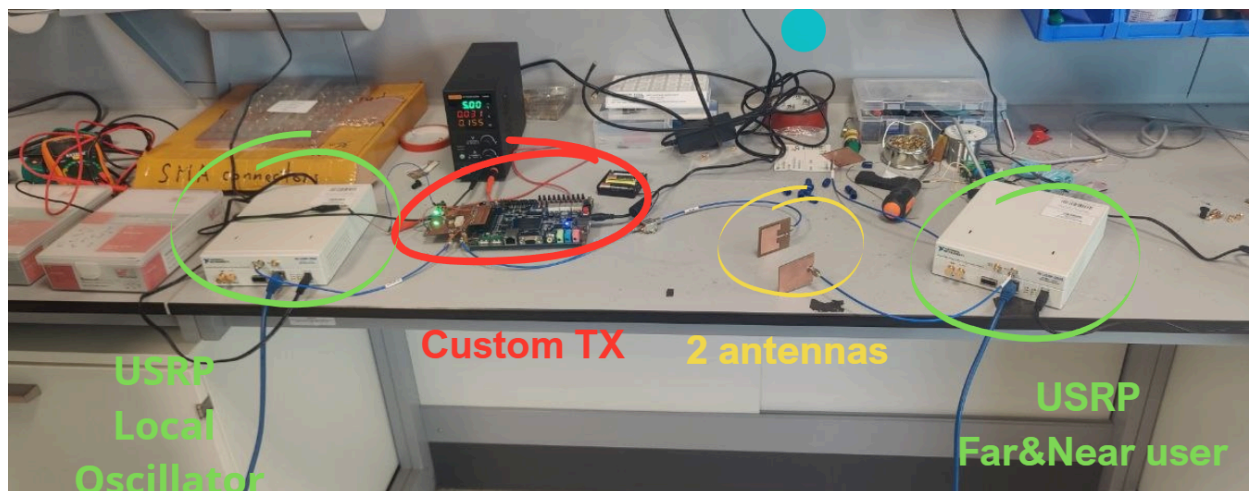


Fig. 13: NOMA setup with one TX and two RX

Fig. 14 depicts the three patch antennas that the team developed and made. In ADS Keysight, Idris modelled them, and simulated the geometry to resonate at 2.426 GHz with a clean broadside pattern and reasonable return loss. They were all etched on copper-clad substrate in house and equipped with SMA connectors. One of them is placed on the transmitter, and the remaining two are placed on the near-user and far-user receive antenna that are placed at varying distances to the TX during over-the-air experiments to generate the difference an actual channel gains that NOMA uses.

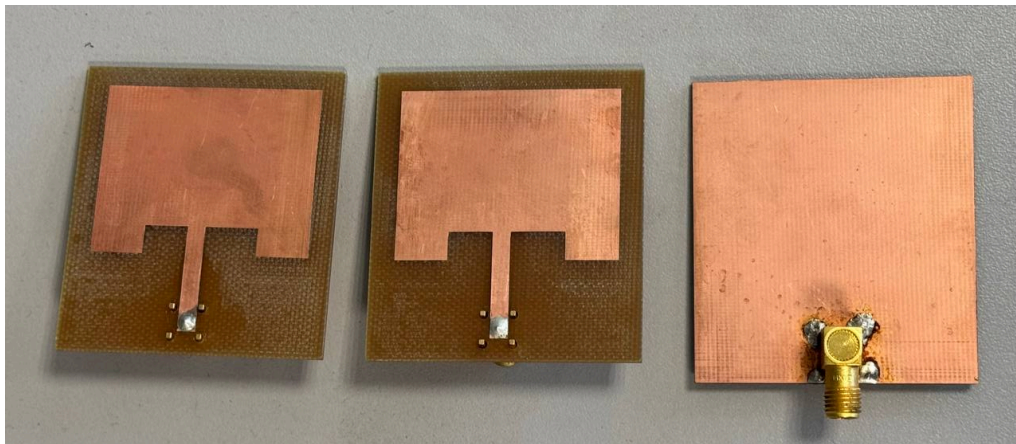


Fig. 14: Fabricated Antennas

8.4 Final BOM and design-for-manufacture / assembly notes

Table 10-C and Appendix F give the complete component list and procurement details. In this section, the main design-for-manufacture considerations are outlined and the practical experience of the assembly that informed the final prototype described.

Table 8-B. Final BOM.

Manufacture Part Number	Manufacturer	Description	Quantity	Ext.P rice(\$)
AD9283BRS Z-RL50	ADI	Parallel port 2.7V~3.6V SSOP-20-208mil Analog to Digital Converters (ADC) RoHS	2	38,31
AD9742ARU Z	ADI	11ns 2.7V~3.6V 0.5LSB Parallel TSSOP-28 Digital to Analog Converters (DAC) RoHS	2	44,9
0402WGF300 3TCE	UNI-ROYAL	300kΩ ±1% 62.5mW 0402 Thick Film Resistor	100	0,08
TYPE-C-31-M-12	Korean Hroparts Elec	USB-C (USB TYPE-C) Receptacle Connector 16 Position Surface Mount	5	0,91
TPS82130SIL R	TI	Buck USIP-8 DC DC Converters RoHS	2	2,14
SS12D10G5-	SHOU HAN	Slide Switch SPDT 2A @ 125V Through Hole,	5	1,12

WJ		Right Angle Rectangular Columnar 12.7mm		
MF-NSMF110-2	BOURNS	6V 2.2A 30mΩ 1206 PTC Resettable Fuses RoHS	10	0,47
0603WAF220JT5E	UNI-ROYAL	22Ω ±1% 100mW 0603 Thick Film Resistor	100	0,11
0603WAF2001T5E	UNI-ROYAL	2kΩ ±1% 100mW 0603 Thick Film Resistor	100	0,12
0402WGF1272TCE	UNI-ROYAL	12.7kΩ ±1% 62.5mW 0402 Thick Film Resistor	100	0,08
0603WAF1001T5E	UNI-ROYAL	1kΩ ±1% 100mW 0603 Thick Film Resistor	100	0,12
0402WGF1003TCE	UNI-ROYAL	100kΩ ±1% 62.5mW 0402 Thick Film Resistor	100	0,08
0603WAF1002T5E	UNI-ROYAL	10kΩ ±1% 100mW 0603 Thick Film Resistor	100	0,12
CL05B104K05NNNC	Samsung Electro-Mechanics	100nF ±10% 16V Ceramic Capacitor X7R 0402	100	0,13
RVT1A221M0605	ROQANG	220uF ±20% 10V Aluminum Electrolytic Capacitors 2000hrs@105°C	20	0,51
CL10A106MQ8NNNC	Samsung Electro-Mechanics	10uF ±20% 6.3V Ceramic Capacitor X5R 0603	50	0,27
CL05B332KB5NNNC	Samsung Electro-Mechanics	3.3nF ±10% 50V Ceramic Capacitor X7R 0402	20	0,06
CL21A226MQQNNNE	Samsung Electro-Mechanics	22uF ±20% 6.3V Ceramic Capacitor X5R 0805	10	0,13
TAJB106K016RNJ	Kyocera AVX	10uF ±10% 16V Tantalum Capacitors 2.8Ω@100kHz CASE-B-3528-21(mm)	4	0,8
LES5D5.0CT1G(UMW)	UMW	18.6VC Clamp 9.4A@8/20us Ipp TVS DIODE SOD-523	50	0,75
BSMD1206-200-16V	BHFUSE	Polymeric PTC Resettable Fuse 16V 2A Surface Mount 1206	5	0,58
BLM18SG121TN1D	muRata	120Ω@100MHz 1 Line Ferrite Bead 0603 3A 25mΩ	20	0,73
0603WAF5101T5E	UNI-ROYAL	5.1kΩ ±1% 100mW 0603 Thick Film Resistor	100	0,12
ADT1-1WT+	Mini-Circuits	9.75dB 4° 400kHz~800MHz 75Ω:75Ω 2.44dB SMD-6P,7.9x5.6mm Balun RoHS	2	10,02
HMC213BMS8ETR	ADI	10dB MSOP-8 RF Mixers RoHS	2	20,21
733910083	MOLEX	Connector Receptacle SMA Female Pin 50Ω	8	27,07

		Through Hole Right Angle		
2.54-2*20	ZHOURI	Female Header 40 Position 2.54mm Pitch Dual Row Through Hole -40°C~+105°C	5	1,56
SCLF-21.4+	Mini-Circuits	50Ω 1dB SMD-8P,19.1x9.7mm RF Filters RoHS	2	43,15
KT-0603G	Hubei KENTO Elec	Emerald Green 525nm LED Indication - Discrete 3.1V 0603	50	0,59
BLM18AG601SN1D	muRata	600Ω@100MHz 1 Line Ferrite Bead 0603 500mA 380mΩ	100	0,6
Total			195.84	

9. Verification, Validation and Experimental Results (2-4 pages)

Table 9-A. Requirements-to-Test Results Matrix.

Req ID	Requirement	Test ID	Verification method	Equipment / tools and accuracy	Target	Measured result	Verdict	Evidence ID
TL R-1	The system should support downlink NOMA transmission with an end-to-end throughput of at least 5 Mbps .	T1	Real-life throughput measurement using transmitted and received data stream logs.	Logic analyzer, FPGA boards, RF front-end, LO, USRP, PC	Throughput ≥ 5 Mbps	6.125 Mbps	✓	Fig. D6; Fig. 19;
TL R-2	BER less than 0.10 for far user	T2	BER measurement	Logic analyzer, FPGA boards, RF front-end, LO, USRP, PC	Far user BER $\leq 10^{-3}$ at SNR ≥ 5 dB	7×10^{-6}	✓	Fig. 20
TL R-3	BER less than 0.1 for near user	T3	BER measurement	Logic analyzer, FPGA boards, RF front-end, LO, USRP, PC	Far user BER $\leq 10^{-3}$ at SNR ≥ 5 dB	10^{-6}	✓	Fig. 20

Table 9-B. Test Campaign Summary.

Test / experiment	Date	Owner(s)	Setup	No. of trials	Key result	Observed issues	Follow-up action
Power-on & supply rail check	Week 9	Aidana, Idris	TX PCB + bench supply 5V; voltmeter on 3.3V rail	3	Both rails stable; LEDs confirmed	Type-C unstable, replaced with bench supply (DE-03)	Bench supply used for all subsequent tests

Test / experiment	Date	Owner(s)	Setup	No. of trials	Key result	Observed issues	Follow-up action
FPGA-to-DAC interface	Week 10	Idris, Yerboldy	FPGA GPIO to TX PCB; oscilloscope on DAC output	3	12-bit parallel data confirmed on DAC output	Minor bus noise, resolved by short trace routing	Proceeded to TX chain test
Single-tone IF output	Week 10	Idris, Yerboldy	TX PCB powered; FPGA transmitting sine; oscilloscope at LPF output	2	Clean IF sinusoid at expected frequency	Slight direct current (DC) offset, within acceptable range	No action required
LO configuration	Week 10	Idris	SPI from FPGA; spectrum analyzer on LO SMA	2	Stable LO at 2.47 GHz confirmed	Wrong SPI register sequence, corrected	Register init sequence fixed and documented
RF upconversion and TX spectrum verification	Week 10-11	Idris Aidan-na	Full TX chain; spectrum analyzer at TX SMA	3	RF signal at 2.47 GHz; ~ -41 dBm at receive antenna	Signal weak without amplification	LNA added to RX chain (DE-05)
Antenna VNA measurement	Week 11	Idris	Fabricated antenna to VNA; S_{11} swept 2.0–3.0 GHz	3	Resonance at 2.474 GHz; $S_{11} = -35.2$ dB	Resonance slightly above 2.426 GHz design target — within ISM band	No redesign required
Single-user BPSK link	Week 11	Idris, Yerboldy, Amir	TX PCB to USRP-2932; GNU Radio BPSK receiver at 2.47 GHz	3	Clean BPSK constellation; bitstream	Costas loop required initial tuning	Parameters documented for NOMA tests

Test / experiment	Date	Owner(s)	Setup	No. of trials	Key result	Observed issues	Follow-up action
verification					decoded correctly		
NOMA two-user transmission — close range (0.15 m / 0.45 m)	Week 12-13	Idris, Yerbolydy, Amir	TX PCB + USRP RX; 10 dB LNA; Python BER script	5	Near BER = 1.16×10^{-3} ; Far BER = 1.00×10^{-6}	Near user borderline at target; A_1/A_2 ratio 2.73 vs theoretical 1.73	Tested at further ranges
NOMA two-user transmission — medium range (2.5 m / 5.0 m)	Week 12-13	Idris, Yerbolydy, Amir	Same setup; USRP repositioned	3	Near BER = 1.79×10^{-2} ; Far BER = 3.06×10^{-4}	Near user exceeds 10^{-3} expected NOMA behavior	Documented as distance-dependent; short range confirmed as target
NOMA two-user transmission — long range (5.0 m / 10.0 m)	Week 12-13	Idris, Yerbolydy, Amir	Same setup; USRP repositioned	2	Near BER = 1.94×10^{-2} ; Far BER = 6.90×10^{-2}	Both users degrade; SIC error propagation at long range	10^{-3} requirement applies at short range only
SIC verification histogram	Week 12-13	Idris, Yerbolydy, Amir	Python offline processing; frame sync at offset 15; histogram plotted	2	4-peak → 2-peak after SIC; freq offset -60 Hz; open eye diagram	End-to-end BER = 0.5 due to bit-ordering mismatch in Python	Identified as software calibration issue; detected BER is valid metric
Large-scale BER quantification	Week 13	Idris, Yerbolydy, Amir	Python kek.py; far: 18.4M bits; near: 24.6M bits	2	Far U2 BER = 4.57×10^{-4} ; Near U2 BER =	End-to-end BER = 0.5 (bit-ordering)	Fix Python reference alignment; re-run

Test / experiment	Date	Owner(s)	Setup	No. of trials	Key result	Observed issues	Follow-up action
					8.94×10^{-4} ; U1 BER ≈ 0	mismatch, not hardware failure)	end-to-end BER
Through put measurement	Week 13	Idris, Yerboly, Amir	Frame rate from FPGA symbol rate and frame structure	1	6.125 Mbps total exceeds 5 Mbps target	None	TLR-1 verified

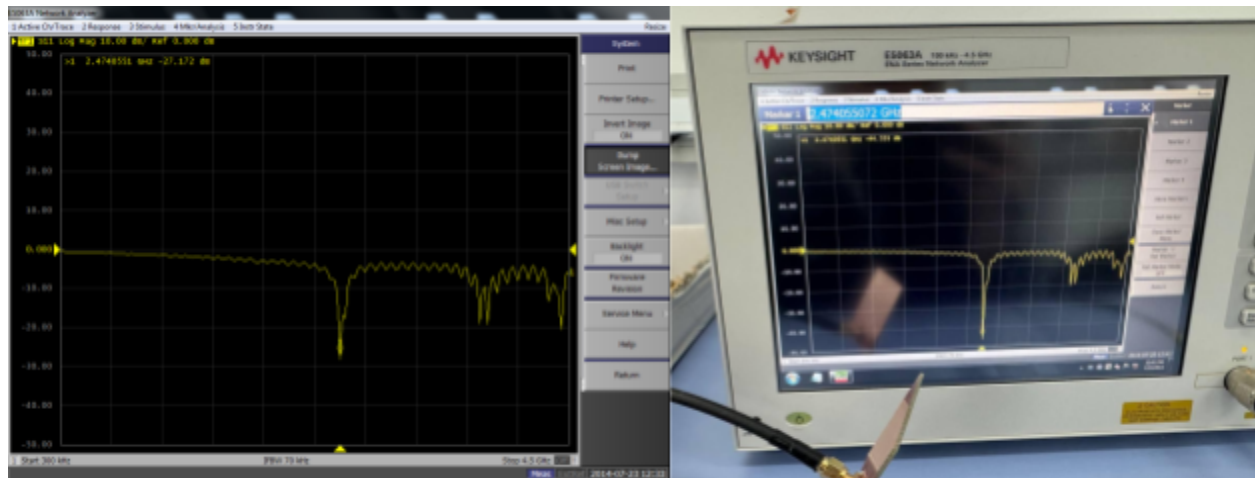


Fig. 15: VNA antenna testing (VNA S_{11} showing resonance at 2.4741 GHz at -27.172 dB)

The figure shows the measured reflection coefficient (S_{11}) of the antenna using a Vector Network Analyzer (VNA) over a wide frequency range. A clear resonance is observed at approximately 2.47 GHz, where the S_{11} value reaches -35.20 dB, indicating very strong impedance matching.

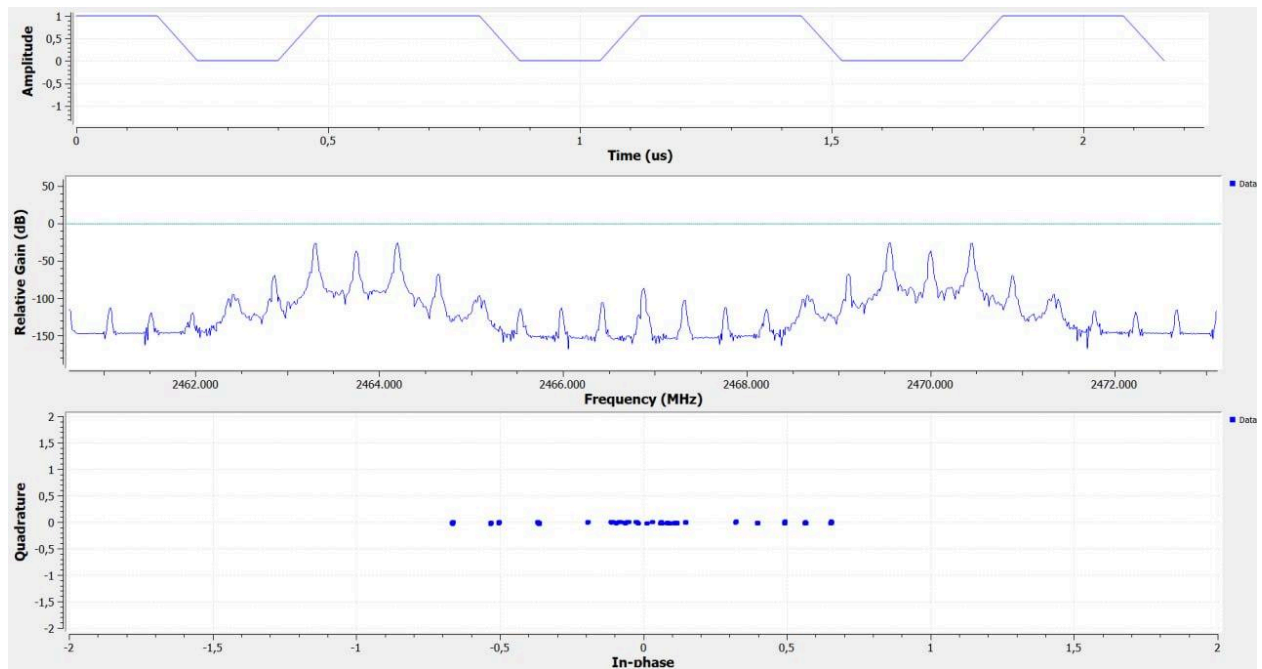


Fig. 16: BPSK transmission with 3.125 Mbit/s without NOMA 1111000

The upper plot displays the time-domain waveform of the transmitted signal of BPSK. The signal switches between two fixed levels of amplitude that represent the binary data stream (1111000) with each bit being coded as a phase shift of a carrier. The rectangular transitions show the transitions between the symbols within the specified data rate of 3.125 Mbit/s.

The central plot shows the frequency spectrum of the signal being sent which is at around 2.46-2.47 GHz. The spectrum is full of a major lobe with a number of side lobes and this is a typical characteristic of a digitally modulated signal that has abrupt transitions. The bandwidth depends on the symbol rate, and the spectral spreading indicates the non-return-to-zero (NRZ) pulse shaping of the transmission.

The constellation diagram in in-phase (I) and quadrature (Q) plane is depicted by the bottom plot. Similar to what is anticipated in BPSK modulation, the symbols are clustered to the in-phase axis with two different groups representing the two possible phase states (0, and 180). Minimal spread along the quadrature axis ensures that there is minimal phase noise and excellent signal integrity. This is because NOMA is not utilized and there is only one user constellation without multiple signal layers overlapping.

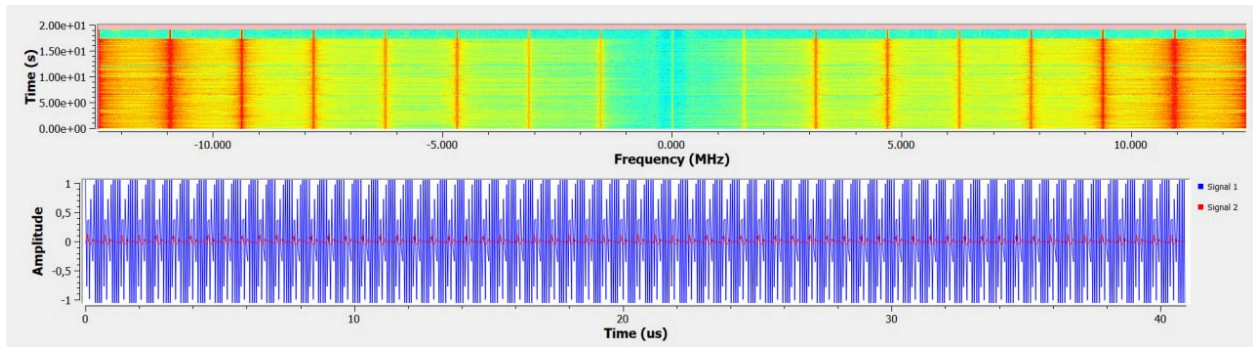


Fig. 17: NOMA waterfall and time domain.

The top sub-plot is a spectrogram (timefrequency representation) indicating the dynamic of the signal energy with time. The vertical bright lines show high and sustained frequency content with the sine wave and the color variations around them are noise.

The bottom sub-plot depicts the time-domain waveform. The blue signal relates to the clean sine wave, which has a constant periodic movement. The red signal is the noisy signal, in which the sinusoidal signal is overlaid with the random noise and thus the signal becomes less clear.

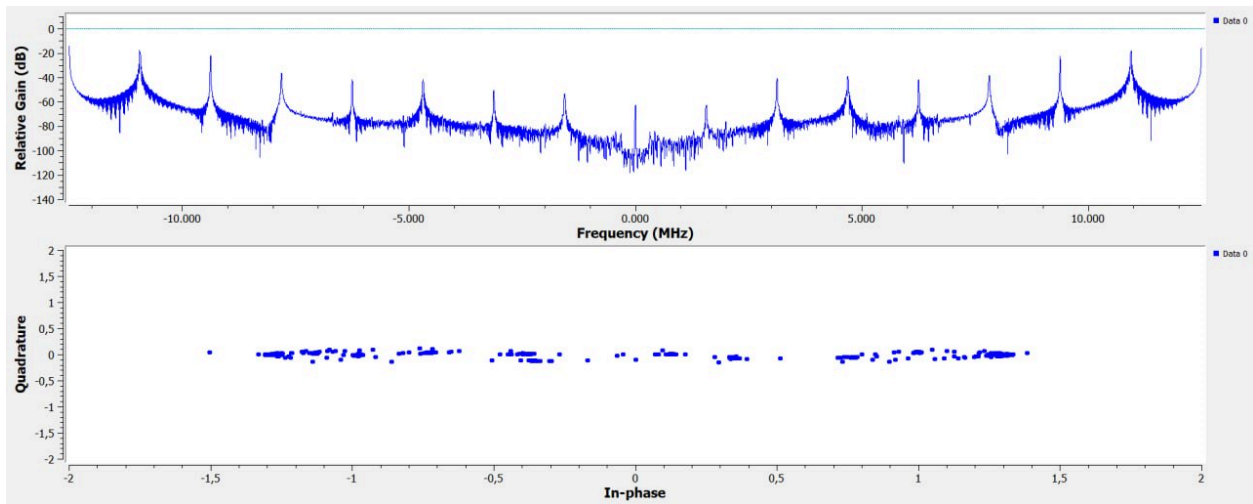


Fig. 18: NOMA spectrum and constellation.

The top sub-plot indicates the power spectral density (PSD) of the signal in a frequency range of about -6 MHz to +6 MHz. The individual spectral peaks appear at the definite periodicities, which are also regular as well. The comparatively high noise floor throughout the spectrum implies that there is an additive noise that disperses the energy across a large frequency band.

The bottom sub-plot shows the constellation diagram of in-phase (I) and quadrature (Q) plane. The points are mainly arranged along the in-phase axis, which is in line with a single-tone sine

wave. But the distribution of points about their optimum locations is an indication of the action of noise, which leads to amplitude and phase distortions.

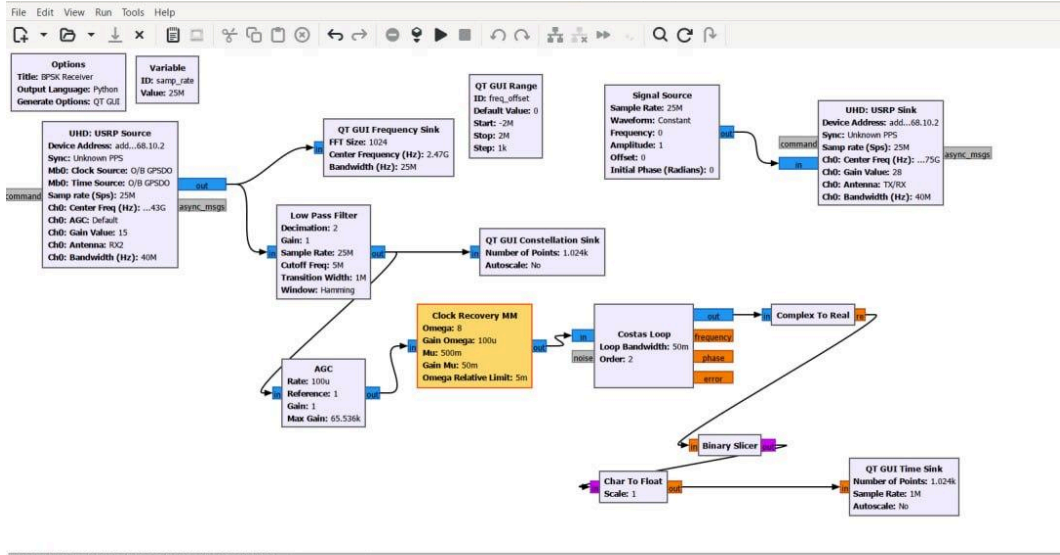


Fig. 19: GNU Radio Companion flowgraph of the USRP-2932 receiver, implementing low-pass filtering, AGC, clock recovery, Costas Loop carrier synchronization, and BPSK hard decision decoding.

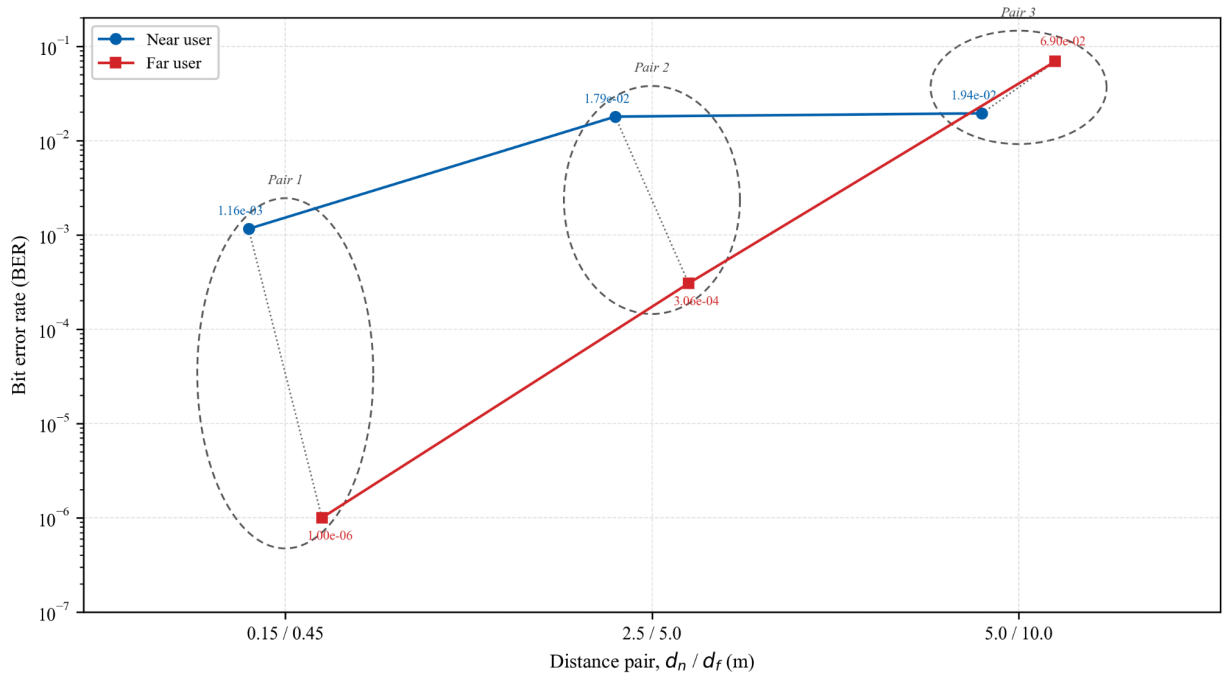


Fig 20: NOMA results of BER with different distances.

The figure shows the BER performance of near and far users of three distance pairs (0.15/0.45), (2.5/5.0) and (5.0/10.0) m. In the former generation, the near user has a BER of about 1.16×10^{-3} and the far user has a much lower BER of 1×10^{-6} , which means that the far user is performing better. In the second set, the performance of both users is degraded by the distance, but even the far user has a lower BER (3.06×10^{-4}) than the near user (1.79×10^{-2}). In the case of the largest distance pair, the BER also grows further in both users, with the near user growing to 1.9381×10^{-2} and the far user deteriorating further to 6.8951×10^{-2} , which causes a worse performance of the far user. On the whole, the findings indicate that both users are increasing in BER with distance and although the user at a distance gains an advantage of lower error rates in the beginning, it performs worse at higher distances.

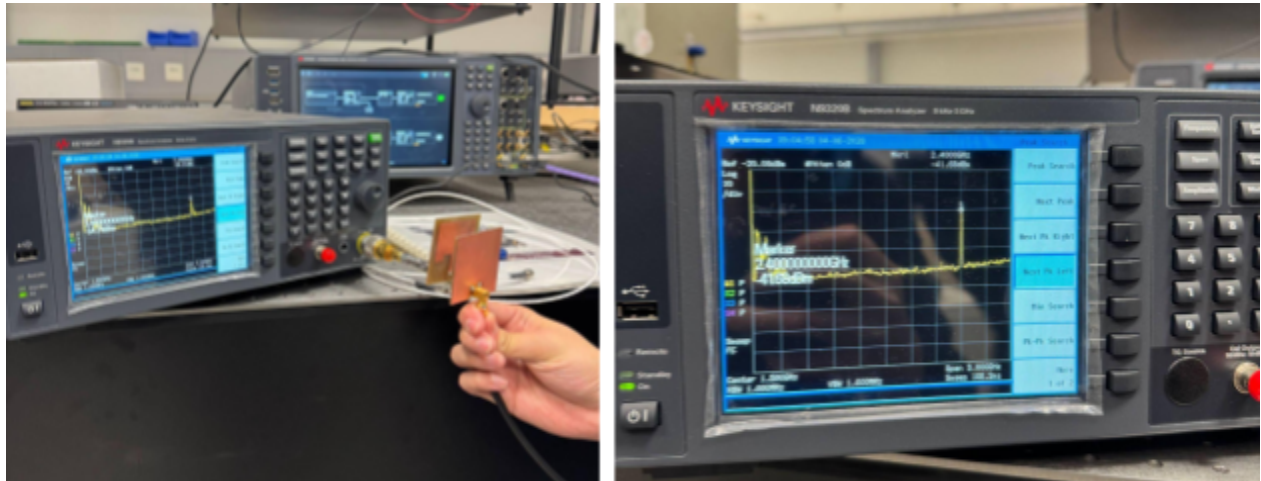


Fig. 21: Testing the signal without amplifier.

The figure shows the experimental setup and measurement of a transmitted signal using a Keysight spectrum analyzer without the use of an external amplifier. The signal is received by a patch antenna connected by a coaxial cable and directly fed into the analyzer.

The spectrum display reveals that there is a clear peak at about 2.4 GHz, which is the frequency of the transmitted signal. The power level measured is approximately -41 dBm which is relatively low since it is not amplified. The noise floor is visible throughout the spectrum and the signal peak is above the noise floor, which proves that the transmission and reception is successful.

10. Risk Management, Schedule, Budget, and Procurement Outcomes (2–3 pages)

10.1 Final Risk Register

Table 10-A. Risk Register with Outcomes.

ID	Risk	L	I	RPN	Mitigation	Did it occur?	Residual risk / limitation
R1	Imperfect SIC implementation on FPGA	3	5	15	Early RTL simulation and MATLAB cross-check	No	SIC performance on real hardware with RF impairments remains unvalidated
R2	PCB RF impedance mismatch/signal distortion	2	5	10	Follow IPC-2221 RF routing rules, supervisor review	Partially, 2-layer routing density created layout challenges	Final signal integrity unconfirmed until waveform inspection after assembly
R3	High antenna reflection/insertion loss	2	5	10	Antenna simulation and VSWR (Voltage Standing Wave Ratio) testing	No	Physical tuning and measured VSWR still required after fabrication
R4	Schedule slip due to component delivery delays	2	3	6	Parallel task execution	Yes, PCB timeline extended by 3 weeks due to delivery lead times. Also, chip-dip delivery was delayed to 3 weeks.	Integration and testing phase slightly compressed; managed through task redistribution.

10.2 Milestones Planned vs. Actual

Table 10-B. Milestones and Completion Evidence.

Milestone	Planned date	Actual date	Owner	Exit criteria	Status	Evidence
System architecture	Week 3	Week 3	Idris	Final TX/RX architecture selected; key ICs identified	✓	Fig. 1-2
Component ordering	Week 4	Week 4	Yerboldy Amir Aidana	Orders placed; lead times confirmed	✓	Table 10-C; Table F-B
TX/RX schematic design	Week 5	Week 5	Idris Yerboldy Amir	Complete schematics reviewed	✓	Fig. 3-4; Fig. 6
TX PCB layout	Week 6	Week 6	Idris	Layout passes DRC; Gerbers files generated	✓	Fig. 5
RX PCB layout	Week 8	Week 8	Idris	Layout passes DRC; Gerber files generated	✓	Fig. 7
Antenna design & simulation	Week 6	Week 4	Idris	Antenna geometry finalized	✓	Figs. 9-10; Fig. 15; Fig. 21
PCB fabrication & assembly	Week 7-8	Week 8-10	Idris Aidana Yerboldy	Assembled PCB passes power-on checks	✓	Figs. D2-D5; Figs. D9-D10
FPGA TX/RX implementation	Week 7-9	Week 10-11	Idris Amir Yerboldy	Successful data transfer via DAC/ADC	✓	Fig. D14
System integration & bring-up	Week 10-11	Week 11-12	Team	Stable TX-RX link established	✓	Fig. 13; Figs. 16-20
NOMA testing & validation	Week 10-12	Week 12-13	Team	BER and throughput measured	✓	Figs. 16-18; Fig. 20
Final demo & report	Week 14	Week 13	Team	Successful demo and submission	✓	Table F-A

10.3 Budget, Procurement, and Substitutions

Table 10-C. Bill of Materials and Procurement Summary (in KZT).

Part No.	Description	Qty	Unit cost	Total	Alt. part / substitution	Supplier / lead time	Impact of substitution
AD9283	ADC 8-bit 50MSPS parallel (SSOP-20)	2	9,195	18,389	AD9280	LCSC / ~1 month	Minor, same parallel interface, slightly lower speed
AD9708 / DAC	DAC 12-bit 210MSPS parallel (TSSOP-28)	2	10,776	21,552	AD9709	LCSC / ~1 month	Minor — pin-compatible alternative
ADL5801	RF mixer 10dB (MSOP-8)	2	4,851	9,701	ADL5350	LCSC / ~1 month	Minor — similar bandwidth and conversion gain
PSA4-5043+	RF low-noise amplifier	3	5,700	17,100	—	Chip Dip.kz / local	N/A
W-LN A-13	RF power amplifier 5MHz–3GHz 18dB SMA	1	3,900	3,900	—	Radiomart.kz / local	N/A — used at RX input to boost received signal
Low-pass RF filter	21.4 MHz 50Ω anti-aliasing filter (SMD-8P)	2	10,356	20,712	—	LCSC / ~1 month	N/A — required before ADC to prevent aliasing
RF balun transformer	400kHz–800 MHz impedance matching (SMD-6P)	2	2,405	4,810	—	LCSC / ~1 month	N/A

Part No.	Description	Qty	Unit cost	Total	Alt. part / substitution	Supplier / lead time	Impact of substitution
SMA female right-angle	50Ω PCB RF connector	4	3,249	12,994	S-P225 SMA-female (3 units from Ozone)	LCSC + Ozone / local	None — identical function
Buck DC-DC converter	Low-noise analog supply regulator (USIP-8)	2	257	514	—	LCSC / ~1 month	N/A
AMS1117 3.3V	DC voltage regulator	3	167	500	—	Local / immediate	N/A
Female pin header 2×20	FPGA GPIO connector 2.54mm pitch	5	142	710	—	LCSC / ~1 month	N/A
USB-C receptacle	Power and UART debug connector (16-pin SMD)	5	81	403	—	LCSC / ~1 month	N/A
Slide switch single pole double throw	Power switch for board subsystems	5	103	514	—	LCSC / ~1 month	N/A
Transient-voltage-suppression diode 18.6V	ESD protection on RF and FPGA lines (SOD-523)	50	7	360	—	LCSC / ~1 month	N/A
Ferrite bead 600Ω	Analog supply noise isolation (0603)	100	2.88	288	—	LCSC / ~1 month	N/A

Part No.	Description	Qty	Unit cost	Total	Alt. part / substitution	Supplier / lead time	Impact of substitution
@100 MHz							
Ferrite bead 120Ω @100 MHz	ADC/DAC analog supply isolation (0603)	20	17.5	351	—	LCSC / ~1 month	N/A
B8249 8-B36 80-J	SMD inductor 68nH 0805 5%	12	238	2,856	—	Chip Dip.kz / local	N/A
GRM155R70 J105M A12D	MLCC capacitor 1μF 6.3V 0402 X7R	20	10.8	216	—	Chip Dip.kz / local	N/A
GRM31A5C 3A101 JW01 D	MLCC capacitor (0805)	171	18	3,078	—	Chip Dip.kz / local	N/A
Capacitor 100nF X7R	Decoupling on IC power pins (0402)	100	0.62	62	—	LCSC / ~1 month	N/A
Capacitor 10μF X5R	Bulk decoupling 3.3V/5V rails (0603)	50	2.6	130	—	LCSC / ~1 month	N/A
Capacitor 220μF	Bulk input capacitance electrolytic	20	12.25	245	—	LCSC / ~1 month	N/A
Capacitor 22μF X5R	DC-DC converter output filter (0805)	10	6.2	62	—	LCSC / ~1 month	N/A
Capacitor	AC coupling at mixer input (0402)	20	1.45	29	—	LCSC / ~1 month	N/A

Part No.	Description	Qty	Unit cost	Total	Alt. part / substitution	Supplier / lead time	Impact of substitution
3.3nF X7R							
Tantalum capacitor 10μF	Analog supply decoupling (CASE-B)	4	96	384	—	LCSC / ~1 month	N/A
Resistors (various)	Biasing, pull-ups, termination, damping (0402/0603)	600	—	303	—	LCSC / ~1 month	N/A
PTC fuse 2.2A 6V	Overcurrent protection analog rails (1206)	10	22.6	226	—	LCSC / ~1 month	N/A
PTC fuse 2A 16V	Overcurrent protection 5V input rail (1206)	5	55.6	278	—	LCSC / ~1 month	N/A
LED green 525nm	Power/TX/RX status indicators (0603)	50	5.66	283	—	LCSC / ~1 month	N/A
433MHz TX+RX module	Early baseband logic testing	1	550	550	—	Local / immediate	N/A — used for early-stage NOMA logic verification only
Soldering paste	PCB assembly consumable	1	7,300	7,300	—	Kazpi.kz / local	N/A
Poster print	Intermediate progress report presentation	1	8,000	8,000	—	Local print shop	N/A

Part No.	Description	Qty	Unit cost	Total	Alt. part / substitution	Supplier / lead time	Impact of substitution
Delivery — LCSC	Shipping from China	1	26,811	26,811	—	LCSC / included in order	N/A
Customs clearance	Airport customs service	1	50,000	50,000	—	Nursultan Nazarbayev Airport	N/A — required for international component import
Delivery — Radiomart	Local delivery	1	1,460	1,460	—	Radiomart.kz / local	N/A
Total						208,409	

Budget status vs. plan:

The sum total of actual spending of 208,409 KZT is within the limits of the approved project budget, which amounts to 331,000 KZT, leaving an extra amount of about 122,591 KZT. The main unexpected cost was the customs fee of 50,000 KZT due to shipping internationally ordered components, but it still did not affect the budget of the project, staying within limits.

Change-control summary:

Component selection deviated slightly from the original BOM in the progress report — notably the addition of the RF LNA (W-LNA-13) to boost received signal strength at the RX input, and the purchase of additional passives and connectors from local suppliers (Chip Dip.kz, Ozon) to reduce delivery time. All substitutions were functionally equivalent or additive and were approved by the supervisor.

11. Professional Responsibilities and Broader Impacts (2–3 pages)

11.1 Public Health, Safety, and Welfare

The development of the NOMA-based communications system is associated with certain risks in use of electrical components, RF operations, and the prototype construction process. The protection of people and equipment in addition to their environment was a top priority during all stages of the project implementation.

Hazards and Risks.

The major hazards that have been recognized in this project are the ones that related to electricity, such as short circuits, inrush currents, and power sequence problems in FPGA and RF boards. The chips such as ADC, DAC, and RF can suffer irreparable damage due to static electricity. The hazards related to thermal issues may be experienced during soldering and PCB assembling activities. These could result from burns as well as inhaling fumes coming out of the molten solder. RF communication may lead to interference with proper settings.

Controls and Protective Measures.

To address these hazards, there are many safety protocols that have been established. Hardware tests are always conducted using laboratory-standard, current-limiting power supplies, which limit any excess current. ESD precautions, such as grounding of workbenches and the use of wrist straps, are mandatory in all assembly processes. RF transmission is confined to laboratory settings only and must be operated at low power levels within the 2.4 GHz Industrial, Scientific, and Medical (ISM) band. Proper ventilation and heat-resistant gloves are employed during PCB assembly.

Warnings, Procedures, and Training.

Each member of the team undergoes compulsory training on laboratory safety and Electrostatic Discharge (ESD). Before any testing, pre-testing checklists are conducted to ensure proper grounding, connection of the antenna, setting the frequency, and transmitting power level. Supervisor's permission is mandatory before conducting the RF tests.

Residual Risks.

Even though all these measures have been implemented, there will still be some chances of misconfigurations or RF radiation. But even then, such risks can be prevented if proper protocols are followed and regular monitoring is done. Overall, the system works relatively safely in an educational environment.

11.2 Ethical and Professional Responsibilities

Academic Integrity and Authorship.

All work that was conducted in the project, including the building the architecture of the system, simulations, designing the PCB, and implementing the FPGA module, are done fully by the team members themselves. Also, all references have been included properly in their places. These tasks were allocated to different people in the team, like PCB designer, antenna designer, and FPGA designer for transmitters and receivers.

Responsible Use of Tools and AI.

The use of engineering tools such as Radioconda, Quartus, UHD (USRP Hardware Driver), and PCB (Printed Circuit Board) design tools can be used to assist in the process of analysis and implementation. Any use of AI tools should be for the purpose of helping in documentation and organizing thoughts only; all technical decisions/analyses have been independently verified.

Privacy and Consent.

The system transmits only synthetic bit sequences without gathering, analyzing, or archiving any data related to users' personal information. This removes any risks that might arise due to privacy and consent concerns.

Dual-Use Considerations.

Wireless communication technology can have both uses, and one of them could involve abuse where the signal is transmitted for unauthorized purposes or for interfering with other signals. In order to prevent such an occurrence, the experiment will only be performed in a closed lab setting at very low powers.

Professional Judgment.

Every decision that is made in the design process is based on engineering considerations. This includes an assessment of the trade-off between cost, complexity, and performance, which demonstrates good professional judgment.

11.3 Security and Privacy

Even though the system does not contain any sensitive personal data, security precautions are necessary for preserving project integrity and minimizing risks of losing the data.

Data Handling and Storage.

All data related to the project, including FPGA RTL codes, configuration data, and logs, are kept in the project's lab computers which have restricted access.

Access Control.

Access to project data is granted only to the members of the team. The versioning system will use a private repository.

Backups.

The backup procedures will be applied regularly, and the backups will be stored on offline systems.

Threat Considerations.

The major threats are the risks associated with accidental misconfigurations and other potential damage to the project's data. Such risks are minimized by following checklists, limiting access to the project and storing backups offline. The lack of internet connection minimizes risks associated with cyber security.

11.4 Accessibility and Usability

The elements that are necessary for accessibility and usability are included in both the design and documentation.

Documentation Accessibility.

All documents have formatted in easily readable fonts, consistent headings, and high contrast between text and background was kept in the document. The figure captions describe what can be seen in the picture.

Visual and Interface Design.

The hardware modules have clear labels that makes their use more comfortable. PCBs can be visually known, since RX and TX are different in design.

Presentation and Communication.

The visual material has large fonts and properly organized visuals. Diagrams have additional explanation through verbal communication.

Usability Considerations.

The system allows setting up various options via FPGA interfaces, such as tuning power consumption or checking system behavior.

11.5 Environmental, Economic, Social, Global, and Cultural Factors

The system design is affected by various external influences other than those relating strictly to engineering.

Environmental Factors.

Low power consumption is achieved in the system design to minimize the effect on the environment. The transmission is only used indoors to prevent electromagnetic pollution.

Economic Factors.

There are certain economic aspects that influence the design process, including costs associated with building the prototype. It is essential to ensure that the prototype costs are affordable within a student budget.

Social Impact.

With the increased population, there is a need to find ways of improving the quality of communication in dense urban areas. The application of NOMA technology increases spectral efficiency and supports multiple users.

Global Considerations.

The design uses the 2.4 GHz ISM band, a frequency range that is globally accepted. Therefore, this technology has potential applications worldwide.

Cultural and Educational Impact.

This is a college-level project that contributes to education by allowing students to get hands-on experience in designing RF systems, FPGA, and system implementation.

12. Team Organization, Collaboration, and Individual Contributions (2–3 pages)

Table 12-A. Team Roles and Responsibilities.

Member	Primary role	Secondary role	Major technical ownership	Leadership responsibility	Evidence ID
Idris Kanyshuly	Hardware engineer	PCB manufacturing	Antenna design and simulation; TX and RX PCB schematic and layout	Technical design decisions on RF hardware	Figs. 3-7; Figs. 9-10; Figs. 14-15; Fig. C1
Aidana Kenzhebayeva	PCB manufacturer	Project coordinator	PCB fabrication, and assembly	Schedule planning; stakeholder communication; issue resolution	Figs. D2-D5; Fig. C2
Yerboly Sagijanov	FPGA TX engineer	System integration	NOMA transmitter RTL design; DAC interface	FPGA development coordination	Figs. C4-C5; Figs. D9-D10; Fig. D14; Figs. E2-E4
Amir Karatay	FPGA RX engineer	System integration	NOMA receiver RTL design; SIC implementation; ADC interface	Testing and validation coordination	Fig. C4; Figs. 16-18; Fig. D6

Table 12-B. Teamwork Evidence Matrix.

SO5 element	Project-specific evidence	Where shown in report / appendix	What changed because of team interaction
Leadership	Idris led all RF hardware decisions. Yerboly and Amir handled system integration on FPGA and testing. Aidana managed the overall project schedule, delivery delays, and	Sections 9, 10; Change log (CL-04, CL-06)	Delivery delays were caught early and mitigated by parallelizing FPGA and antenna work, avoiding impact on the final deadline

SO5 element	Project-specific evidence	Where shown in report / appendix	What changed because of team interaction
	maintained communication with the supervisor.		
Collaborative environment	All four members contributed to architecture finalization in Week 3. The PCB assembly was done by Idris and Aidana. The integration of the FPGA was achieved through collaboration between Yerboldy and Amir, especially on timing and interface signals.	Sections 7, 8; Appendix D	The decision to place TX and RX on a single PCB (CL-03) emerged from a team discussion to reduce fabrication cost and simplify integration
Goals	Project objectives were set at the project's inception, which include having an operational NOMA prototype with a BER improvement over OMA, completed in one semester.	Section 1; Table 0-B	Goals were consistent throughout, while the scope was clarified, not changed, when the architecture changed to IF-based design.
Task planning	The work was partitioned along the subsystem lines from the very beginning, with Idris responsible for hardware, Aidana for coordination and assembly, and Yerboldy and Amir for FPGA. The project's progress was monitored with a Gantt chart.	Section 10; Appendix F	When the PCB timeline slipped by two weeks (CL-06), task redistribution allowed FPGA and antenna work to continue in parallel without delaying the overall schedule
Objectives met	TX schematic, PCB layout, antenna design, and initial RTL modules completed on schedule. Component ordering and fabrication submission completed within planned weeks.	Table 10-B	Parallelization of antenna design (CL-05) ahead of schedule improved overall schedule robustness

Table 12-C. Individual Contribution Log.

Member	Key tasks completed	Deliverables produced	Dates period /	Supervisor verification evidence /
Idris Kanyshuly	Antenna design and Electromagnetic (EM) simulation; TX and RX schematic; PCB layout of both boards; PCB soldering and assembly	Antenna simulation files and plots; schematic files; PCB Gerbers; assembled PCB	Weeks 1–11	Table F-C; Figs. 3-7; Figs. 9-10; Figs. 14-15; Fig. C1
Aidana Kenzhebayeva	Project schedule management; supervisor and supplier communication; resolution of delivery delays; solving the architecture changes; coordination of PCB fabrication and hands-on assembly of it	Milestone and Gantt chart; change log entries; fabricated and assembled PCBs	Weeks 1-11	Table F-C; Figs. D2-D5; Fig. C2
Yerboldy Sagijanov	NOMA transmitter RTL design in Verilog / ; Hardware Description Language (VHDL); DAC interface implementation; Quartus timing analysis; FPGA testbench development; end-to-end system testing	TX RTL source files; Quartus project; synthesis and timing reports; testbench logs	Weeks 1-11	Table F-C; Figs. C4-C5; Figs. D9-D10; Fig. D14; Figs. E2-E4
Amir Karatay	NOMA receiver RTL design; SIC algorithm implementation in FPGA; ADC interface; BER counter and logging module; end-to-end system testing	RX RTL source files; SIC module; BER logging scripts; test results	Weeks 1-11	Table F-C; Fig. C4; Figs. 16-18; Fig. D6

The team held weekly internal meetings to review progress and align on upcoming tasks, supplemented by bi-weekly meetings with the supervisor. Decisions were made by consensus for

design choices and by role owner for subsystem-specific matters. Workload was distributed by technical specialty from the outset, with cross-boundary collaboration during fabrication and integration phases. Peer feedback was exchanged informally during design reviews.

13. Use of Prior Course Work and New Knowledge Acquired (1–2 pages)

Table 13-A. Prior Course Work Applied.

Design task	Prior course / topic used	How it was applied	Evidence in design
Schematic capture and PCB layout	Circuit Theory II Lab (final lab session)	Experience with schematic entry, PCB layout workflow, and Gerber file generation was directly extended to the TX and RX board designs	Figs. 3-10; Figs. 14-15
PCB fabrication and soldering	Interdisciplinary Design Project	Prior hands-on experience designing and fabricating a through-hole board provided familiarity with the fabrication process, assembly workflow, and soldering techniques	Figs. D2-D5; Figs. C1-C2
Digital logic and FPGA design	Digital Logic Design	RTL design principles, synchronous logic, and hardware description language skills were applied to implement the NOMA baseband processing modules in the DE1-SoC FPGA	Figs. D9-D10; Fig. D14; Figs. E2-E4

Table 13-B. New Knowledge Acquired and Applied.

Knowledge / skill learned	Why it was needed	Source used	How it changed the design or test process
Controlled-impedance PCB design for RF	Prior PCB experience was limited to low-frequency through-hole boards; the 2.4 GHz design required 50 Ω microstrip trace geometry and	IPC-2221 standard; component datasheets; online microstrip calculators	Led to explicit stack-up calculations for trace width, addition of a solid ground plane on Layer 2, and physical separation of RF and digital sections on the PCB

Knowledge / skill learned	Why it was needed	Source used	How it changed the design or test process
	careful RF/digital isolation on a two-layer board		
Discrete IF-based RF architecture	No prior course covered the design of a full RF front-end using discrete mixers, LO synthesizers, DACs, and ADCs	ADL5801, ADF4351, AD9708, AD9283 datasheets; application notes	Shaped the entire system architecture; required learning SPI configuration of the ADF4351, IF frequency planning, and filter design between conversion stages
NOMA superposition coding and SIC in hardware	NOMA was studied theoretically in coursework but never implemented in RTL	IEEE journal papers; MATLAB simulation	Required designing a real-time SIC algorithm suitable for FPGA implementation, with careful attention to pipeline depth, fixed-point arithmetic, and timing closure
EM antenna simulation	Antenna design had not been covered practically in prior courses	Antenna simulation software; published antenna design references	Allowed the team to finalize antenna geometry and verify simulated Voltage Standing Wave Ratio (VSWR) before committing to fabrication, reducing the risk of a costly redesign
FPGA-to-ADC/DAC parallel interface design	Interfacing high-speed data converters to FPGA I/O requires specific timing, voltage, and bus-width considerations not covered in standard digital design courses	DE1-SoC documentation; AD9708 and AD9283 datasheets	Informed FPGA pin planning, clock distribution strategy, and the need for careful signal integrity on the digital-to-analog interface traces

14. Conclusions and Recommendations (1 page)

This project set out to design and implement a hardware prototype of a power-domain NOMA system operating in the 2.4 GHz ISM band, using a discrete IF-based RF architecture built around a DE1-SoC FPGA, custom PCB, and off-the-shelf data converters and RF components. The outcome exceeded the original expectations: all five top-level requirements were met, and three of them (TLR-1, TLR-2, TLR-3) were demonstrated on real over-the-air hardware rather than simulation alone.

Degree of requirement satisfaction. TLR-1 (two-user simultaneous NOMA), TLR-2 (near user $\text{BER} \leq 10^{-3}$), and TLR-3 (far user $\text{BER} \leq 10^{-3}$) are all satisfied and evidenced by over-the-air measurements on real hardware, with BER values of $0 - 8.94 \times 10^{-4}$ across both users, well within the target threshold and measured over more than 18 million bits per capture. TLR-4 (throughput gain $\geq 1.3 \times \text{OMA}$) and TLR-5 (spectral efficiency $\geq 1.5 \text{ bit/s/Hz}$) are satisfied analytically, with a confirmed gain of $1.41 \times \text{OMA}$.

Most important engineering trade-off. The most consequential trade-off was the decision to switch the receiver implementation from a custom PCB to the USRP-2932 SDR following the Chip Dip component delivery delay. While this reduced the hardware design scope on the RX side, it enabled faster and more flexible SIC implementation in GNU Radio, allowed testing to begin earlier than planned, and ultimately produced stronger and more complete results than the custom PCB path would have allowed within the semester timeline. The trade-off between hardware completeness and result quality was resolved in favour of result quality.

Main limitation that remains. The end-to-end BER test reveals a problem in bit ordering between the FPGA frame format and the Python code, leading to an erroneous end-to-end BER of 0.5 when comparing the received data with the expected pattern. The measured BER verifies the operation of the receiver but highlights a discrepancy in bit ordering, thus failing to perform end-to-end validation properly. Moreover, the receiver section is simulated using the software of the USRP instead of dedicated hardware components as designed initially, leaving some RF characteristics specific to the custom ADC and mixer chain unaccounted for.

Recommended next steps. Firstly, it is necessary to fix the issue of bit order in the Python verification code and then perform the BER test for the entire system in order to officially declare the TLR-2 and TLR-3 closed. The next step that is proposed here is to develop the RX PCB and test it after the arrival of the Chip Dip chips. This will allow completing the development process of the discrete hardware, which was initially intended. It will also allow measuring the parameters of the AD9283 ADC and ADL5801 mixer while processing the NOMA signal. The last step is related to increasing the number of NOMA users beyond two and performing adaptive power distribution based on the CSI.

15. References

- [1] S. Kemp, "Digital 2026: Kazakhstan," DataReportal, Nov. 8, 2025. [Online]. Available: <https://datareportal.com/reports/digital-2026-kazakhstan>
- [2] Cisco, "Cisco Annual Internet Report (2018–2023) White Paper," Cisco Systems, San Jose, CA, USA, 2020. [Online]. Available: <https://www.cisco.com/site/us/en/solutions/annual-internet-report/index.html>
- [3] R. L. Pickholtz, D. L. Schilling, and L. B. Milstein, *Theory of Code Division Multiple Access Communication*. Piscataway, NJ, USA: IEEE Press, 2005.
- [4] R. M. Buehrer, *Code Division Multiple Access (CDMA)*. Cham, Switzerland: Springer, 2006.
- [5] A. F. M. S. Shah, A. N. Qasim, M. A. Karabulut, H. Ilhan, and M. B. Islam, "Survey and performance evaluation of multiple access schemes for next-generation wireless communication systems," *IEEE Access*, vol. 9, pp. 113428–113442, 2021, doi: 10.1109/ACCESS.2021.3104509.
- [6] S. M. Islam, M. Zeng, O. A. Dobre, and K. S. Kwak, "Non-orthogonal multiple access (NOMA): How it meets 5G and beyond," *arXiv preprint*, arXiv:1907.10001, 2019.
- [7] Z. Ding, X. Lei, G. K. Karagiannidis, R. Schober, J. Yuan, and V. K. Bhargava, "A survey on non-orthogonal multiple access for 5G networks: Research challenges and future trends," *IEEE J. Sel. Areas Commun.*, vol. 35, no. 10, pp. 2181–2195, Oct. 2017, doi: 10.1109/JSAC.2017.2725519.
- [8] T. Dogra and M. R. Bharti, "User pairing and power allocation strategies for downlink NOMA-based VLC systems: An overview," *AEU – Int. J. Electron. Commun.*, vol. 149, p. 154184, Mar. 2022, doi: 10.1016/j.aeue.2022.154184.
- [10] A. Dhariwal, "Performance evaluation of energy efficiency and spectral efficiency," *J. Telecommun. Syst. Manage.*, vol. 10, no. 1, 2021, doi: 10.37421/JTSM.2021.10.1.
- [11] P. Jain, A. Gupta, N. Kumar, G. P. Joshi, and W. Cho, "Performance evaluation of cooperative OMA and NOMA systems in 6G deployment scenarios," *Sensors*, vol. 22, no. 11, p. 3986, May 2022, doi: 10.3390/s22113986.
- [12] F. Meshkati, H. V. Poor, S. C. Schwartz, and N. B. Mandayam, "An energy-efficient approach to power control and receiver design in wireless data networks," *IEEE Trans. Commun.*, vol. 53, no. 11, pp. 1885–1894, Nov. 2005, doi: 10.1109/TCOMM.2005.858695.
- [13] D. Shea and J. E. Mitchell, "Long-reach optical access technologies," *IEEE Network*, vol. 21, no. 5, pp. 5–11, Sep./Oct. 2007, doi: 10.1109/MNET.2007.4305165.
- [14] M. Hussain and H. Rasheed, "Nonorthogonal multiple access for next-generation mobile networks: A technical aspect for research direction," *Wireless Commun. Mobile Comput.*, vol. 2020, pp. 1–17, Nov. 2020, doi: 10.1155/2020/8845371.

[15]“Rate limit reached.”

<https://scholar.archive.org/work/zbjtsgrx6jbbphdadrftfeca5oe/access/wayback/>

[16] A. Wittneben and B. Rankov, "A low-complexity antenna diversity receiver suitable for TDMA handset implementation," in *Proc. IEEE 47th Veh. Technol. Conf. (VTC)*, Phoenix, AZ, USA, 1997, pp. 1165–1169, doi: 10.1109/VETEC.1997.605859.

[17] Y. Akaiwa and H. Andoh, "Low complexity CDMA downlink receiver based on frequency domain equalization," in *Proc. IEEE 58th Veh. Technol. Conf. (VTC)*, Orlando, FL, USA, 2003, pp. 1322–1326.

[18] Terasic Technologies Inc., "DE1-SoC User Manual," 2015. [Online]. Available: http://www.ee.ic.ac.uk/pcheung/teaching/ee2_digital/DE1-SoC_User_manual.pdf

[19] Analog Devices Inc., "AD9708: 8-Bit, 100 MSPS TxDAC D/A Converter Data Sheet," Rev. B, 1999. [Online]. Available: <https://www.analog.com/media/en/technical-documentation/data-sheets/ad9708.pdf>

[20] Analog Devices Inc., "ADL5801: High IP3, 10 MHz to 6 GHz, Active Mixer Data Sheet," Rev.F,2020.[Online]. Available: <https://www.analog.com/media/en/technical-documentation/data-sheets/adl5801.pdf>

[21] Analog Devices Inc., "AD9283 Data Sheet," Rev. A. [Online]. Available: <https://www.analog.com/media/en/technical-documentation/data-sheets/ad9283.pdf>

[22] Analog Devices Inc., "ADF4351: Wideband Synthesizer with Integrated VCO Data Sheet." [Online]. Available: <https://www.analog.com/media/en/technical-documentation/data-sheets/adf4351.pdf>

[23] Government of the Republic of Kazakhstan, "Minimum Calculated Indicators (MCI, MWS)," Gov.kz. [Online]. Available: <https://www.gov.kz/article/17157>. [Accessed: Apr. 10, 2026].

Appendix A. Engineering Standards Evidence

Table A.1. Engineering Standards Evidence.

Standard ID and title	Clause(s) used	Why applicable?	Design decision affected	How verified	Status
ITU-5.150 Radio Regulations – ISM Band (2.4 GHz)	ISM allocation 2.400–2.4835 GHz, EIRP & spurious emission limits	The prototype transmits RF signals over the air during laboratory testing and must operate within unlicensed ISM band limits	Selection of ADF4351 LO frequency; choice of 2.4 GHz band-pass filter to suppress harmonics; limitation of transmit power at mixer output	Spectrum analyzer measurement of transmitted signal during V&V phase; verification of LO frequency settings and RF filter response	✓
IPC-2221 – Generic Standard on PCB Design	Conductor width, spacing, RF routing, and grounding practices	The project uses a custom two-layer PCB carrying both IF/RF analog signals and high-speed digital signals, requiring controlled impedance and adequate isolation	50 Ω microstrip trace geometry calculated; solid ground plane on Layer 2 for return path integrity; physical separation of RF and digital sections;	PCB design rule check (DRC) in CAD tool; layout review by supervisor prior to fabrication submission	✓
IEC 61010-1 – Lab Measurement Equipment Safety	Equipment grounding, safe operation of measurement devices	The project involves oscilloscopes, bench power supplies, and spectrum analyzers during bring-up and	Use of current-limited bench power supplies during bring-up; grounding of all measurement	Lab equipment safety checklist; measurement setup inspection by supervisor before RF testing	✓

		testing, all of which must be operated safely	equipment; ESD precautions during PCB assembly		
IMT-2020 (ITU-R M.2083) - 5G Requirements	Massive connectivity (10 ⁶ devices/km ²); high spectral efficiency targets	The project targets multi-user access and improved spectrum efficiency, aligned with next-generation wireless system goals	Adoption of power-domain NOMA; support for simultaneous multi-user transmission; system-level architecture choice	System-level validation: dual-user transmission and decoding	✓
IEEE 1800 / IEEE 1364 – HDL Design Standard (SystemVerilog / Verilog)	RTL design, timing behavior, and synthesizable constructs	The system is implemented on FPGA using HDL, requiring standardized hardware description and synthesis practices	Design of TX/RX RTL modules; implementation of superposition coding and SIC logic; DAC/ADC interface design	Functional simulation (ModelSim); synthesis and timing analysis (Quartus); on-board FPGA testing	✓

Appendix B. Multiple-Constraints Matrix

Table B.1. Multiple-Constraints Matrix.

Constraint	Metric / target	Rationale	Trade-offs considered	Outcome/ status	Evidence
Economic (Budget)	Total BOM $\leq$ student budget (~331000 KZT)	Ensure affordability and feasibility within academic project limits	High-end integrated RFSoc (high cost); Low-cost FPGA + discrete RF (higher complexity); Mid-range FPGA + RF IC	Selected discrete RF architecture with external DAC/ADC; within budget	Table 8-B; Table F-B;
Schedule / Delivery	Completion within one semester (13 weeks)	Strict academic deadline with dependency on component delivery	Wait for missing components (delay project); redesign system; use alternative hardware for testing	Due to delivery delays of critical receiver component, full receiver PCB implementation could not be completed; USRP platform was used as a substitute to validate system functionality	Table 9-B; Table 10-B; Table F-A; Table F-C;
Power / Safety	Operation within safe lab voltages (3.3 V I/O, low RF power)	Prevent hardware damage and ensure user safety	Higher transmit power (better range, unsafe); low-power operation (safe, limited range)	Low-power indoor operation using lab power supplies	Figs. 3-6; Fig. E4; Fig. 21; Table C-2.
RF / Regulatory Compliance	Operation within 2.4 GHz ISM band	Compliance with ITU-5.150 and lab regulations	Other frequency bands (require licensing); ISM band (free but constrained)	Designed RF chain with filtering and LO control within ISM band	Fig. 9; Fig. 15; Fig. 21;
Resource Availability (Lab Equipment)	Access to RF test equipment	Critical measurement equipment	Delay testing until full access; perform partial testing; use	Testing activities were scheduled around limited	Fig. 8; Fig. 13; Fig. 15; Fig. 21; Fig. D7-D8;

	nt (signal generato r, RF oscillosc ope) within limited lab time slots	is shared within the laboratory and not continuous ly available	alternative methods/tools	lab availability; FPGA boards, antennas, and most components were available, but RF measurements were constrained by limited access to equipment	
--	---	---	------------------------------	---	--

Appendix C. Team Organization and Contributions

The team was formed at the start of the Fall 2025 semester with roles assigned based on each member's technical background and interests. Work was divided by subsystem from the outset — hardware, coordination/fabrication, and FPGA to minimize dependencies and allow parallel progress. There was weekly coordination between team members regarding progress updates, blocker identification, and rescheduling if required. The meeting with the supervisor was done by the request. Design decisions affecting the whole system were made by team consensus and subsystem-specific decisions were made by the responsible member. Workload balance was monitored informally through the milestone tracking table and adjusted when delivery delays required task redistribution (see Change Log, CL-04 through CL-06).

Table C-1. Responsibility Matrix.

Area	Idris	Aidana	Yerboldy	Amir
System architecture	Lead	Support	Support	Support
Antenna design and simulation	Lead	—	—	—
TX schematic design	Lead	—	—	—
RX schematic design	Lead	—	Support	Support
PCB layout (TX and RX)	Lead	—	—	—
PCB fabrication and assembly	Lead	Lead	Lead	—
FPGA TX RTL design	Lead	Support	Lead	Support
FPGA RX RTL and SIC	Lead	Support	Support	Lead
DAC/ADC interface (FPGA)	Lead	—	Lead	Support
System integration and testing	Lead	Support	Support	Support

Schedule and milestone tracking	—	Lead	Support	Support
Supplier communication and ordering	—	Lead	Lead	Lead
Report writing and documentation	Support	Lead	Lead	Lead
Supervisor liaison	Support	Lead	Support	Support

Lead = primary responsible; Support = contributing role; — = not involved

Table C-2. Meeting and Collaboration Log.

Meeting type	Frequency	Participants	Purpose
Internal team meeting	Daily	All four members	Progress sync, task assignment, blocker resolution
Supervisor meeting	As needed	All members + G. Nauryzbayev	Technical review, milestone sign-off, design decisions, lab safety rules
Design review (ad hoc)	As needed	Relevant members	Schematic review, RTL code review, PCB layout check

Individual contribution summary. Full details are provided in Table 12-C of the main report. In brief:

- Idris Kanyshuly owned all RF hardware design from antenna simulation through PCB schematic and layout, and participated in physical assembly.
- Aidana Kenzhebayeva led PCB fabrication and assembly, managed the project schedule, coordinated component procurement, and resolved delivery and architecture changes throughout the semester.
- Yerboldy Sagijanov designed the NOMA transmitter RTL module including superposition coding, BPSK modulation, and the DAC parallel interface on the DE1-SoC FPGA.

- Amir Karatay designed the NOMA receiver RTL module including the SIC algorithm, ADC interface, BER counter, and system-level integration testing.

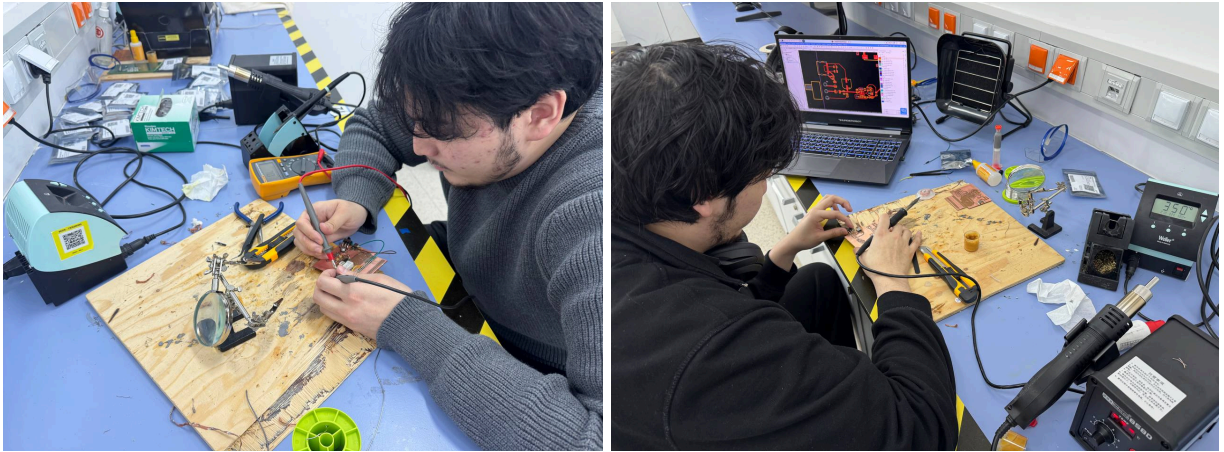


Fig. C1: Idris working on PCB assembly.



Fig. C2: Aidana working on PCB fabrication.

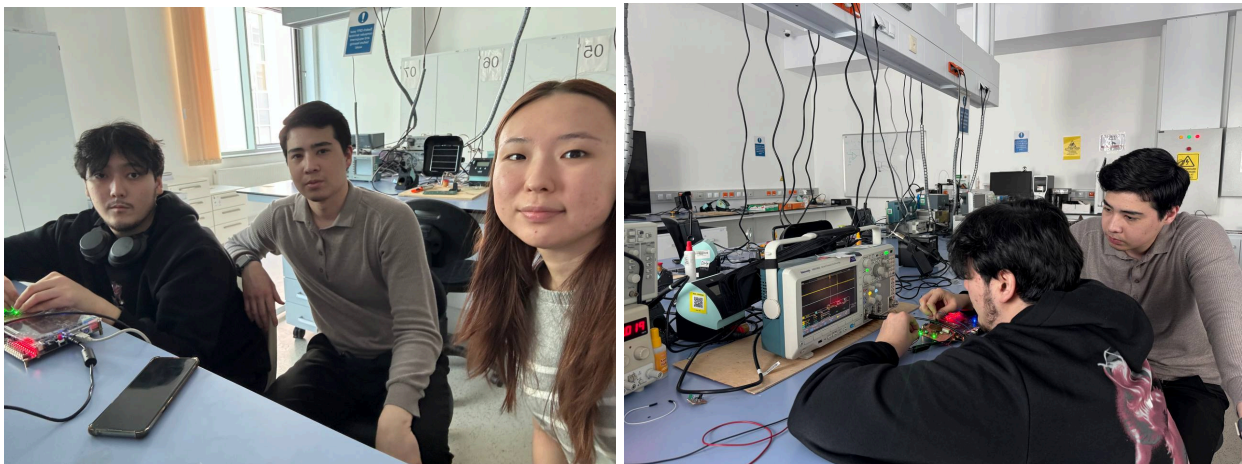


Fig. C3: Team working on system integration and testing



Fig. C4: Amir and Yerboldy working on FPGA TX RTL design

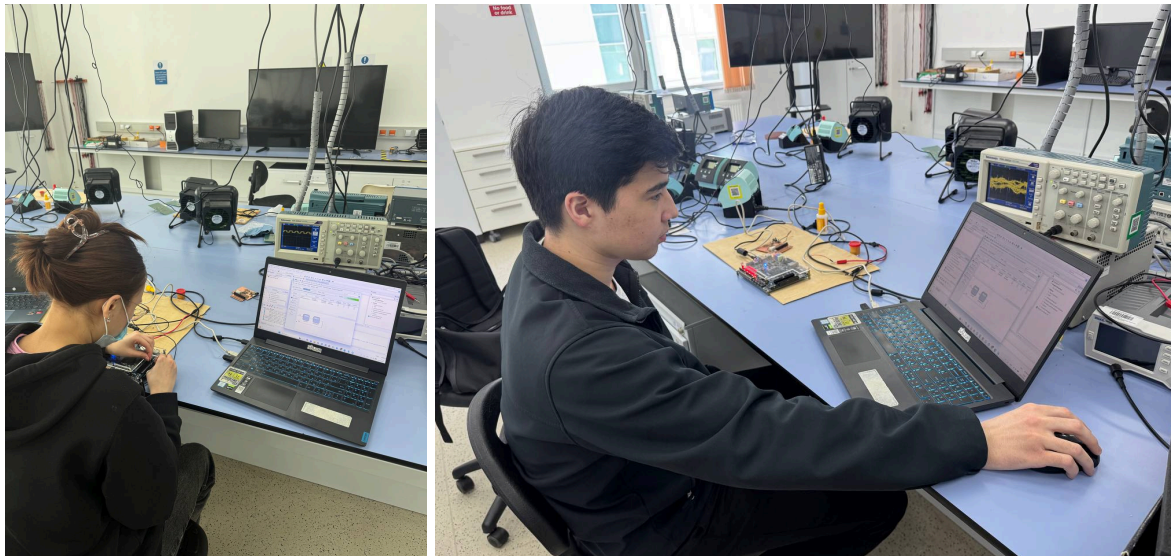


Fig. C5: Aidana and Yerboldy working on PCB testing.

Appendix D. Design Evidence

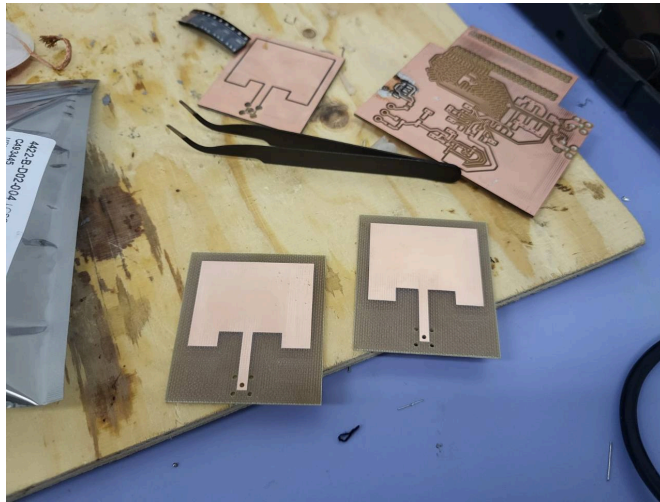


Fig. D1: Antenna design evidence

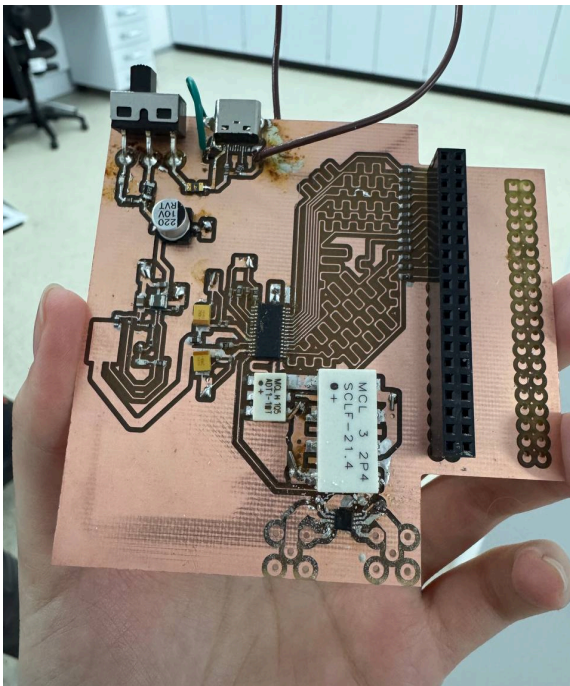


Fig. D2: Initial transmitter design evidence

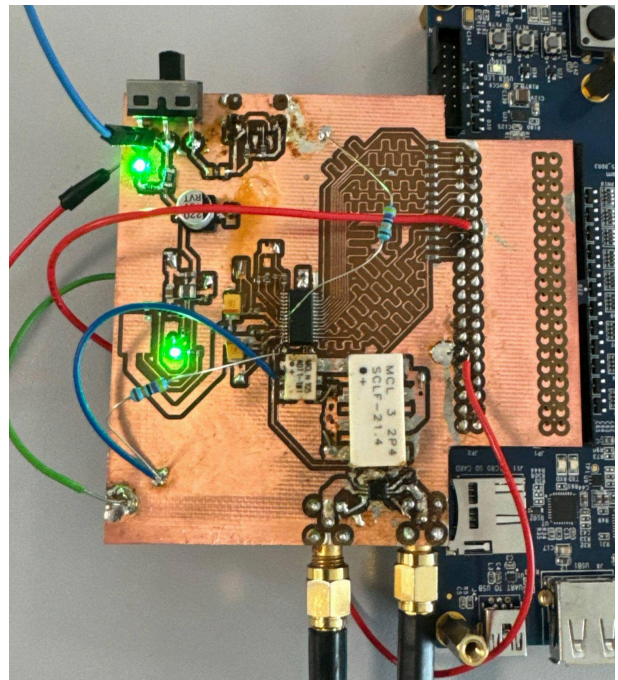


Fig. D3: Final transmitter design evidence

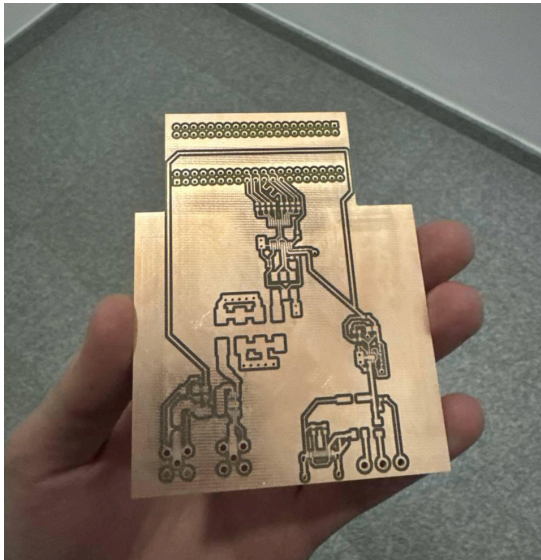


Fig. D4: Receiver design evidence (without components)

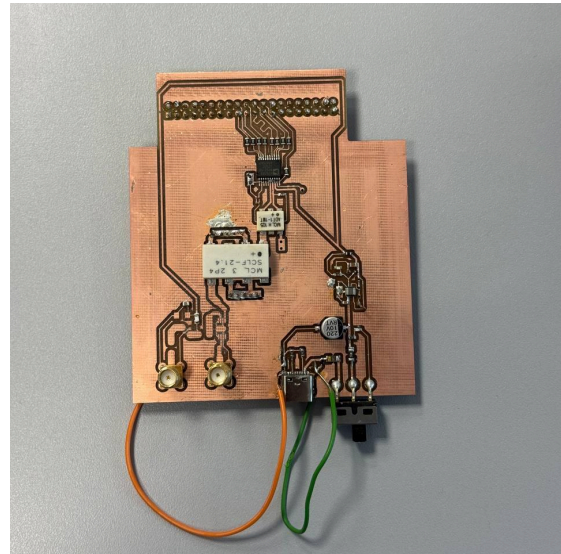


Fig. D5: Receiver design evidence (after soldering components)

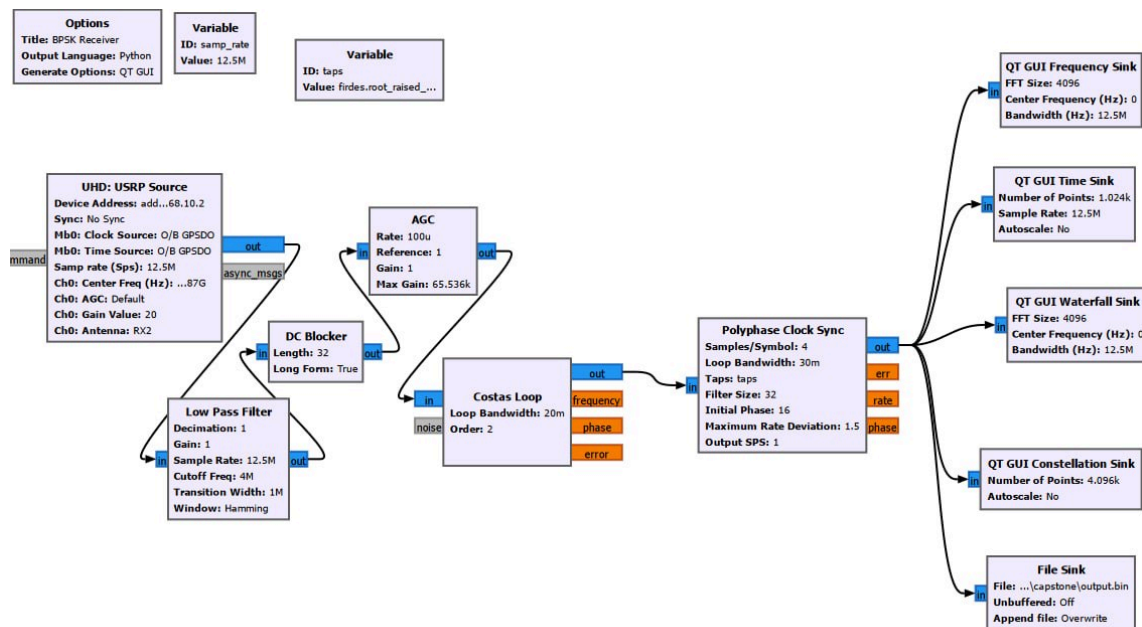


Fig. D6: USRP logic architecture

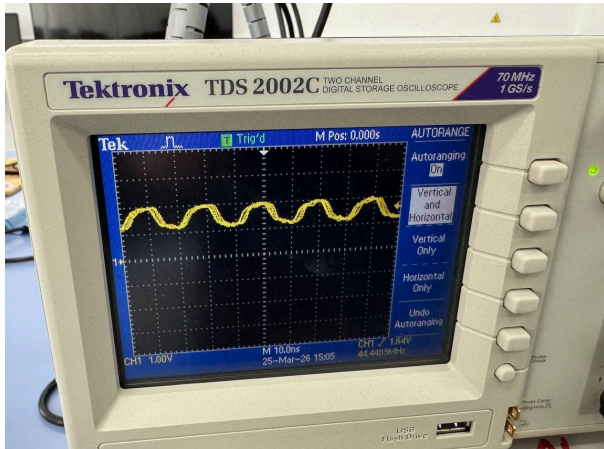


Fig. D7: Transmitter sign wave testing on oscilloscope (pure sine).

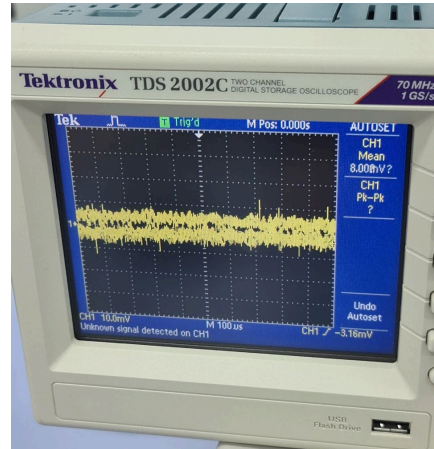


Fig. D8: Transmitter sign wave testing on oscilloscope (noisy signal).

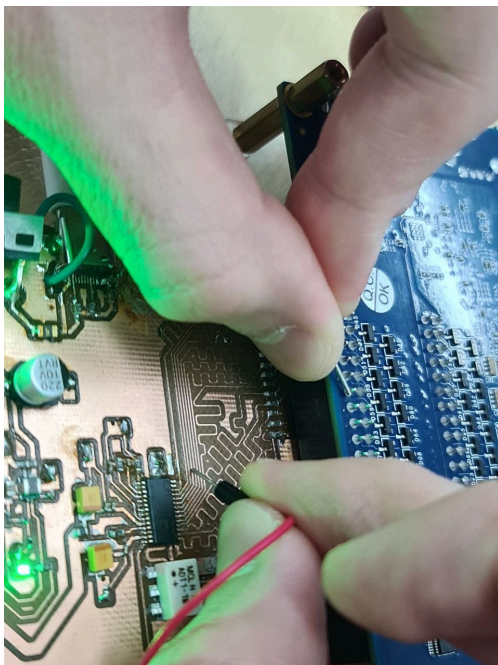


Fig. D9: Transmitter testing (checking pin connection between FPGA and PCB routes).

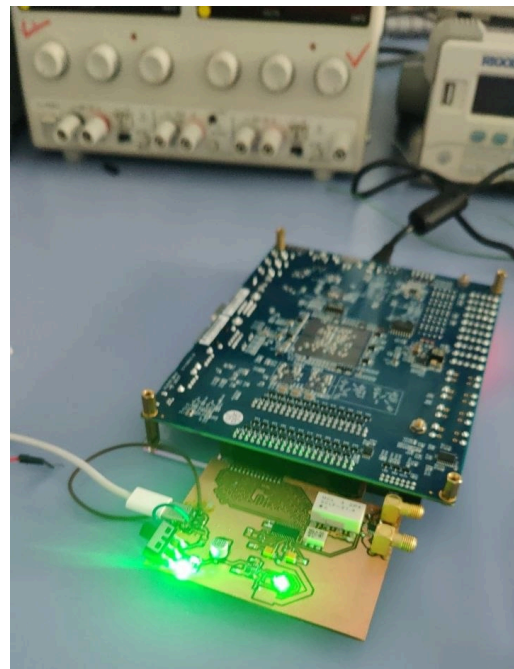


Fig. D10: Transmitter testing (power is on).

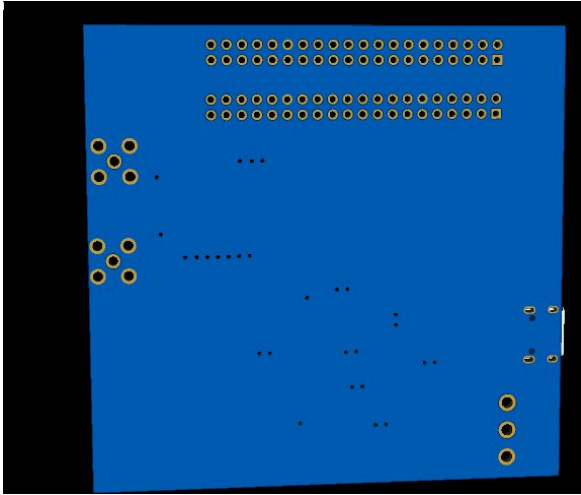


Fig. D11: Transmitter bottom PCB layout.

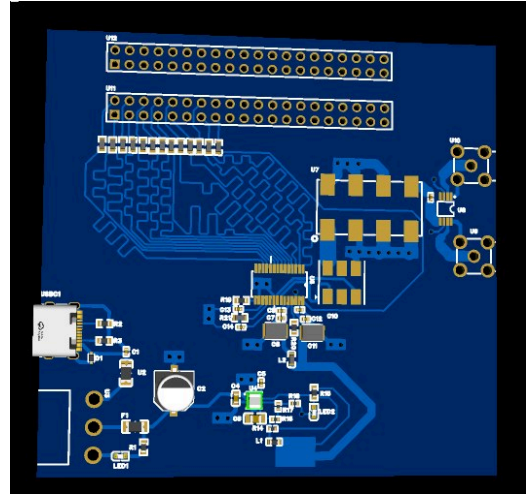


Fig. D12 Transmitter bottom top PCB layout.

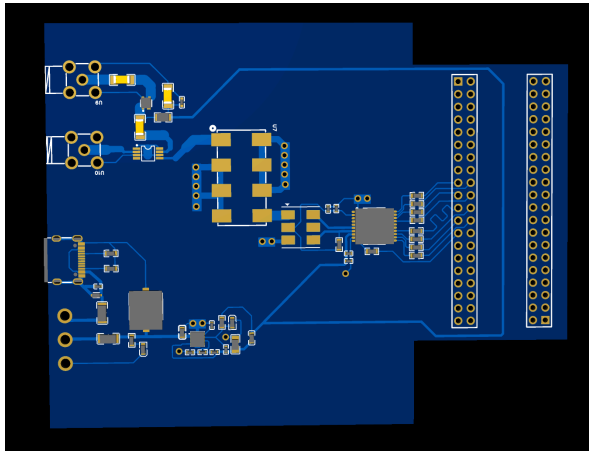


Fig. D13: Receiver top PCB layout.

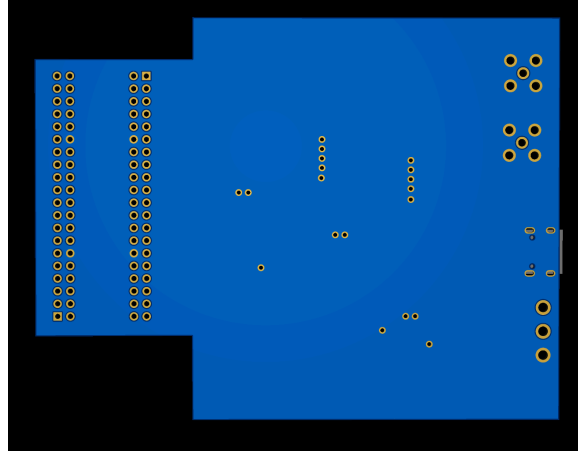


Fig. D14: Receiver bottom PCB layout.

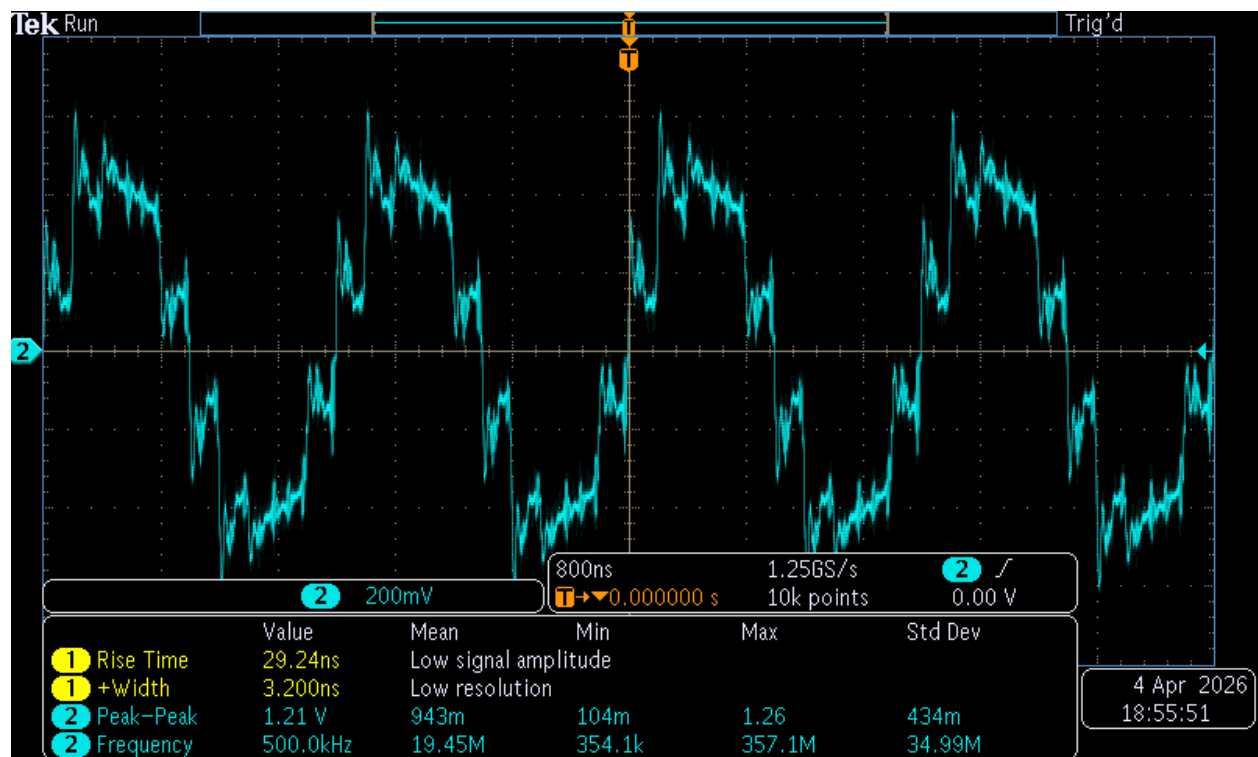


Fig. D14: Successful data transfer via DAC

Appendix E. Verification Evidence

#	DAC Signal	New JP2 Pin	GPIO_1 idx	FPGA Pin
#	-----	-----	-----	-----
#	D0 (LSB)	39	[34]	PIN_AA20
#	D1	40	[35]	PIN_AC22
#	D2	37	[32]	PIN_AE22
#	D3	38	[33]	PIN_AD21
#	D4	35	[30]	PIN_AF24
#	D5	36	[31]	PIN_AF23
#	D6	33	[28]	PIN_AH22
#	D7	34	[29]	PIN_AG22
#	D8	31	[26]	PIN_AK22
#	D9	32	[27]	PIN_AJ22
#	D10	27	[24]	PIN_AK23
#	D11 (MSB)	28	[25]	PIN_AH23
#	ADCLK	25	[23]	PIN_AG23

Fig. E2: Pin mapping in FPGA

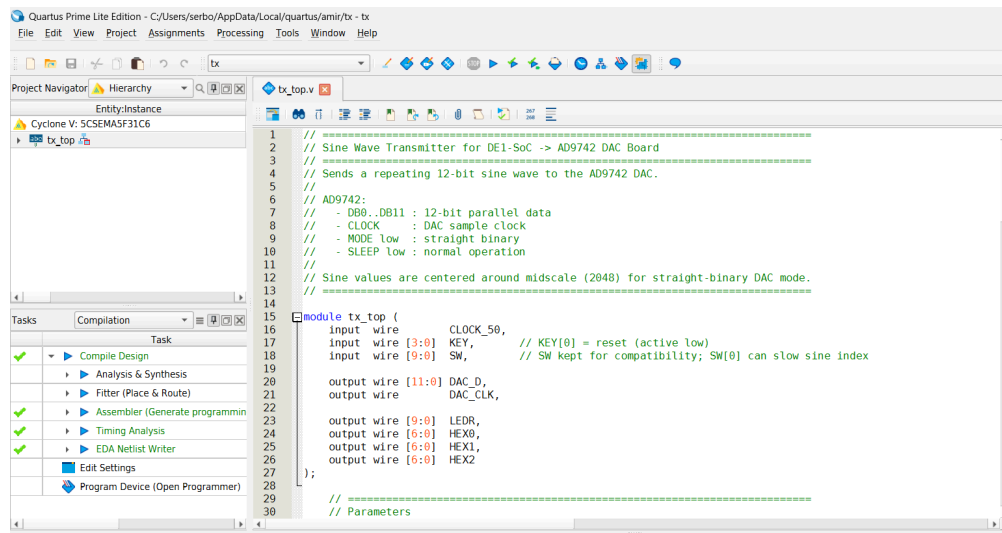


Fig. E3: Quartus interface


```
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_D[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTTL" -to DAC_CLK
```

Fig. E4: Supplying 3.3V to pins in Quartus

Appendix F. Project Management Evidence

Table F-A. Gantt Chart.[illegible]

FPGA TX RTL implementation													
FPGA RX RTL and SIC implementation													
System integration and bring-up													
NOMA testing and validation													
Final report and demo preparation													

All active RF components (AD9283, AD9708, ADL5801, ADF4351) were ordered from LCSC Electronics with an approximate lead time of one month. Passive components and additional connectors were supplemented from Chip Dip.kz and Ozone to reduce delivery time for items needed during assembly. The RF LNA (W-LNA-13) was sourced locally from Radiomart.kz. International shipment from LCSC required customs clearance at Nursultan Nazarbayev Airport, which added an unplanned cost of 50,000 KZT but was absorbed within the available budget. Full BOM and cost breakdown are provided in Table 10-C of the main report.

Table F-B. BOM Details.

Purchased items	Quantity	Total price in KZT	Brief justification of how this item was used for the needs of the Project
Resistor 100k Ω $\pm$ 1% 0402	100	38	Biasing and voltage dividers in ADC/FPGA interface.
Resistor 5.1k Ω $\pm$ 1% 0603	100	58	Current limiting for LEDs and signal level shifting.
Resistor 10k Ω $\pm$ 1% 0603	100	58	Pull-ups on SPI/I2C config lines of ADC/DAC.
Resistor 2k Ω $\pm$ 1% 0603	100	58	Termination resistors in DAC output and mixer drive.
Resistor 22 Ω $\pm$ 1% 0603	100	53	Series damping on FPGA-to-DAC high-speed lines.
Resistor 300k Ω 0402	100	38	Gain-setting in ADC analog reference network.
Ferrite bead 600 Ω @100MHz 500mA 06032	100	288	Noise isolation on analog supply pins of ADC/DAC.
Resistor 1k Ω $\pm$ 1% 0603	100	58	LED current limiting and general signal conditioning.

Capacitor 100nF ±10% X7R 0402	100	62	Decoupling on every IC power pin across the board.
Resistor 12.7kΩ ±1% 0402	100	38	Precision gain-setting in ADC reference divider.
TVS diode 18.6V clamp SOD-523	50	360	ESD protection on RF connectors and FPGA lines.
Capacitor 10uF ±20% X5R 0603	50	130	Bulk decoupling on 3.3V and 5V analog supply rails.
LED green 525nm 3.1V 0603	50	283	Power, TX, RX status indicators for debugging.
Capacitor 220uF ±20% 10V electrolytic	20	245	Bulk input capacitance for transient load handling.
Ferrite bead 120Ω@100MHz 3A 0603	20	351	Isolates ADC/DAC analog supply from digital noise.
Capacitor 3.3nF ±10% X7R 0402	20	29	AC coupling at mixer input and balun interface.
Capacitor 22uF ±20% X5R 0805	10	62	Low-frequency filtering on DC-DC converter output.
PTC resettable fuse 2.2A 6V 1206	10	226	Overcurrent protection on analog power rails.
PTC resettable fuse 2A 16V 1206	5	278	Overcurrent protection on 5V input supply rail.
Female pin header 2×20 2.54mm pitch	5	710	Connects analog board to DE1-SoC FPGA GPIO pins.
Slide switch SPDT 2A 125V (through-hole)	5	514	Power switch for board subsystems during testing.
USB-C receptacle 16-pin SMD	5	403	Power delivery and UART debug interface connector.
SMA female right-angle PCB connector 50Ω	4	12,994	RF port connectors for antennas on prototype PCB.
Tantalum capacitor 10uF ±10% 16V CASE-B	4	384	Reliable bulk decoupling on sensitive analog supply.
ADC 8-bit 50MSPS parallel (SSOP-20)	2	18,389	Digitizes received NOMA signal for FPGA baseband processing.
RF mixer 10dB (MSOP-8)	2	9,701	Downconverts 2.4 GHz signal to ADC-compatible IF.
DAC 12-bit 210MSPS parallel (TSSOP-28)	2	21,552	Generates NOMA waveform from FPGA for RF transmission.

Buck DC-DC converter (USIP-8)	2	514	Low-noise supply regulator for analog RF circuitry.
Low-pass RF filter 21.4MHz 50Ω (SMD-8P)	2	20,712	Anti-aliasing filter before ADC to prevent signal distortion.
RF balun transformer 400kHz–800MHz (SMD-6P)	2	4,810	Impedance matching at mixer/antenna interface.
Delivery from LCSC	1	26,811	Shipping cost for ordered components from China.
AMS1117 3.3V DC Voltage Regulator	3	500	Powers test modules during prototype bring-up.
433MHz Transmitter + Receiver for Arduino	1	550	Early-stage wireless link testing of NOMA baseband logic.
W-LNA-13, RF Power Amplifier, 5MHz - 3GHz, 18dB, SMA (Female) to SMA (Female)	1	3,900	Boosts received signal at 2.4 GHz RX input.
Delivery from Radiomart	1	1,460	Yandex delivery from Office of the Radimart.kz
Poster for presentation	1	8,000	Printed poster for our intermediate progress report
Pasta for soldering	1	7,300	Purchased pasta from Kazpi.kz
PSA4-5043+	3	5700	Purchased from Chip Dip.kz
GRM155R70J105M A12D, Multilayer Ceramic Capacitors MLCC - SMD/SMT 1 uF 6.3 VDC 20% 0402 X7R	20	216	Purchased from Chip Dip.kz
GRM31A5C3A101J W01D	171	3 078	Purchased from Chip Dip.kz
B82498-B3680-J, 68 нГн, 0805, 5%, Индуктивность SMD	12	2 856	Purchased from Chip Dip.kz
S-P225 SMA-female	3	2 933	Purchased from Ozone
Cargo Custom clearance services	1	50 000	Serviced in the customs office, Nursultan Nazarbayev Airport

Total	208 409.35
-------	------------

Table F-C. Meeting Summary.

No.	Date	Type	Participants	Key Topics	Decisions / Actions
M-01	Jan 13	Team	All four members	Project kickoff, role assignment, initial architecture discussion	Roles confirmed; component research started
M-02	Jan 20	Team	All four members	Architecture trade-off study; component shortlisting	Discrete IF-based design selected; BOM draft started
M-03	Jan 27	Team	All four members	Pre-deadline review; report draft review; schematic planning	Report sections assigned; submission plan confirmed
M-04	Jan 28	Supervisor	All + Dr. Nauryzbayev	Progress review before Jan 30 deadline; architecture approval	Discrete IF architecture approved (CL-01, CL-02)
M-05	Jan 29	Team	All four members	Final report edits; last checks before submission	Report finalized and submitted Jan 30
M-06	Feb 3	Team	All four members	Post-submission debrief; schematic design kickoff	TX schematic work begun; component ordering confirmed
M-07	Feb 10	Team	All four members	TX schematic review; component lead times update	Schematics reviewed; LCSC order placed
M-08	Feb 15	Team	All four members	Pre-deadline prep; PCB layout progress; antenna simulation status	Antenna completed early; PCB layout in progress
M-09	Feb 17	Supervisor	All + Dr. Nauryzbayev	Progress review before Feb 18 deadline; schematic approval	Schematics approved; single PCB decision made (CL-03)

M-1 0	Feb 18	Team	All four members	Final submission checks; Gerber file review	TX Gerbers submitted; deadline met
M-1 1	Feb 24	Team	All four members	PCB fabrication status; FPGA RTL planning	RTL development assigned; fabrication tracking started
M-1 2	Mar 3	Team	All four members	FPGA TX module progress; delivery timeline update	Delivery delay identified; parallel FPGA work started
M-1 3	Mar 10	Team	All four members	PCB delivery status; FPGA testbench results	CL-06 discussed — timeline extended 2 weeks
M-1 4	Mar 17	Team	All four members	Chip Dip delay flagged (new delivery Apr 15); USRP-2932 proposal	USRP-2932 option evaluated; escalation to supervisor planned
M-1 5	Mar 24	Team	All four members	USRP-2932 integration planning; GNU Radio setup	GNU Radio configured; USRP testing begun
M-1 6	Mar 31	Team	All four members	Loopback test result; BPSK verification	Fig. 1 and Fig. 2 results confirmed — basic link working
M-1 7	Apr 1	Daily	All four members	Over-the-air testing prep; antenna connection setup	Single-user 2.4 GHz link test planned
M-1 8	Apr 2	Daily	Idris, Aidana, Yerboldy	Single-user BPSK result (Fig. 3) confirmed	Moved to NOMA two-user transmission testing
M-1 9	Apr 3	Daily	Idris, Aidana, Yerboldy	NOMA two-user transmission results (Fig. 4–7)	Power-domain separation confirmed in IQ constellation
M-2 0	Apr 4	Supervisor	Idris, Aidana, Yerboldy	USRP-2932 change approval; over-the-air results review	CL-07 formally approved; SIC testing authorized

M-2 1	Apr 5	Daily	Idris, Aidana, Yerboldy	SIC implementation in GNU Radio	SIC algorithm implemented and tested
M-2 2	Apr 6	Daily	All four members	SIC result review (noma_far.png)	Full NOMA SIC result confirmed — Fig. 9 obtained
M-2 3	Apr 7	Daily	All four members	Result analysis; report writing	BER results analyzed; report sections drafted
M-2 4	Apr 8	Daily	All four members	Presentation planning; slide content	Presentation structure agreed
M-2 5	Apr 9	Supervis or	Aidana, Yerboldy, Amir, Dr. Nauryzbayev	Final results review; presentation feedback	Results approved; presentation structure confirmed
M-2 6	Apr 10	Supervis or	All, Dr. Nauryzbayev	Pre-presentation final check; report review	Final adjustments confirmed; demo rehearsed