Design of Germanium P-Type Point Contact Detector ASIC Preamplifier

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Abstract

This Master's thesis investigates the preamplifier designs for High Purity Germanium (HPGe) detectors and compares their performance characteristics. The topic is important in the fields of nuclear physics, materials science, and medical imaging, as HPGe detectors are widely used in these fields. Despite the availability of various preamplifier designs, there is still a gap in the research regarding the optimization of these designs.

The main focus of the work carried out is to analyze and study the existing designs of preamplifier circuits for HPGe detectors, compare their performance characteristics, and create a new design with improved parameters of noise, gain, and rise time. This new design is based on several special modifications, such as optimizing the input stage, refining the feedback loop, and enhancing the power supply rejection ratio. The study utilized simulation and analysis methods in Orcad software to evaluate and optimize the preamplifier circuits.

The key message of the thesis is the optimization of preamplifier designs for HPGe detectors, yielding significant improvements in performance characteristics. The final implemented preamplifier design demonstrated a rise time of 3.58 ns, voltage of 15.276 V, and noise of 1301 eV with a 50 pF detector capacitance. This improved design is compared to a widely-used existing design, referred to as the "previous design," which had a rise time of 6.68 ns, voltage of 13.42 V, and noise of 1441 eV. The complexity of the new design has been kept simple, low cost, and with low power consumption, making it a promising candidate for practical applications.

The research contributes to the field of preamplifier design for HPGe detectors by providing valuable insights into the optimization of preamplifier designs, demonstrating significant improvements in performance characteristics. The key optimizations include enhancing the input stage, refining the feedback loop, and improving the power supply rejection ratio. The Printed Circuit Board (PCB) design creation and feasibility analysis of chip fabrication further demonstrated the potential for applying the optimized preamplifier designs in practical applications. Overall, this research provides a promising solution for improving the performance of HPGe detectors, benefiting various fields such as nuclear physics, materials science, and medical imaging.

Acknowledgements

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List of Abbreviations & Symbols

ADC	Analog-to-Digital Conversion
ASIC	Application Specific Integrated Circuit
BJT	Bipolar-Junction Transistor
BOM	Bill of Material
CAD	Computer-Aided Design
CCSP	Capacitor Charge-Sensitive Preamplifier
CMOS	Complementary Metal–Oxide–Semiconductor
CSP	Charge-Sensitive Preamplifier
CTCSP	Continuous-Time Charge-Sensitive Preamplifier
DC	Direct Current
DRC	Design Rule Checks
DSP	Digital Signal Processor
EDA	Electronic Design Automation
FET	Field-Effect Transistor
FWHM	Full Width at Half Maximum
GERDA	The Germanium Detector Array
GDSII	Graphic Design System
HPGe	High Purity Germanium Detector
IDM	Integrated Device Manufacturer
IC	Integrated Circuit
JFET	Junction Field-Effect Transistor
LNGS	Laboratori Nazionali del Gran Sasso
LVS	Layout Versus Schematic
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMT	Photomultipliers
r.m.s	Root Mean Square
SiP	System-in-Package

SNR	Signal-to-Noise Ratio
T.A	Transimpedance Amplifier
TSMC	Taiwan Semiconductor Manufacturing Company
UMC	United Microelectronics Corporation
VSP	Voltage-Sensitive Preamplifier

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Chapter 1 – Introduction

In the modern world, High Purity Germanium Detectors (HPGe) are the most frequently utilized detectors in the wide range of applications from fundamental sciences to the industries . This technology is unique among analogs due to their performance characteristics, as high energy resolution, sensitivity and power efficiency. However, the given technology struggles with the output signal magnitude, as the radiation pulse has a very low amplitude and extremely sensitive to external noise sources. Therefore, the output signal requires further amplification and processing electronics to upgrade the Signal to Noise Ratio (SNR) to be read out and utilized in applications. The mentioned processing is held by specially designed preamplifier electronics, which has a role of amplification and shaping the signal amplitude.

The technology of preamplifiers plays a vital role in the domain of radiation detection technology. Radiation detectors rely on pulse-processing electronics to extract the initial signal within the radiation information [1]. However, the output signal from the sensor has a relatively small amplitude and high output impedance [1] – [3]. It may cause problems in the extraction process of the final signal to analyze the radiation interaction [2], [3]. Therefore, the preamplifier is designed to act as an interface between the detector and pulse-processing electronics [5].

The main functions of the preamplifiers are:

- Increasing the SNR by promptly terminating the capacitance of the detector output signal [4].

  To keep the initial rate of SNR, the preamplifier must be set as near as possible to the detector, as the signal-transferring cable should maintain short [1].
- Maintain the impedance rate between the components. The impedance rates should match to avoid the possible appearance signals, which can dramatically worse the signal quality [4], [5].

The amplitude of detector signals plays a crucial role in facilitating the operation of recording and analyzing devices. For instance, pulsed ionization chambers and semiconductor detectors produce signals in the range of hundreds of microvolts at maximum. Consequently, the detector signals need to be amplified by a factor of 2,7, or even by 10, depending on the type of detector and the energy of the detected radiation [1].

Typically, an amplifying device comprises two essential parts, namely, the preamplifier and the main amplifier. The preamplifier is located as close to the detector as possible to minimize parasitic capacitance and noise on the input circuits. The preamplifier is designed to require minimal adjustments for operational work. On the other hand, the main amplifier is generally positioned behind the radiation shield, often at a considerable distance from the preamplifier and detector. Different signal processing methods are employed by preamplifiers based on the type of detector and whether the measurement is amplitude energy or time [1].

Some of detectors such as scintillators have strong output signals which do not need any pre-amplifiers and only fast amplifier can be applied. Also since the amplitude of signal is high, it will have high SNR enough to have high energy or time resolutions. However, detectors such as silicon and germanium detectors and proportional counters used for X-ray and gamma-ray spectroscopy and charged particle spectroscopy have samller signal amplitudes, that is why to get better energy resolutions, we need to use low noise pre-amplifiers. [1], [7].

To achieve low noise preamplifiers for silicon and germanium-charged particle detectors and proportional counters, field-effect transistors (FETs) are commonly used in their input circuits. Although preamplifiers for these detectors usually operate at room temperature, for high-resolution gamma and X-ray spectroscopy, preamplifiers, FETs are also cooled to nitrogen temperature to minimize noise. They are placed inside the cryostat. HPGe detectors have very high output impedance and for impedance matchinhg, we need high input impedance

in preamplifiers, therefore FEts are proper options compared to Bipolar Junction Transistors (BJTs), resulting in less noise generation and higher immunity to radiation effects [1], [2], [6].

1.1 Aims and Objectives

The design of preamplifier for HPGe detectors mainly rely on maintaining the essential parameters of the output signal. The goal of every preamplifier, is to have signal with desirable shape and low noise characteristics. The crucial aspects of preamplifier output signal are: rise time, gain, SNR and decay time. Listed aspects should be controlled and have acceptable level for further processing. To meet acceptable balance of listed parameters corresponding design should be implemented. According to above mentioned points, the main aim of the thesis work is to design preamplifier circuit for HPGe detector with consistent parameters. Furthermore, the respective PCB design in CAD file of the implemented schematic will be in focus. The thesis research aims to verify the circuit's performance before implementing chip design, that is why the PCB design was firstly implemented.

The objective of the research work is to investigate exiting designs and based on these technologies try to optimize and modernize them from the points of gain, SNR, rise time etc.

1.2 Methodology

The present Master's thesis aims to investigate the optimization of preamplifier designs for HPGe detectors through simulation studies. The study investigates previous preamplifier designs, each with its unique parameters, to identify potential areas for modification and optimization, focusing on SNR optimization [1]. The performance of the optimized designs has been compared with that of the current preamplifiers to determine their general effectiveness.

The thesis also addresses the design and creation of the PCB for fabrication purposes, using CAD software. The feasibility study of the designed chip has been conducted to determine the potential for successful fabrication.

To simulate the performance of the preamplifier designs, the Orcad CAPTURE CIS software from Cadence has been selected. This software is widely used in professional applications and industries for analyzing electronic circuits performance and designing PCB's. Orcad CAPTURE CIS stands out due to its extensive library of electric components, which makes it a preferred choice for simulating and analyzing the performance of various electronic devices and circuits.

Additionally, the study includes a comparison of various preamplifier designs to determine the most effective approach. Several factors have been considered, including noise reduction techniques, sensitivity, linearity, and dynamic range. By comparing various designs, the study aims to provide insights into the most effective strategies for optimizing preamplifier performance for HPGe detectors.

In conclusion, this thesis project aims to explore the optimization of preamplifier designs for HPGe detectors through simulation studies, PCB design creation, and feasibility of chip fabrication analysis. The Orcad CAPTURE CIS software has been used for simulating and analyzing various preamplifier designs to determine their effectiveness in enhancing the performance of HPGe detectors.

1.3 Problem Statement

The modern signal processing and amplifying technologies allows us to operate tiny amplitude signals described in mile and micro volts [8] - [10]. The preamplifiers can amplify the signal with a gain rate of 40 dB and with noise level of 5 $\frac{nV}{\sqrt{Hz}}$. In [1] the preamplifier circuit is designed with parameters of gain in preamplifier being $\approx 3{,}5$, noise characteristics being 2

$\frac{nV}{\sqrt{Hz}}$, minimal power consumption comprising 50 mW and with a feedback resistance accounting to 10 GΩ [1]. However, the design still needs to be improved as the noise parameters are still not desirable. Hence, the design requires to be optimized from the point of SNR and final amplification. Furthermore, the contemporary solution for the modification of preamplifier technology in minimizing the size and construction as creating a chip design is necessary. The improvement of the SNR even by minimal value can advance the radiation detection industry by many factors [8] - [10]. Furthermore, the possible chip design solves the issue of the modernization, power consumption and overall provides global financial, technological benefits for manufacturers and consumers. However, chip design is a complex and expensive process, which critically requires PCB design verification before implementing any chip design. To achieve this, mathematical calculation of the parameters, simulation of the components and final comparison of the modified result with initial circuit will optimize the current preamplifier design.

1.4 Background Information

The most famous experiment held with germanium detector is the GERDA experiment (Germanium Detector Array) launched at the Laboratori Nazionali del Gran Sasso (LNGS) [1]. The experiment is searching for neutrinoless double beta decay (0vββ), by using high purity enriched 76Ge crystal diodes as a beta decay source and particle detectors. The principle of the work relies on HPGe detectors being launched in 64m^3 cryostat, fulfilled by liquid argon, which has a temperature of –186°C. The screening is supplied by additional level of 3m water, equipped by photo multiplier technology for detecting Cherenkov light. Furthermore, apart from listed screening, the laboratory is located underground, protecting it from cosmic radiations [1].

1.4.1 Charge Sensitive Amplifiers

Fig. 1.1 indicates the basic concept of charge amplifier operation with an integrated process using parallel RC circuit. The process relies on the detector transiting short current pulses to the amplifier. The feedback resistor in this scheme provides current integration into voltage pulses by amplifying and discharging them [1], [2], [6]. Thus, producing an exponential decay of the signal with some time constant [1]. This means that the signal weakens over time, and the time between each pulse stays the same because of the feedback resistor. The feedback resistor is shown in Figure 1.1 and can be adjusted by using a switch that can be configured rapidly after each pulse. The schematic indicated below uses a feedback resistor for this purpose. The initial stage of the system is the most vital part of the overall system, as it defines the general noise parameters of the signal, and that is why it should be installed at the minimum distance from the detector input [1] - [3], [5].

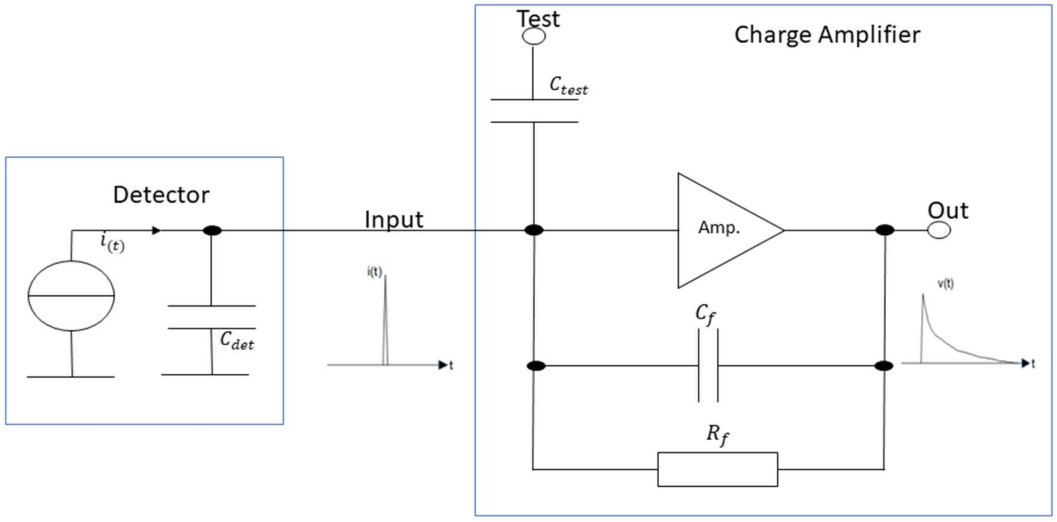

Figure 1.1 : Charge amplifier basic circuit [1]

To provide the most optimal results of such a system, the input capacitance of the scheme $C_{GS} + C_{GD}$, provided by the input FET in common-source configuration, should not

overcome the detector capacitance level. Here, C_{GS} – stands for capacitance between the gate and source terminals of the FET, while C_{GD} - stands for capacitance between the gate and drain terminals. When a FET is utilized as an input for an amplifier in a common-source configuration, the total input capacitance to the amplifier (Amp.) would be the sum of these two capacitances. The C_{test} capacitor is provided in the circuit for calibration and test purposes as a representative for detector. A step signal is provided on the test input of the circuit, giving current steps. The charge indicator can be calculated as [1]:

$$q = C_{test}V_{test}, \tag{1.1}$$

where q is charge generated by test signal, C_{test} is the capacitance of test signal and V_{test} is the voltage rate of test signal.

$$V_{out} = \frac{q}{C_f}, \tag{1.2}$$

where V_{out} is output voltage rate and C_f is feedback capacitance rate.

The amplification rate is calculated as:

$$A = \frac{V_{out}}{V_{test}} = \frac{C_{test}}{C_f}, \tag{1.3}$$

where A is amplification rate.

The C_{test} capacitance is quite sensitive to stray capacitances. Stray capacitance is the unintended capacitance that occurs in electrical circuits and components due to the natural presence of conductive materials and insulators [1]. Therefore, the number should be concrete to provide a compatible charge rate, which will also be calculated in the following chapters. The amplificated rate is described in the Eq. 1.3 and to keep the amplification rate, the indicator of the capacitance of the feedback capacitor should be kept lower than the test capacitor indicator $C_f < C_{test}$ [1].

1.5 Related Works

The literature review has been carried out in the relevant area of the research topic, strictly concentrating on the research related to the preamplifier for HPGe detectors.

Mainly, there are 2 types of preamplifiers in the industry of radiation detection technology. Those are: charge sensitive and voltage sensitive preamplifiers. The main difference of them, is that Charge-Sensitive Preamplifier (CSP) have current pulse as the input from the detector and converts that energy into voltage signal, while Voltage-Sensitive Preamplifier (VSP) directly amplify the voltage signal from the detector.

CSP's are the most commonly used in HPGe detectors, as they equipped by relatively high input impedance. This feature, enables CSP to minimize the loss of the energy by the presence of the capacitors on the input stages of the circuit. Nevertheless, there are many designs and technologies of implementing preamplifier circuits in the field of HPGe detectors.

In the sense of CSP's Junction Field-Effect Transistor (JFET) preamplifiers are the most widely utilized concepts, which provides high input impedance, low noise and overall stability of the signal. These circuits typically managed with JFET transistors and feedback line, which enables the gain factor of the amplifier. These preamplifiers differ with dramatically low noise characteristics, comprising around less than 1 electron equivalent noise.

A meticulously crafted and executed design for a low-noise charge amplifier circuit tailored for the LEGEND-200 cooperation has been investigated in [1]. This circuitry aims to detect rare interactions between dark matter particles and atomic nuclei, requiring a robust and accurate amplification system [1].

The basic concept of preamplifier design can be observed in the Fig. 1.2. The amplifier circuit comprises two distinct components: a preamplifier and a post amplifier, with additional feedback and coupling capacitor integration. The preamplifiers sole purpose is to convert the minute charge signal generated by a radiation detector into a voltage signal of considerable

impedance, which then gets amplified further by the post amplifier. The preamplifier is comprised of a high-input-impedance field-effect transistor (FET) and a feedback capacitor. The FET functions as a voltage-controlled resistor, varying its resistance in response to the input charge signal. The feedback capacitor provides a DC bias to the FET and stabilizes the amplifier gain.

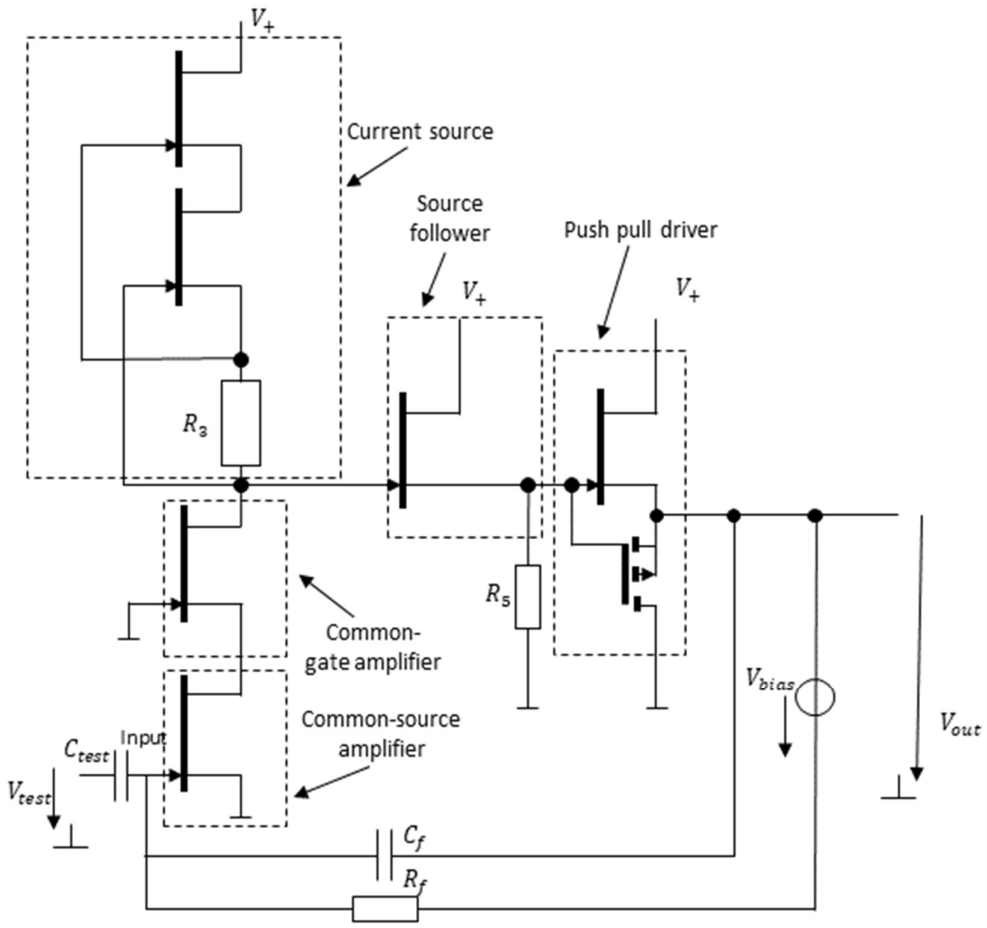

Figure 1.2: Preamplifier circuit [1]

The basic concept of post amplifier design can be observed in the Fig. 1.3. The post amplifier is designed to provide further amplification to the signal received from the

preamplifier. It incorporates a low-input-impedance operational amplifier and a feedback network of resistors and capacitors. The operational amplifier effectively amplifies the voltage signal from the preamplifier and provides a low-impedance output, which can drive the load without significant signal loss. The feedback network is tailored to stabilize the amplifier gain, reduce noise, and ensure that the amplifier output accurately reflects the input signal [1].

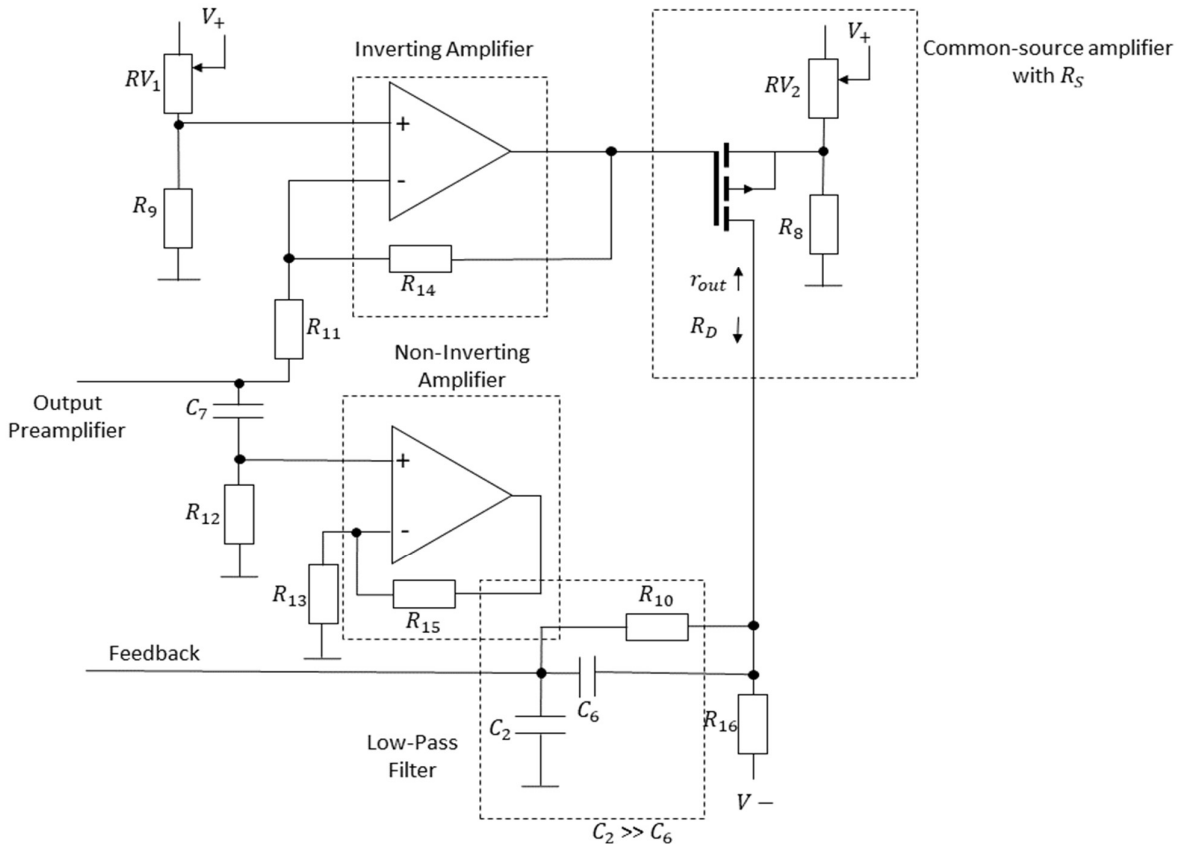

Figure 1.3: Post amplifier circuit structure [1]

The amplifier circuit underwent rigorous characterization and testing utilizing various input signals. The test results showcase the circuits excellent performance, amplifying the input charge signal with a gain of up to 2.5. According to [1] test results, the circuit presented in the Fig. 1.2 and 1.3 achieved a noise level of approximately 0.8 keV Full Width at Half Maximum (FWHM) at room temperature, highlighting the amplifiers incredible noise performance. This aspect is particularly important as it directly affects the experiments detection sensitivity [1].

An exhaustive examination of the circuit's general construction, aimed at low-noise charge amplification endeavors such as identifying rare interactions between atomic nuclei and dark matter particles in [1]. Additionally, the thesis delves into essential factors to consider when designing the amplifier, including how input noise affects performance, selecting fitting components for the feedback network, and weighing the trade-offs between gain and noise performance.

The overall circuit design is presented in the Fig. 1.4. The design and performance of a low-noise charge amplifier that incorporates a fast rise time and active discharge mechanism has been investigated in [2]. In simpler terms, an active discharge mechanism in electronic circuits helps to quickly release the stored energy in capacitive loads, like capacitors or circuits with unintended capacitance. This quick release is crucial in situations where rapid changes between charged and discharged states are needed, such as in fast digital circuits, power supplies that switch modes, or any other applications where timing is critical [2]. The authors aim to improve the SNR in HPGe detectors used in gamma-ray spectroscopy by minimizing noise and maximizing signal amplification [2].

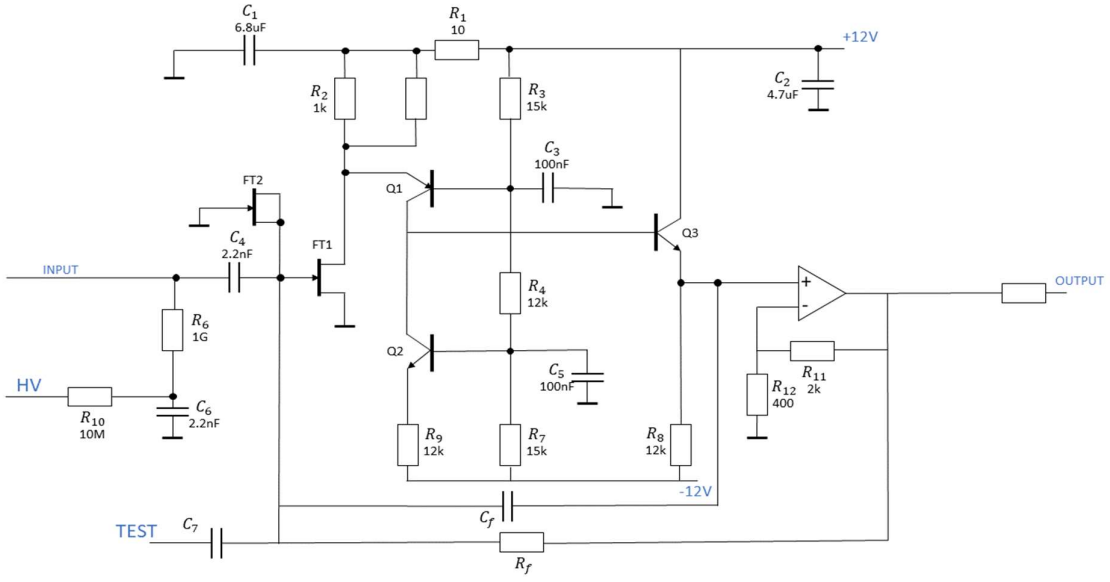

Figure 1.4: Preamplifier circuit with active discharge mechanism

The charge preamplifier design uses a feedback capacitor to convert the detector's charge into a voltage signal, which is then amplified by a low-noise amplifier [2]. The circuit uses low impedance line described by feedback resistor, which aims to quickly discharge feedback capacitor. The fast rise time of the amplifier is achieved through careful component selection, while the active discharge mechanism is implemented to mitigate noise and improve the amplifier's stability [2].

The presented experimental results demonstrate the performance of the amplifier, showing that it achieves a low noise level and a fast rise time, leading to an improvement in the energy resolution of the HPGe detector. The amplifier's active discharge mechanism is also shown to reduce the recovery time of the amplifier, which is an essential factor in high-count rate applications [2]. Overall, has been presented valuable insights into the design and performance of preamplifier circuits for HPGe detectors, demonstrating the importance of low noise, high gain, and fast rise time in achieving optimal performance [2]. The authors' active discharge mechanism is an innovative approach that can be applied to other preamplifier circuits to enhance their performance in gamma-ray spectroscopy applications [2].

A simple preamplifier schematic was designed by integrating Application Specific Integrated Circuit (ASIC) is presented in [3]. The created circuit can provide 2.4 V pulse with 100 Ω load approximately in 13 ns time without any considerable fluctuation. The authors design performance capable to for ensuring optimal performance and signal transmission over 100 Ω load, which is a standard value often used in designing electronic circuits, particularly for transmission lines and signal processing applications. By using a known and standardized load value, the authors could design the preamplifier circuit to achieve specific performance targets, such as minimizing signal distortion, noise, and power consumption, while maintaining compatibility with other components and systems [3]. Moreover, the output signal results illustrated 110 r.m.s electrons with 16 pF detector capacitance in various environment

temperatures [3]. Noise value is described in r.m.s in [3], which stands for root mean square. In noise r.m.s is described as the process, providing mean of the power output over period of time [3].

For the input stage of the scheme BF862 FET in a common-source configuration is used, as shown in Fig. 1.5 [3].

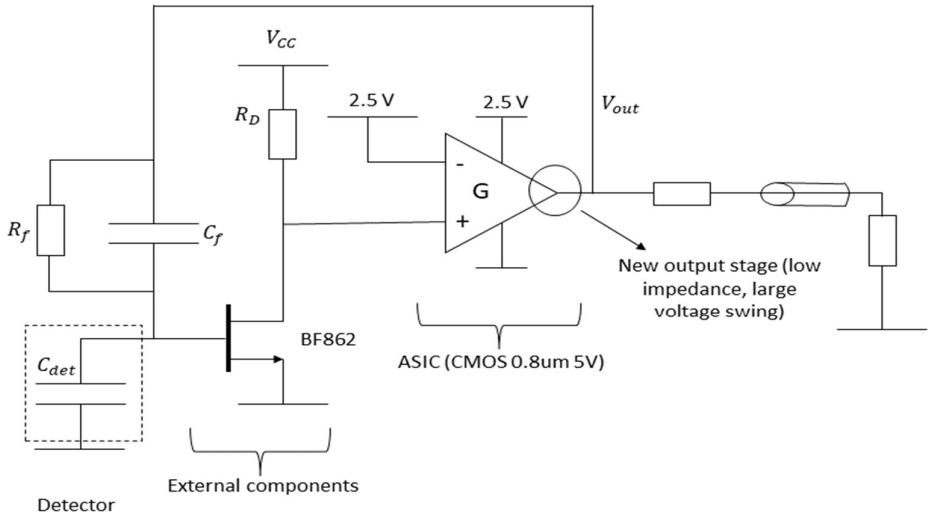

Figure 1.5: Preamplifier circuit structure [3]

The input signal at the first stage goes through common-source JFET, providing high impedance rate of the signal [3]. The main element ASIC, consists of cascaded common-source p-type Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), parallel connected to another MOSFET with Miller capacitor, used for signal stabilization [3]. The overall loop gain is described as the multiplication of the listed gains and computed as:

$$A_0 = g_m R_D G_0, \tag{1.4}$$

where, g_m is the transconductance of the JFET, R_D is the drain resistor, $G_0 = \Delta V_0/\Delta(V_+ - V_-)$ is the low-frequency gain of the integrated amplifier [3].

The internal structure of the gain utility is depicted in the Fig. 1.6.

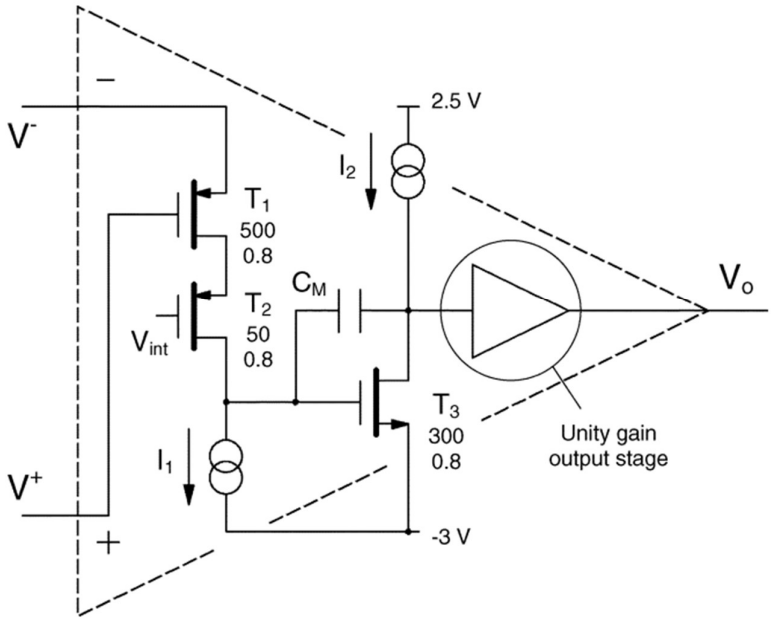

Figure 1.6: Gain path of the preamplifier [3]

The analogous charge-sensitive preamplifier of for HPGe implemented and result reported in [5]. The schematic indicated optimal results in noise degradation of 101 r.m.s electrons with rise time of 8.3 ns. The main goal of the work was to optimize the Advanced Gamma Tracking Array (AGATA) detector, in particular modernization techniques for Transimpedance Amplifier (T.A) technology [5].

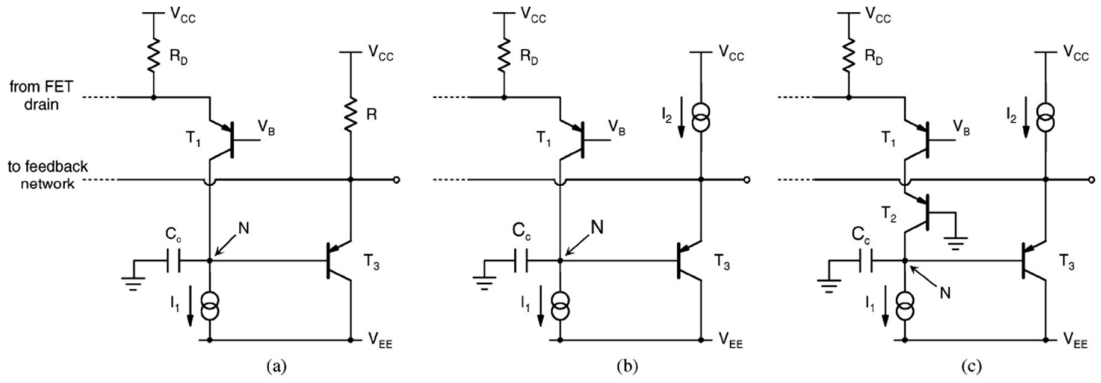

Figure 1.7: Simplified variations of TA [5]. (a) base version of T.A, (b) version of T.A with integrated current source, (c) version of T.A with integrated current source and cascaded FET

Fig. 1.7 illustrates different variations of simplified schematic of Transimpedance Amplifier (T.A). The use of folded-cascade schematic has considerable drawback for the parameter of the loop gain in the face of Miller effect generated in the input stage of FET. The problem was solved by the use of second BJT transistor. The follow up of the circuit was upgraded by the increase of the overall load resistance, which results in the improvement of loop gain figure at low frequencies. The main disadvantage of the modernized circuit could be increase of noise parameter, however experimental results indicated the proper biasing of the circuit can solve this issue [5].

The simplified circuit diagram for [6] is illustrated in Fig. 1.8. Another CSP suitable for silicon and germanium detector is reported in [6]. The schematic design for [6] provides wide bandwidth with 10 ns rise time. The input stage equipped by low-noise JFET ensures minimal values of noise. The input stage has a cascade structure, which is current generator [5], [6]. The current generator consists of 3 components and can supply with a current I, 3I and 5I. On the next step, the signal forwarded to JFET in common-source gain position, equipped by Miller capacitor, which can be adjusted between 2 pF and 5 pF [6].

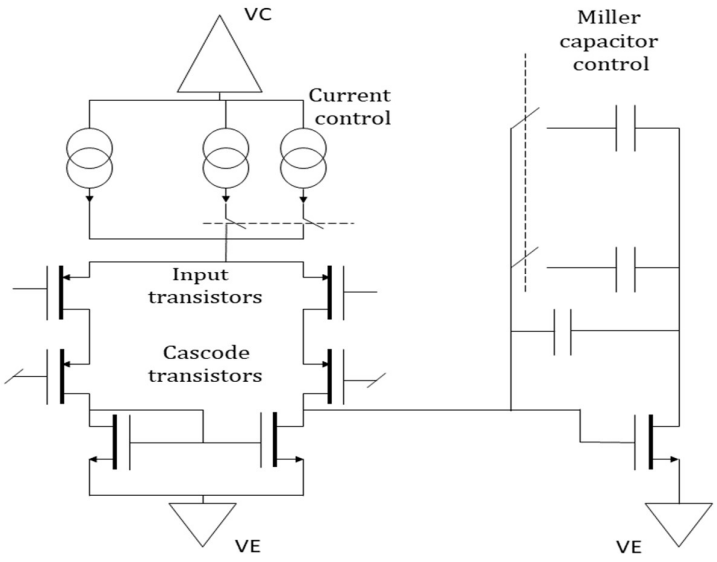

Figure 1.8: Simplified schematic of the input stage [6]

A JFET-CMOS preamplifier for HPGe detectors has been developed and reported in [7]. Built in a 5 V 0.35 μm mid-oxide and computer simulated Complementary Metal-Oxide-Semiconductor (CMOS) engineering. Computer simulated CMOS engineering refers to the process of using computer software to design, analyze, and optimize CMOS circuits and devices. The circuit has a rapid reset device, for the charge detecting stage de-saturation. The method enables the reduction of decay time in the presence of a dangerous high-radioactivity background. Additionally, it enables charge information recovery even when the preamplifier is deeply saturated. The reset time and input charge are proportional to each other, which enables dramatic increase of the energy measurement range by an order of magnitude [7].

A multi-channel CSP named CC_2 in the GERDA experiment base with HPGe detectors at cryogenic conditions has been investigated in [8]. The proposed system consists of 2 fundamental elements. First one is n-type JFET BF862 acting as the input FET and consequently connected CMOS operational amplifier [8]. BF862 is one of the best choices in the market for front-end device, as it has relatively high input impedance and amplification rate [8]. AD8651 has been selected for the operational amplifier as the most suitable one. Moreover,

the proposed electronics have been tested at 2 different laboratories with germanium detectors. Firstly, in Milano, with Germanium encapsulated detector (SUB) and at LNGS with encapsulated Germanium detectors at both capacitance configurations, low and medium [8].

A new design for preamplifiers to be used in gamma-ray spectroscopy applications with high-capacitance detectors has been reported in [14]. The proposed novel design involves creating a preamplifier with an extensive dynamic range and rapid response time, capable of handling signals with high capacitance and fast rise times [14]. The preamplifier's input stage features an innovative configuration that permits high gain and low noise performance. The shaping circuit ensures rapid response time while preserving linearity. The effectiveness of the design has been demonstrated by measuring energy resolution and timing resolution with a high-capacitance HPGe detector. The results show a significant improvement in energy and timing resolution compared to previous designs, making this new technology highly promising for future gamma-ray spectroscopy applications [14].

Another JFET preamplifier for HPGe detector is reported in [4], which is based on keeping the information unit from the detector, which is charge pulse in the case, on the another capacitor in combination with input JFET capacitance, connected to the input of the preamplifier. The schematic also equipped by fast reset device to perform quick de-saturation of the signal. The project introduced in [9] also demonstrates the schematic for CSP with fast reset system. However, the circuit is integrated to use with solid-state detectors, which have different parameters in comparison with HPGe. Another project integrated with fast-reset circuit was introduced in the research [10]. Fast low-noise hybrid preamplifier with logic and/or system was integrated to perform Analog to Digital (ADC) saturation of the signal to decrease the dead time. The schematic presented 7.5 ns rise time with 23 pF detector capacitance [10].

One of the main properties of every preamplifier is the ability to operate at cryogenic temperatures, which is referred to be in the range of -150℃ to -273℃ [10], [11]. Therefore, most projects configured to have components with credibility to perform at cryogenic conditions. Another work with double stage n-MOSFET for obtaining negative voltage swing was intended to function at cryogenic environment is reported in [11]. Preamplifier performance was tested at 77k and as the result the value for rise time amounted to 13ns [11]. An integrated schematic for Ultra-Fast Charge-Sensitive Micro-Probe for semiconductor detectors has been introduced in [12]. Special design with suitable capabilities which obtained approximately 5.3 ns rise time and 5 V output amplitude result with 16- pF detector capacitance has been developed in [12]. The design also has advanced an Application-Specific Integrated Circuit (ASIC) version, which maintained rise time less than 1 ns. Featured design is similar to another circuit presented in the [13]. A special structure for non-linear pole-zero compensation, which enables the technology of filtering/removing of indirect behavior of the charge reset technology has been reported in [13]. The second novelty of the design consists of fast-reset structure providing the dramatic reduction of dead time.

1.5.1 Summary

Overall, the summary of all illustrated articles present charge-sensitive preamplifier designs for germanium and other semiconductor detectors. The aim of all designs is to provide amplification and low-noise rate of the signal. The common factor of all discussed preamplifiers is FET's, especially input FET's configured in the common-source parameter to provide high impedance rate, as the signal coming from the detector also has high impedance. The review of most circuits for preamplifier, clearly depicts that BF862 JFET is the most desirable option for getting low-noise and high gain output signal [1]. Another noticeable common factor is the presence of gain utility, which is designed with various designs at each article. For instance, in

the work reported in [1] gain utility was presented in the post amplifier circuit by 2 operational amplifiers. A common-source MOSFET's for amplification purposes was used in [2]. Moreover, all indicated designs provided Miller capacitor to eliminate the Miller effect, as the all circuits implement amplification of the signal parameters. To conclude, the overall analysis has depicted that the use of JFET preamplifiers in combination with BJT's manages stable results, in terms of output signal performance. Moreover, the utilization of JFET technologies satisfy the main factors of any HPGe signal output. Given technology has an equal balance in comprising signal requirements. The method, provides fast rise time, high gain and low noise of the output signal, which are the most desirable option for further signal processing electronics setup. Furthermore, another common and crucial factor of most presented designs is the schematic durability to operate at cryogenic conditions, which is reached by selecting components able to operate 77 k temperatures [1].

It is a fact, that there is a competitive race between designers of CSP's and each design has its unique parameters. The concept of these CSP designs has been taken into account as the fundamental for the further creation of the new CSP circuit.

1.6 Thesis Structure

The thesis is organized in following way:

The introduction chapter introduces with the term of preamplifier technology for HPGe detectors, by providing background information and Literature Review on the topic.

Chapter 2 focuses on different preamplifier designs integrated for HPGe detectors, compare the characteristics and outline key parameters and design highlights.

Chapter 3 introduces, with design of the preamplifier with corresponding graphs and calculations.

Chapter 4 contains information regarding chip and PCB design and demonstrates PCB design in CAD file. Moreover, chapter depicts information regarding feasibility of chip production and list possible barriers and opportunities.

Chapter 2 – Preamplifier Designs Analysis

The history of the charge sensitive amplifier for HPGe detectors dates back to the 1960s when the first HPGe detectors were created. The early amplifiers utilized distinct components such as vacuum tubes and distinct transistors and were relatively extensive and intricate.

In the 1970s, integrated circuit (IC) technology advanced rapidly, leading to the development of the first hybrid charge sensitive amplifiers. These amplifiers used separate components for input and output stages and an integrated circuit for signal amplification and shaping. The hybrid amplifiers were smaller, more dependable, and had lower power consumption than their distinct counterparts [16] – [32].

During the late 1970s and early 1980s, engineers made a big leap in charge sensitive amplifier design with the introduction of the monolithic charge sensitive amplifier. These amplifiers were a game-changer as all the essential components were combined into one single chip. This innovation brought significant benefits to the table, including a reduction in size, cost, and power consumption of the amplifier. At the same time, the signal quality remained top-notch [16] - [23].

With the development of technology, several distinct designs of monolithic amplifiers emerged, each with their unique advantages and disadvantages. Some of these included MOSFET-based amplifiers, JFET-based amplifiers, and CMOS-based amplifiers. Depending on the particular application requirements, each of these designs could be the perfect fit.

In recent years, there has been a growing trend in using low-power, high-speed CMOS technology to design charge sensitive amplifiers. This trend has led to the development of several new amplifier designs, such as the switched capacitor charge sensitive preamplifier and the continuous-time charge sensitive preamplifier. These are 2 main types of CSP's used in the domain of radiation detection technology. Capacitor Charge-Sensitive Preamplifiers (CCSP)

accumulate and store input charge on a capacitor for discrete event processing, while Continuous-Time charge-sensitive preamplifiers (CTCSP) use a feedback resistor and capacitor to continuously process input charge signals. The key difference lies in their operating modes: CCSPs are suitable for discrete events with time to discharge, whereas CTCSPs handle continuous charge signals without requiring a separate discharge step.

2.1 Low-Noise Charge Amplifier for the LEGEND-200 Cooperation analysis

This chapter will introduce and illustrate analysis of different optimal CSP preamplifier designs by simulating the results and overall comparison of the performances.

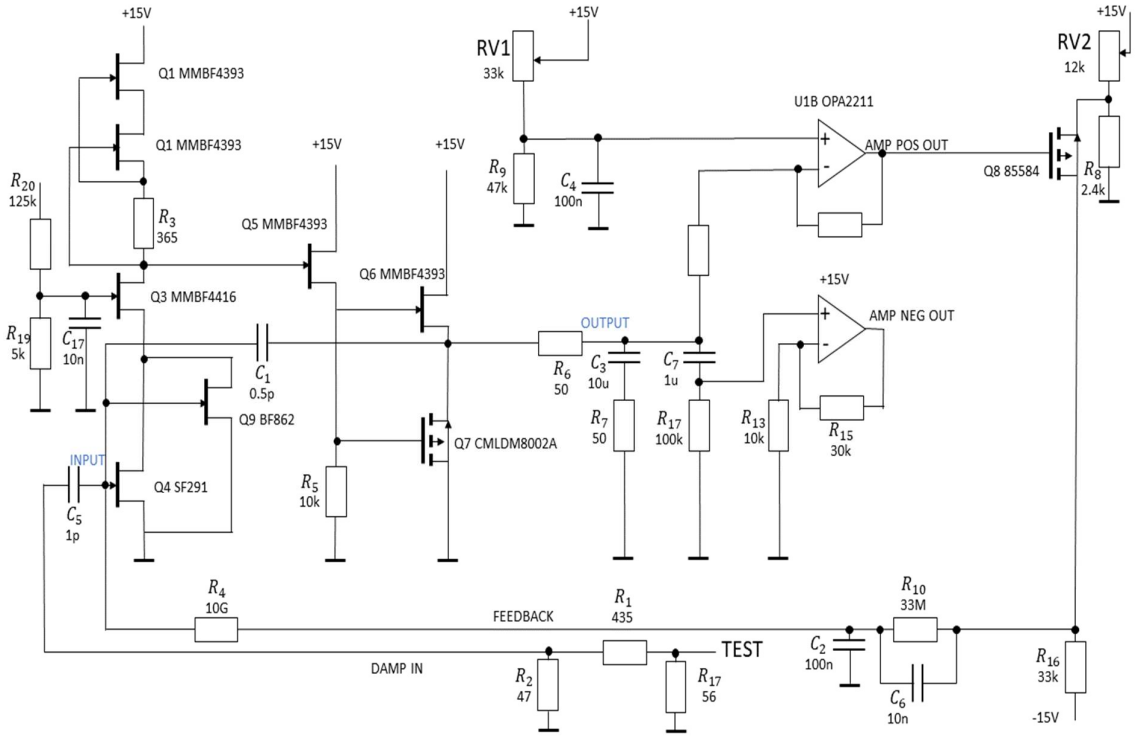

Figure 2.1: Full preamplifier schematic LEGEND 200 [1]

The overall circuit structure of the collided preamplifier and post amplifier block can be observed in the Fig. 2.1. The charge input is applied to Q4 and Q9, configured as common-source JFET's, which provides high input impedance and relative high gain. The

transconductance rate of the input FET can be calculated as presented in the Eq. 2.1 The gain factor of the FET is calculated by the Eq. 2.2. The r_0 is the resistance rate between the drain and source, which is applied for the configuration of Channel Length modulation and described as in the Eq. 2.3 [1].

$$g_m = \frac{i_{out}}{v_{in}} = 2\sqrt{\frac{I_{DSS}}{V_{th}^2} I_{D0}}, \tag{2.1}$$

where, I_{DSS} is the rate of maximum flowing current through FET, V_{th}^2 is the threshold voltage, applied to the gate of FET and I_{D0} is the constant, representing the bulk effect of the JFET [1], [2], [7], [15].

$$A_S = -g_m \, R_D \big|\big| R_L \big|\big| r_0 = \frac{v_{out}}{v_{in}}, \tag{2.2}$$

where, R_D is the drain resistor and R_L is the load resistor.

$$r_0 = \frac{1}{\lambda I_{D0}}, \tag{2.3}$$

where, λ is a component constant, which has values ranging from $1m\frac{1}{V}$ to $100\,m\frac{1}{V}$ [1].

On the second stage the signal is applied to the Q3, in the common-gate configuration, which provides elimination of input capacitance rate of input signal. The voltage amplification rate of Q3 is the same as Q4 and Q9, but just non-inverting. The third stage is the cascaded 2 JFET's Q1 and Q2 in the common-source configuration, ensuring current source. The resulting amplified and shaped signal travels through source-follower Q5, which has relatively high input impedance and maintains 0 amplification of the signal. Finally, the output passed to the post amplifier subsystem with the help of push pull driver, implemented by 2 JFETs Q6 and Q7 complimenting each other [1]. The basic concept of preamplifier block operation can be observed in the Fig. 2.2.

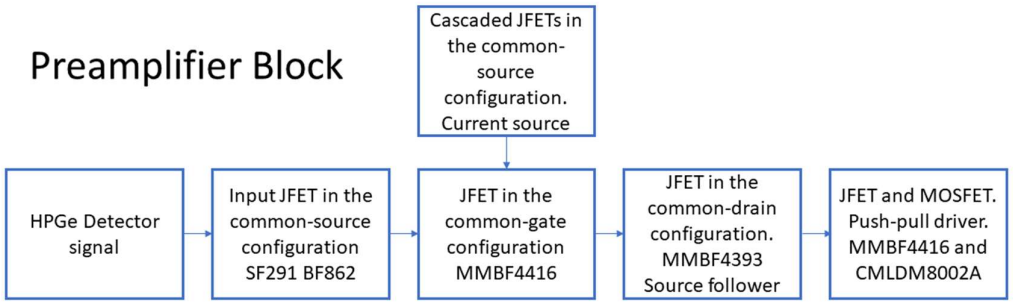

Figure 2.2: Preamplifier block diagram [1]

The fundamental of the post-amplifier is established on two operational amplifiers (Fig. 8). One is inverting and does direct current biasing and amplification. At the same time, the other one acts as non-inverting and only amplifies the signal. The schematic also includes a low-pass filter for compensating signal amplitude increase and filtering the feedback [1]. The low-pass filter is integrated with the capacitor C2 and resistor R10. The circuit simulation showed that the capacitor C2 creates a signal's phase shift. Therefore, to level out the change, the capacitor C6 was added. However, to still maintain the functionality of the low-pass filter, the capacitance rate of the C6 must be much lower than C2 [1].

The basic principle of post amplifier block operation can be observed in the Fig. 2.3.

Table 2.1: LEGEND 200 schematic components list

Component Type	Model	Configuration	Quantity
N-channel JFET	SF291	Common Source	1
N-channel JFET	BF862	Common Source	1
N-channel JFET	MMBF4416	Common-Gate	2
N-channel JFET	MMBF4393	Common-Source/Common-Drain	3 1
Dual P-channel MOSFET	CMLDM8002A	N/A	1
P-channel MOSFET	BSS84	Common-Source	1
Operational Amplifier	OPA2211	Inverting Amplifier	1
Operational Amplifier	OPA2211	Non-Inverting Amplifier	1
DC Voltage Source	N/A	15V	11

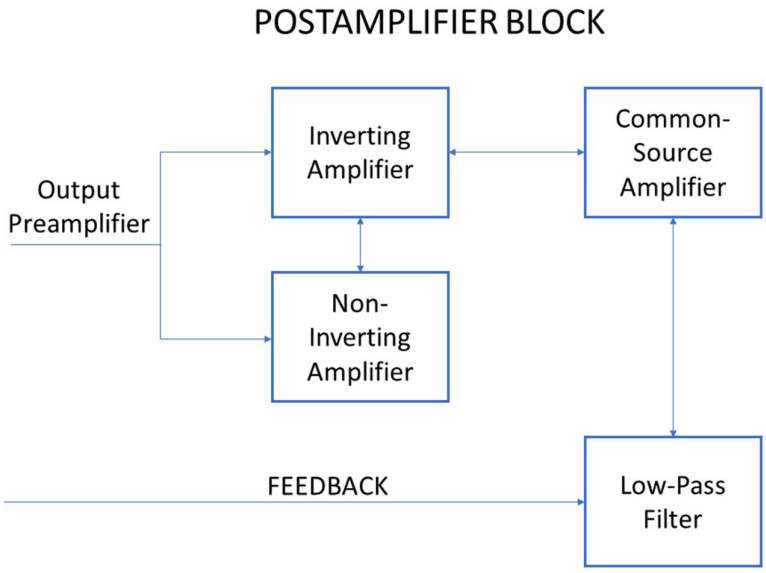

Figure 2.3: Post Amplifier block diagram [1]

2.2 Wide-Dynamic-Range Fast Preamplifier analysis

Another low-noise ultra-fast preamplifier design was implemented in the [14]. The input charge is applied to the input 4 parallelly connected JFET's (J1, J2, J3, J4). The reason to

implement 4 FET's in parallel relies on maintaining high transconductance g_m rate. The high magnitude of transconductance enables to keep low the rising-edge time constant τ_r, which is one of the most important parameters slowing the operation speed of CSP. The rising edge time is calculated as:

$$\tau_r = C_T(\frac{C}{C_F g_m}), \tag{2.4}$$

where, C_T is the sum of input, detector, feedback and stray capacitances, C is the amplification node capacitance, C_F feedback capacitance and g_m is the transconductance rate.

The overall circuit diagram is presented in the Fig. 2.4 and components list is indicated in the Table 2.2. The design is also equipped by 3 BJT's, which has a basic role of voltage amplification, due to the lack of power supply. Operational Amplifier is used to amplify the resulting signal to the sufficient rate. The feedback network of the design is presented by parallel connection of the feedback capacitor and resistor. The capacitor acts as a high-pass filter that removes low-frequency noise from the input signal, while the resistor provides a feedback path for stabilizing the amplifier gain.

Table 2.2: Preamplifier schematic components list

Component Type	Model	Configuration	Quantity
N-channel JFET	BF862	Common Source	4
BJT	BFT92	N/A	2
BJT	BFR92	N/A	1
N-channel JFET	SST201	N/A	1
P-channel MOSFET	BSS84	Common-Source	1
Operational Amplifier	LM6171	Non-Inverting Amplifier	1
DC Voltage Source	N/A	500V, 6V, -12V	3

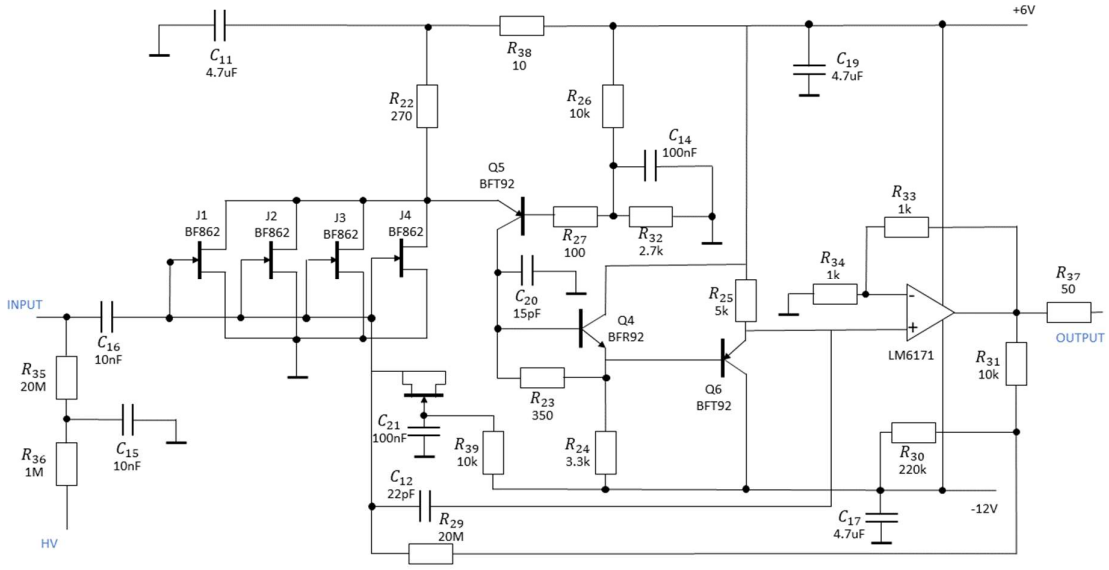

Figure 2.4: Preamplifier circuit(CHIMERA) [14]

The output of the CHIMERA circuit is indicated on the Fig 2.5. The performance of the circuit was tested with 50 pF detector capacitance. The rise time of the final signal is 14.68ns, while the resulting voltage amplitude comprises 430.27 mV.

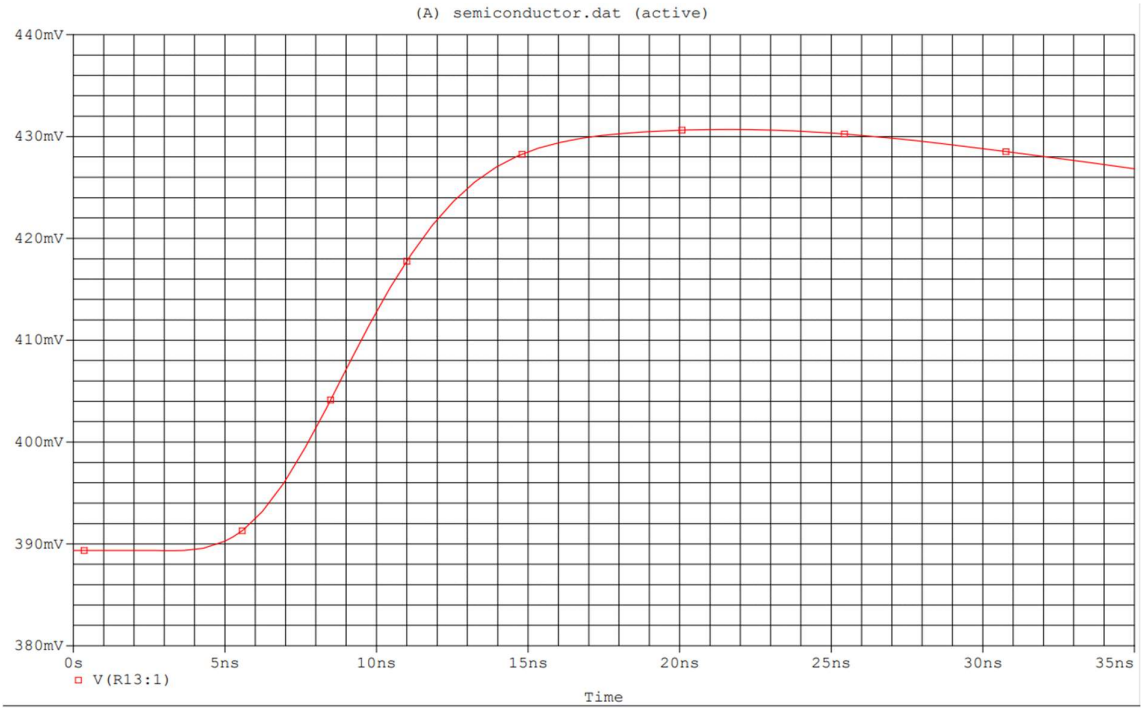

Figure 2.2.1: Output signal of the preamplifier (CHIMERA)

2.3 Comparison of Circuits

In this section we delve into a comparative analysis of two research works that focus on preamplifiers designed for pulse shape analysis of signals from high-capacitance detectors. The objective is to understand the unique features and performance characteristics of each circuit, which will help in choosing the appropriate circuit based on the specific requirements of an application.

2.3.1 Wide-Dynamic-Range Fast Preamplifier

A Wide-Dynamic-Range Fast Preamplifier circuit has a characteristics which excel in linearity, gain stability, and noise characteristics. With its wide dynamic range and quick response times, this circuit presented in the Fig. 2.2.1 is suitable for a variety of applications, including nuclear spectroscopy and particle identification [14].

- The primary attributes and performance aspects of this circuit include:
- Expansive dynamic range: With support for up to 100 MeV for silicon detectors, this circuit can be employed in a diverse array of applications.
- Quick response time: The circuit's rise time of 5 ns highlights its speed and effectiveness.
- Minimal noise interference: The circuit has been thoughtfully designed to reduce noise disturbances, ensuring more accurate signal processing.
- Outstanding linearity and gain stability: This circuit exhibits remarkable linearity and gain stability, leading to accurate and reliable results.
- Adaptable usage: The preamplifier is versatile, as it can be utilized with various detector types such as silicon, germanium, and scintillation detectors.

2.3.2 Low-Noise Charge Amplifier for the LEGEND-200 Cooperation

The research work presented at [1], introduces a preamplifier circuit for high-capacitance detectors, concentrating on optimizing energy resolution and pulse shape discrimination. To achieve enhanced energy resolution without affecting response time, the circuit integrates a creative feedback scheme. Moreover, it showcases solid noise performance and compatibility with a variety of detector types.

The main features and performance aspects of this circuit are:

- Improved energy resolution: The inventive feedback scheme enables better energy resolution, which is crucial in numerous applications.
- Fast response time: This circuit is engineered for quick signal processing while maintaining accuracy.
- Cutting-edge feedback scheme: The distinctive feedback mechanism plays a significant role in the circuit's overall performance and energy resolution.
- Effective noise reduction: Similar to the first circuit, this design minimizes noise interference, allowing for more accurate signal analysis.
- Wide-ranging compatibility: The circuit can work with different detector types, making it an ideal choice for a variety of applications.

Both circuits are designed to address the challenges associated with high-capacitance detectors and pulse shape analysis. A wide-dynamic-range fast preamplifier excels in dynamic range and response time, making it an ideal choice for applications requiring a high degree of versatility, such as nuclear spectroscopy and particle identification. In contrast, the circuit presented in the second research work prioritizes energy resolution and pulse shape discrimination through its innovative feedback scheme.

Although both circuits exhibit low noise performance and compatibility with different detector types, a wide-dynamic-range fast preamplifier circuit places a stronger emphasis on linearity and gain stability. On the other hand, the second research work centers on energy resolution. The appropriate choice between these two circuits ultimately depends on the specific requirements of an application, such as the desired dynamic range, energy resolution, and response time. By carefully evaluating the performance characteristics of each circuit, researchers and engineers can select the most suitable option for their needs.

Chapter 3 - Model Description and Results

3.1 Preamplifier Schematic Study

The design of the project preamplifier circuit is depicted in the Fig. 3.1. The project design analysis has been held with 50 pF detector capacitance with input current pulse signal.

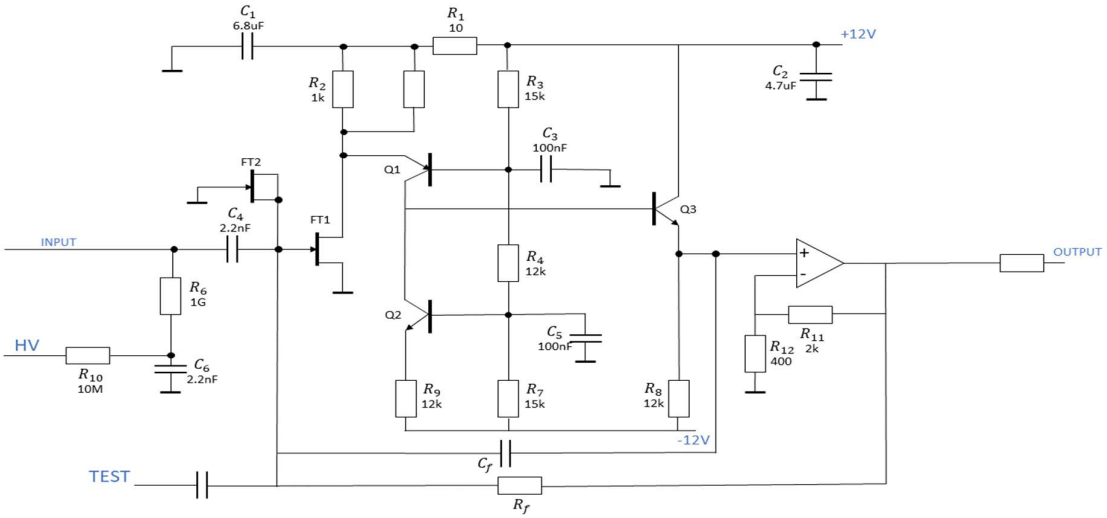

Figure 3.1: Preamplifier Design with Active Discharge Mechanism

The reason for choosing the design as the base for further modification were considered for couple of factors, which are:

- Final characteristics. The design introduced in [2] had the most optimal specification in comparison with other designs, which can be observed in Table 3.1.

Table 3.1: Preamplifier specification with BF862 [2]

Performance	BF862
Integral nonlinearity	±0.04%
Energy sensitivity	150mV/MeV
Rise time	4ns
Decay time	250μs
Power requirements	±12V
Power consumption	220mW
Typical noise at 0pF	0.750keV
Slope	8.5eV/pF
Board dimensions	18x38mm^2

- Design complexity. The structure of the design should not be complex, as it will produce difficulties in the further chip and PCB design and will be time-consuming for analysis and modification procedures. The components library for the base design can be observed in Table 3.2.

Table 3.2: Preamplifier schematic component list

Component Type	Model	Configuration	Quantity
N-channel JFET	BF862	Common Source	2
BJT	BFT92	N/A	2
BJT	BFR92	N/A	1
Operational Amplifier	CLC430	Non-Inverting Amplifier	1
DC Voltage Source	N/A	1000V, 12V, -12V	3

- The presence of sufficient data. Most of the introduced designs do not have sufficient amount of information on the design structure and components library. Research articles and scientific papers studying HPGe detector preamplifiers do not fully disclose the design or try to hide devices used and their values. This should be understandable, as

the preamplifier designs for HPGe detectors are implemented in the industries, and could be designated as strategic information.

- Cost of the design. Budget is essential for future analysis and modifications of the circuit, as the given project planned to be researched further for obtaining better results. Moreover, the design of the PCB and chip will also be hardly affected by the cost and complexity of the preamplifier structure.

For testing the circuit results, simulation studies has been applied with implementing typical input signal. The input signal is applied to the input of FT1 (BF862). The input current pulse amplitude comprises approximately 38 mA with 3 ns rise time. This is the typical value for the output of the detectors[1]. For the input a current pulse was integrated described in the Fig. 3.2.

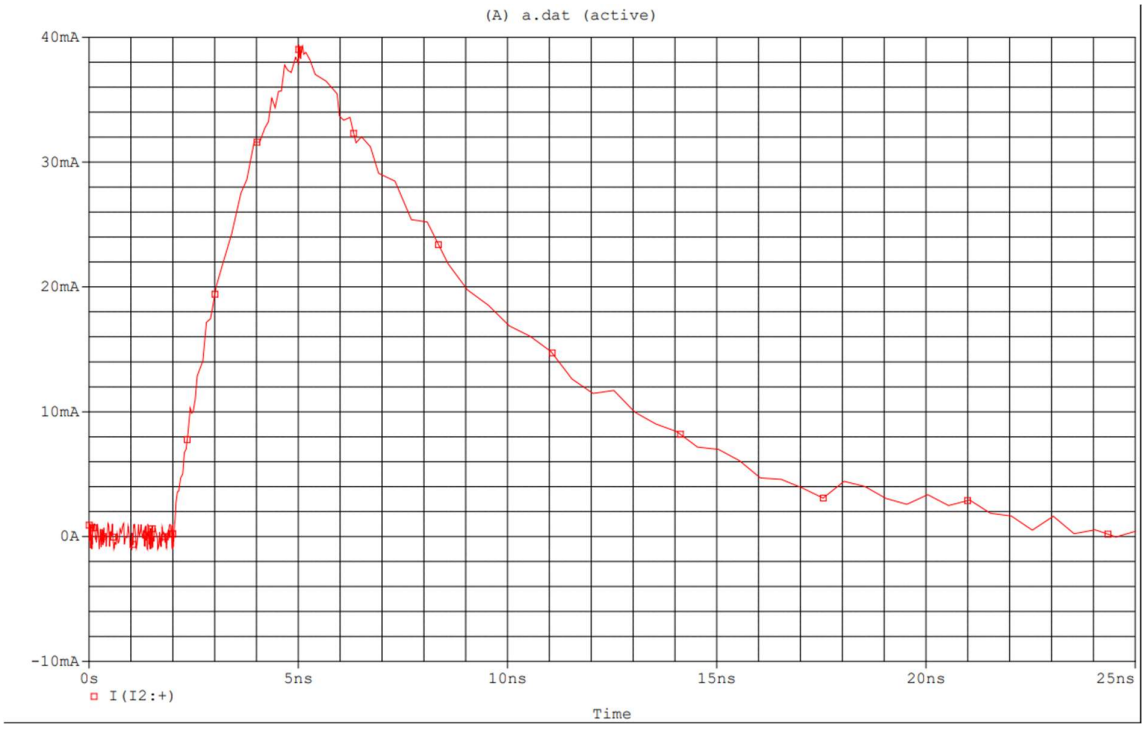

Figure 3.2: Input Pulse Shape

The circuit's input stage consists of a folded-cascade configuration with a FET (FT1) and a bipolar transistor (BJT) (Q1), followed by an active load (Q2). The gain of the cascade stage is determined by the product of FT1's transconductance and the dynamic impedance seen at Q1's collector. A FET (FT2) is included for protection purposes. The drain voltage of FT1 is set at around 4 V by the voltage on Q1's base, and the drain current can be adjusted with RADJ1 to set the gate voltage of FT1 at around 0 V. The circuit uses capacitance C_F as part of the principal feedback loop, making it a charge amplifier. The signal path runs through a noninverting amplifier, which sets the forward gain of a second loop that is used to "rapidly" discharge C_{F1}. The series of three resistors on the hybrid reduce the overall series stray capacitance of the device. The noninverting amplifier has a gain of 6 and is used as a buffer, with a back termination matched to a 50 Ω line. The output signal of the preamplifier circuit can be observed in the Fig. 3.3.

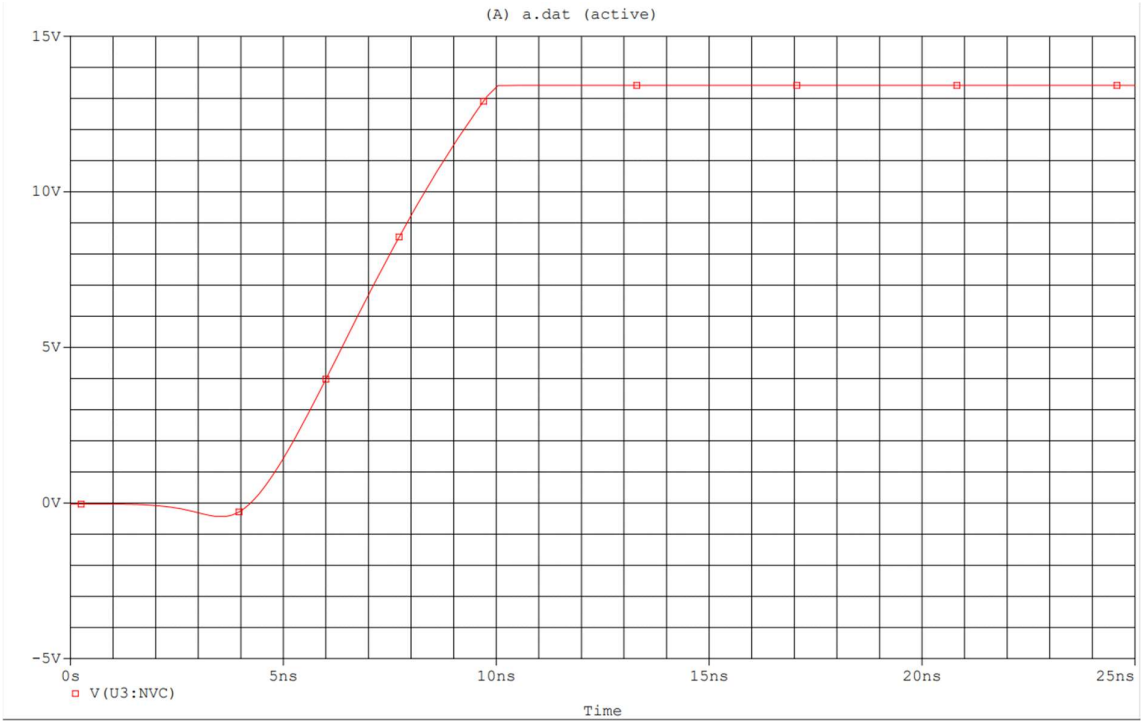

Figure 3.3: Output signal of the base circuit with 50pF detector capacitance

The analysis of the output stage depicts that the implemented Operational Amplifier CLC430 has increased the preserved magnitude of the rise time, while maintaining a relevant level of gain. The design of preamplifier requires fast amplifying node, to keep the rise time of the output signal low. The information of comparison of input/output signals depicted in the Fig. 3.4 and in the Table 3.3.

Table 3.3: Operational Amplifier analysis

Input Voltage	3.75 V
Output Voltage	13.42 V
Input signal Rise Time	2.16 ns
Output signal Rise Time	6.68 ns
Detector Capacitance	50 pF
Gain	3.57

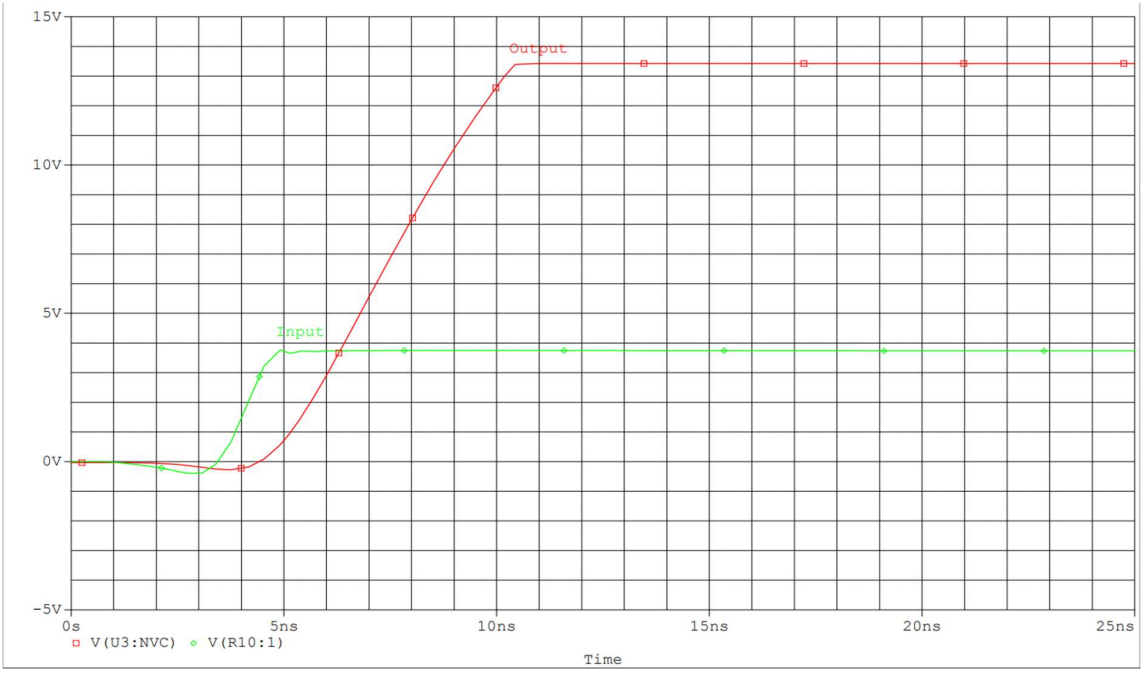

Figure 3.4: Input/Output of the Operational Amplifier CLC430

To optimize circuit performance in the terms of output signal rise time and gain various operational amplifier devices were tested in the room temperature conditions. For testing procedure only fast and low-noise operational amplifier devices were chosen. The results of the analysis have presented clear domination of operational amplifiers manufactured by Analog Devices company. For visual comparison and understanding only applicable examples of operational amplifiers were depicted in the Table 3.4.

Table 3.4: Operational amplifiers results

Operational Amplifier Model	Amplitude	Rise Time	Gain
AD8055an/AD	13.235 V	7.3572 ns	3.54
LM6171	13.424 V	7.3421 ns	3.59
AD8031a/AD	783.591 mV	1.8283 ns	-
OPA2107/BB	75.579 mv	-	-
AD8004	13.821 V	5.7184 ns	3.69
AD8009	13.870 V	4.0812 ns	3.71
AD8014	14.830 V	4.28 ns	3.96
CLC440	13.238 V	4.46 ns	3.54
AD8011	14.031 V	4.14 ns	3.75

The best results were taken from Operational Amplifier AD8014 with the highest gain amount comprising 3.96. The fastest rise time parameter was obtained by the use of AD8011, which is previous version of AD8014. In the context of optimizing both rise time and gain, it has been determined that the AD8014 is the most preferable option. The results of AD8014 output signal can be observed in the Fig. 3.5.

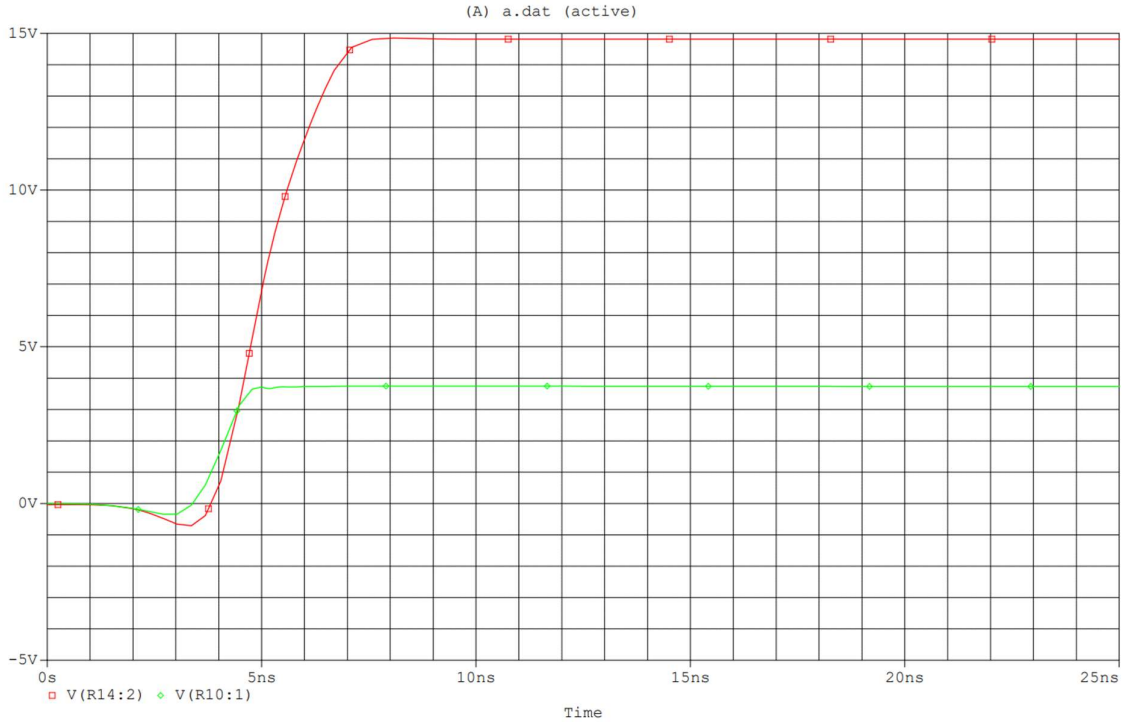

Figure 3.5: Input/Output with Operational Amplifier AD8014

As the next stage for improving the gain coefficient, the feedback resistance of the operational amplifier was calibrated. The basic feedback resistor was calibrated at 2 kΩ and depicted as R11 in the Fig. 3.1. The measurement was done by calibration of operational amplifier feedback resistor.

Table 3.5: Operational Amplifier feedback resistance calibration

Resistance	Gain	Rise Time
2 kΩ	3.96	4.28 ns
6 kΩ	4.05	4.23 ns
10 kΩ	4.04	3.64 ns
14 kΩ	4.07	4.17 ns
20 kΩ	4.07	3.98 ns

Input FET analysis

The input FET analysis have shown that BF862 is the most optimal choice for preamplifier design for HPGe detectors. Most of the research papers approve the use of BF862 due to high impedance, high gain and low-noise characteristics. However, other FET's were tested in the preamplifier design with similar parameters as BF862 and with higher transconductance rate. The testing results were illustrated in the Table 3.6 and held with AD8014 operational amplifier with 20 kΩ feedback resistor.

Table 3. 6: Input FET Analysis (Preamplifier output)

JFET Model	Output Signal Amplitude	Rise Time
BF862	15.274 V	3.98 ns
MPF102	15.196 V	4.03 ns
2SK170	15.197 V	4.07 ns
J309	15.236 V	10.14 ns
2SK117	15.271 V	4.01 ns
2N5457	---	---
2N4416A	15.159 V	3.09 ns

The first stage of input FET analysis was held on the output node of entire preamplifier block, by measuring the output signal rise time and gain effect. BF862 is considered to be the most optimal version as it had to be, however 2SK117 and MPF102 FET's depicted nearly the same performance. BF862, 2SK117 and MPF102 FET's interchangeable device with stable performance and analogous parameters. The performances of the input FET were also tested at the output node of FET. The results depicted in the Table 3.7.

Table 3. 7: Input FET Analysis (Input FET output)

JFET Model	Output Signal Amplitude	Rise Time
BF862	4.53 V	6.46 ns
MPF102	4.47 V	7.82 ns
2SK170	4.54 V	6.59 ns
J309	3.76 V	8.43 ns
2SK117	4.53 V	5.51 ns
2N5457	---	---
2N4416A	4.75 V	6.62ns

The results for input FET output stage had approximately same results. The leading 3 input FET's were BF862, MPF102 and 2SK177. 2N5457 and 2N4416A results were not stable and affected by noise.

BJT analysis

In this section the operation of BJT's have been tested by trying various BJT's. Specifically, Q2 and Q3 functioning and their effect on the overall performance of the design have been studied. Q2 in the circuit is responsible for gain, particularly for voltage amplification which is configured as common-emitter. Q3 responsible for the active discharge mechanism. It helps to quickly discharge the feedback capacitor (C_f) to restore the amplifier's baseline voltage when the input pulse is over. This active discharge mechanism significantly reduces the circuit's settling time, allowing for faster rise times and better overall performance. Test results were presented in the Table 3.8.

Table 3.8: Q2 and Q3 BJT analysis

BJT Model	Output Signal Amplitude	Rise Time
BFR92A	15.274 V	3.98 ns
BFP520	15.270 V	3.87 ns
BFP81	15.160 V	3.99 ns
BFP91A	15.286 V	4.24 ns
BFP93A	15.159 V	4.13 ns
BFP96	15.203 V	4.19 ns
BFG591	15.166 V	4.53 ns
BFQ196	15.235 V	3.87 ns
MMBR571/MC	15.206 V	4.17 ns
Q2SC3354	15.303 V	4.2 ns
2SC3355	15.312 V	4.36 ns
NE46134	15.157 V	4.44 ns
BFR93A	15.171 V	4.09 ns
BFR93AW	15.253 V	4.12 ns
MMBTH10	15.271 V	3.97 ns
BFQ236A	15.188 V	5.44 ns
BFQ232A	15.156 V	5.08 ns

The conducted simulation results depicted that BFP520, BFQ196 MMBTH10 has overall good performance in the preamplifier circuit. BFP520 stands out from the list with improved rise time by approximately 0.1 ns, which is in general positive trend for preamplifier signal.

For the input node BJT (Q1) BFT92W has been simulated. This is the only possible choice for input BJT, as other simulated BJT's depicted nonlinearity and high losses in gain. The obtained rise time with BFT92W resulted in 0.1 ns positive reduction, while maintaining the same level amplitude. The overall obtained rise time with combination of BFT92W as Q1 and BFP520 as Q2 and Q3 resulted in **3.7 ns** and **15.270 V** voltage (Fig. 3.1.6).

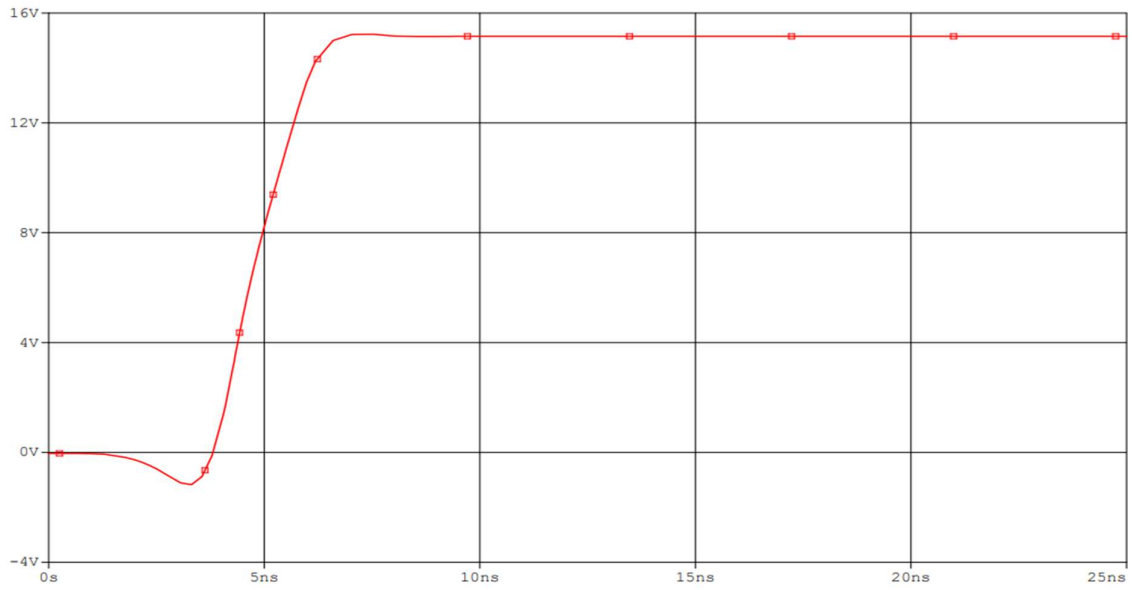

Figure 3.6: Output with modified BJT's

Feedback Calibration

The circuit uses a feedback resistor (R_f) and a feedback capacitor (C_f) to determine the amplifier's gain and time response.

The output signal's rise time mostly depends on the feedback capacitor (C_f) and the detector's input capacitance (C_d). To enhance the rise time, C_f value could be decreased . This action would decrease the time constant ($\tau = R_f \times C_f$) and lead to a faster rise time. However, reducing C_f might result in higher output noise, so it's essential to strike the right balance between rise time and noise performance.

As for the gain, it relies on both the feedback resistor (R_f) and the feedback capacitor (C_f). The gain (A) value is calculated using the formula A = R_f /C_f. There are few options to boost the gain: increase R_f, decrease C_f, or modifying both parameters. The results were tested with modified BJT's, AD8014 with 20kΩ and BF862 in the input. The detector capacitance as default was set 50 pF.

The aim of the experiment was to obtain better results of the rise time and gain. The Table 3.9 demonstrates the results of feedback calibration.

Table 3.9: Feedback calibration

R_f, GΩ	C_f, pF	Rise time, ns	Amplitude, V
2	0.5	3.92	15.290
2	1	3.96	15.236
2	1.5	3.71	15.264
4	0.5	3.81	15.309
4	1	3.85	15.317
4	1.5	4.12	15.285
8	0.5	3.58	15.276
8	1	3.81	15.267
8	1.5	4.19	15.212
10	0.5	3.79	15.292
10	1	3.94	15.290
10	1.5	3.65	15.271

The results illustrate that configuration with R_f – 8 GΩ, C_f – 0.5 pF and R_f – 10 GΩ, C_f – 1.5 pF exceeds the range of 3.7 ns rise time and obtains positive trend of voltage.

Noise Analysis

Figure 3.7 presents a comparison between the noise analysis of the initial and modified preamplifier circuits at varying input capacitance levels, with a shaping time of 3 μs employed for an in-depth examination of the noise figure. As evident from the figure, the initial circuit demonstrates lower noise interference at reduced input capacitance levels. For example, the overall noise for the initial circuit design is 691 eV FWHM at 10 pF, 882 eV FWHM at 20 pF, and 1003 eV FWHM at 30 pF of input capacitance. Conversely, the modified circuit exhibits increased noise contribution, attributed to the higher feedback resistor and lower feedback capacitance values. The noise levels for the modified circuit are 814 eV FWHM at 10 pF, 903 eV FWHM at 20 pF, and so on. Table 3.10 enumerates the noise values corresponding to various input capacitance levels. The modified circuit displays superior performance for input capacitance levels above 40 pF and maintains an approximate slew rate of 120 eV per 10 pF, representing an optimal outcome for preamplifier circuits.

Table 3.10: Initial & Modified circuit noise values

	Noise, eV FWHM	**Input Capacitance, pF**
Initial Circuit	691	10
	882	20
	1003	30
	1133	40
	1441	50
	1677	60
Modified Circuit	814	10
	903	20
	1078	30
	1177	40
	1301	50
	1481	60

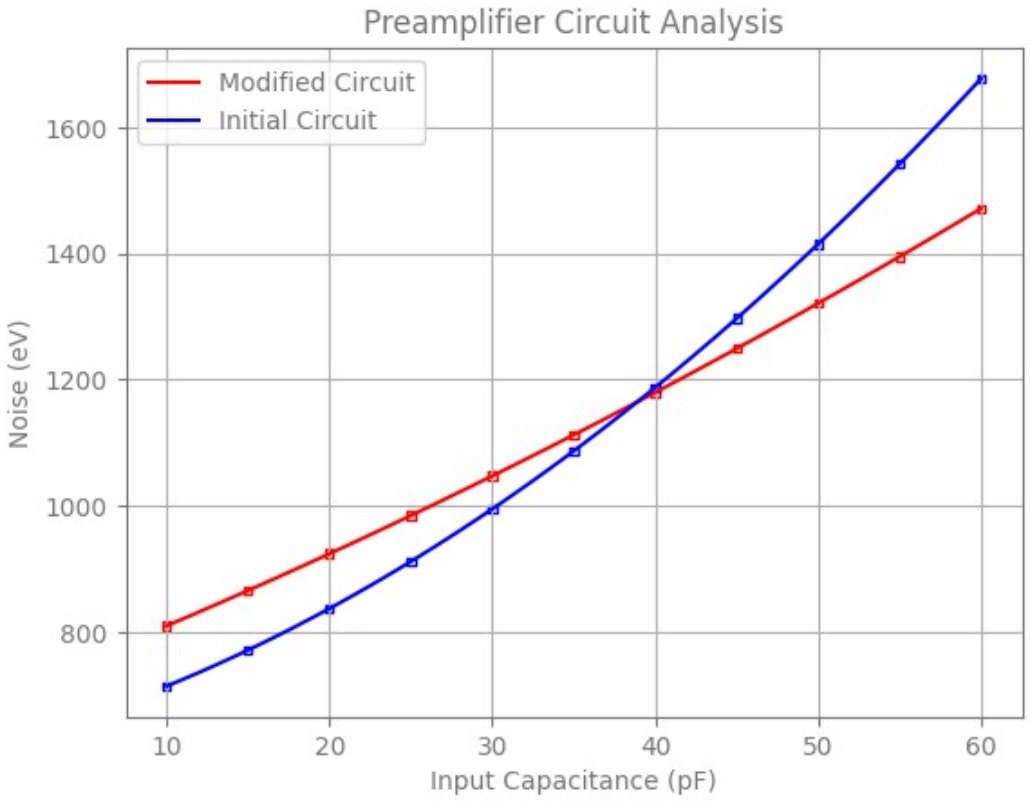

Figure 3.7: Initial & Modified preamplifier circuit noise analysis

Summary

As the results of the preamplifier design analysis and simulation tests, the new design for preamplifier circuit with modified parameters has been studied. The initial preamplifier design had the parameters listed in the Table 3.3, specifically with the rise time 6.68 ns and output voltage amplitude comprising 13.42 V. The noise performances of the circuit indicated 691 eV at 10 pF, while increasing detector capacitance to 50 pF resulted in the increase of noise interaction to 1441 eV with shaping time of 3 µs.

As the input for the preamplifier circuit, 50mA current pulse has been used with 50pF modelled detector capacitance. All of the measurements were conducted in the conditions of the room temperature and simulated by the Orcad Capture CIS software from Cadence.

Step by step analysis of the circuit have depicted the points of the circuit that require

optimization and modification procedures. First of all, amplifying node of the schematic has been simulated to analyze the performance of the circuit with 50 pF detector capacitance. The utilized Operational Amplifier had showed significant slowdown of the rise time, by increasing the value almost to 4ns. The Operational Amplifier analysis illustrated that there are many other options of amplifying devices with better results of gain and speed. The operational amplifiers introduced by the company Analog Devices had the best results among all of the tested devices. AD8014 operational amplifier differed from the list with the best performance characteristics of gain, speed and noise. Consequently, the feedback line of the operational amplifier has been calibrated to obtain higher gain, while keeping low noise and fast rise time.

Special care has been taken to the input node of the preamplifier. The results have showed, that BF862, MPF102 and 2SK177 are the most optimal choices for HPGe detector input. The amplifying node of the preamplifier has been also get modified by the modification of BJT's used in the schematic. As the results, BFP520 has replaced the old BJT BFR92A and input has been replaced by BFT92W. The modification resulted in the overall improvement of reaching 3.7 ns rise time and 15.270 V voltage output. Finally, the feedback calibration analysis has been held.

Chapter 4 – PCB Design

4.1 Feasibility study of the chip fabrication

This chapter examines the feasibility of fabricating a preamplifier circuit as an integrated chip for use in HPGe detectors, focusing on the benefits, barriers, detailed fabrication process, features, and the companies and industries involved in chip fabrication worldwide. The further listed section includes PCB design CAD file, which need to be verified and tested in multiple conditions in real-time for further creation of chip design.

4.1.1 Opportunities and Barriers

Benefits:

1. Miniaturization: Chip fabrication enables significant size reduction, allowing easy integration into compact systems and portable devices [16].
2. Improved performance: Chip fabrication can offer better electrical performance by reducing parasitic elements and shortening interconnections, potentially improving the signal-to-noise ratio, energy resolution, and response time [17].
3. Enhanced reliability: Integrated chips provide higher reliability and longer lifetimes compared to discrete components due to reduced susceptibility to environmental factors and mechanical stress [18].
4. Cost reduction: Chip fabrication can result in cost savings, especially for high-volume production, as the cost per unit decreases with increasing production quantities [19].

Barriers:

1. Design complexity: Designing a preamplifier circuit for chip fabrication demands specialized knowledge of integrated circuit design and semiconductor processes, which may be more complex than designing a circuit using discrete components [20].

2. Fabrication process limitations: Integrating some features of the preamplifier circuit, such as high-voltage components or custom passive components, into standard chip fabrication processes may prove challenging [21].
3. Initial investment: Developing a preamplifier circuit for chip fabrication requires a substantial initial investment in design and fabrication, potentially making it prohibitive for small-scale production or research projects [22].

4.1.2 Detailed Process of Chip Fabrication

1. Schematic design: Design and simulate the preamplifier circuit using a schematic capture tool such as Orcad Capture CIS or Cadence Virtuoso [23].
2. Layout and physical design: Transition to a layout and physical design software (e.g., Cadence Virtuoso) to create the chip layout based on the schematic [23].
3. Design Rule Checks (DRC) and Layout Versus Schematic (LVS) checks: Perform these checks to ensure the layout complies with fabrication process requirements and accurately represents the schematic [23].
4. Parasitic extraction and post-layout simulation: Extract parasitic elements from the layout and run a post-layout simulation to ensure the chip design meets performance specifications [24].
5. Generate output files: Create output files required by the foundry for fabrication (e.g., GDSII) [25].
6. Fabrication: Collaborate with a semiconductor foundry to fabricate the chip using a suitable process (e.g., CMOS, bipolar, or BiCMOS) [26].
7. Packaging and assembly: Package the fabricated chip and assemble it with the necessary components [28]. Testing and validation: Test the fabricated chip to ensure it meets performance and reliability requirements [27].

8. Testing and validation: Test the fabricated chip to ensure it meets performance and reliability requirements [27].

4.1.3 Features of Chip Fabrication

1. Scalability: Chip fabrication enables scaling of the design for various applications and integration requirements [28].
2. Customizability: Chip fabrication allows for the customization of the design to meet specific performance requirements or to optimize for specific detector types [27].
3. Integration with other components: Fabricating the preamplifier circuit as a chip facilitates integration with other components, such as Analog-to-Digital Converters (ADCs) or Digital Signal Processors (DSPs), on a single chip or within a System-in-Package (SiP) solution [28].

4.1.4 Companies and Industries in Chip Fabrication

1. Semiconductor foundries: These companies specialize in manufacturing integrated circuits based on designs provided by their clients. Examples of prominent semiconductor found include Taiwan Semiconductor Manufacturing Company (TSMC), GlobalFoundries, United Microelectronics Corporation (UMC), and Samsung Electronics [31].
2. Electronic Design Automation (EDA) companies: These companies develop software tools used in the design, simulation, and verification of integrated circuits. Major EDA companies include Cadence Design Systems, Synopsys, Mentor Graphics (a subsidiary of Siemens), and Keysight Technologies [29] - [32].
3. Integrated Device Manufacturers (IDMs): IDMs are companies that both design and manufacture their integrated circuits. Examples of well-known IDMs include Intel, Texas Instruments, and STMicroelectronics [31].

4. Fabless semiconductor companies: These companies focus on the design of integrated circuits and outsource the manufacturing to semiconductor foundries. Notable fabless semiconductor companies include Qualcomm, NVIDIA, and Broadcom [32].
5. Semiconductor IP (intellectual property) providers: These companies develop and license reusable circuit designs, known as IP cores, to help accelerate chip design and reduce development costs. Examples of semiconductor IP providers include Arm, Rambus, and CEVA [35].

4.2 PCB Design CAD file

The PCB design of the preamplifier circuit for the HPGe detector was created using EasyEDA software, with board dimensions of 18x38 mm. The PCB consists of two layers to accommodate the numerous connections between the components, ensuring efficient signal routing and optimal performance.

Fig. 4.1 presents top layer view of the PCB design. The PCB design routes are made of copper with the width of 1.5 mm. Allowed maximum angle of routes are 45°. DRC and LVS tests have illustrated successful results. 4 holes have been made on the corner edges of the board, to make it comfortable to mount. Fig 4.2 illustrates bottom layer of the board, while Fig. 4.3 and 4.4 depicts 3D view of the PCB from both sides.

Table 4.1: Bill of Materials of PCB fabrication

No.	1	2	3	4	5	6	7	8
Quantity	1	2	2	2	1	1	3	1
Comment	AD8014	BF862	R2,Rvar	R3,R7	R_f	R6	R4,R8,R9	R11
Designator	Op. Amp	JFET	Resistor	Resistor	Resistor	Resistor	Resistor	Resistor
Footprint	SOIC-8	SOT-23	smd120612	smd120612	smd120612	smd120612	smd120612	smd120612
Value	N/A	N/A	1k	15k	8G	1G	12k	20k
Manufacturer	Analog Devices	NXP Semiconductors	Yageo	Yageo	Yageo	Yageo	Yageo	Yageo
Supplier	Digi-key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key

No.	9	10	11	12	13	14	15	16
Quantity	1	1	1	2	1	1	2	1
Comment	R12	R10	R1	C3,C5	C1	C2	C4,C6	C_f
Designator	Resistor	Resistor	Resistor	Capacitor	Capacitor	Capacitor	Capacitor	Capacitor
Footprint	smd120612	smd120612	smd120612	smc0805	smc0805	smc0805	smc0805	smc0805
Value	400	10M	10	100nF	6.8uF	4.7uF	2.2nF	0.5pF
Manufacturer	Yageo	Yageo	Yageo	Yageo	Yageo	Yageo	Yageo	Yageo
Supplier	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key	Digi-Key

No.	1	2
Quantity	1	2
Comment	BFT92W	BFP520
Designator	BJT Q1	Q2,Q3
Footprint	SOT-23	SOT-23
Value	N/A	N/A
Manufacturer	NXP Semiconductors	Infineon Technologies
Supplier	Digi-Key	Digi-Key

The Bill of Materials (BOM) is a crucial document for PCB and chip fabrication as it lists all the necessary components required for the manufacturing process. This important document lists every single component needed for manufacturing, so it's crucial to make sure that everything is available and accounted for before production begins. The BOM also serves as a reference for quality control, ensuring that the correct components are used during the manufacturing process. This helps to prevent any mistakes that could lead to problems down the line. The table 4.1 in this paper provides a detailed breakdown of all the components needed for PCB fabrication, including their quantities, footprints, and manufacturers.

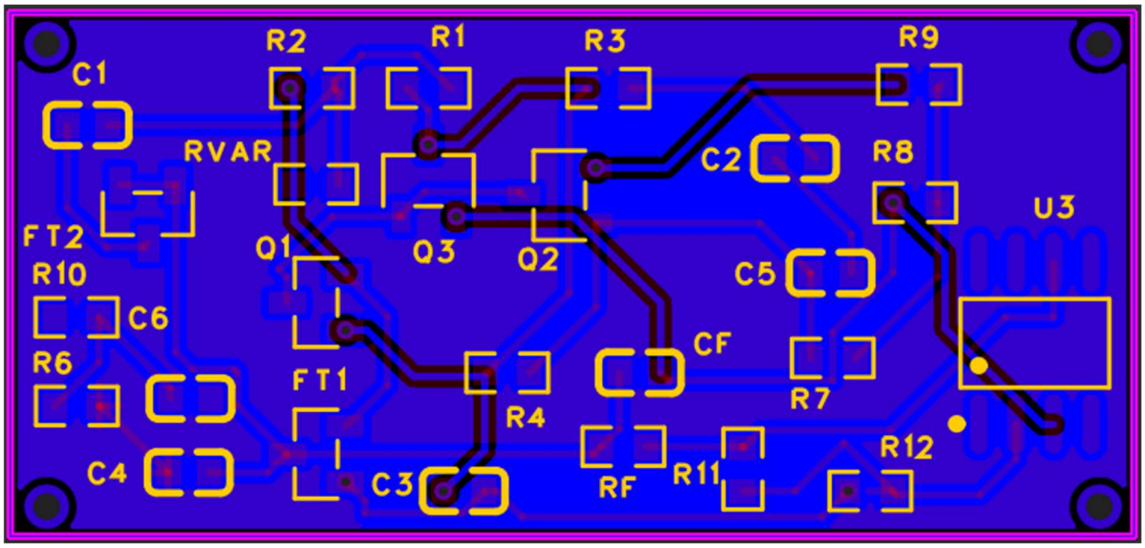

Figure 4.1: PCB board top layer

Figure 4.2: PCB board bottom layer

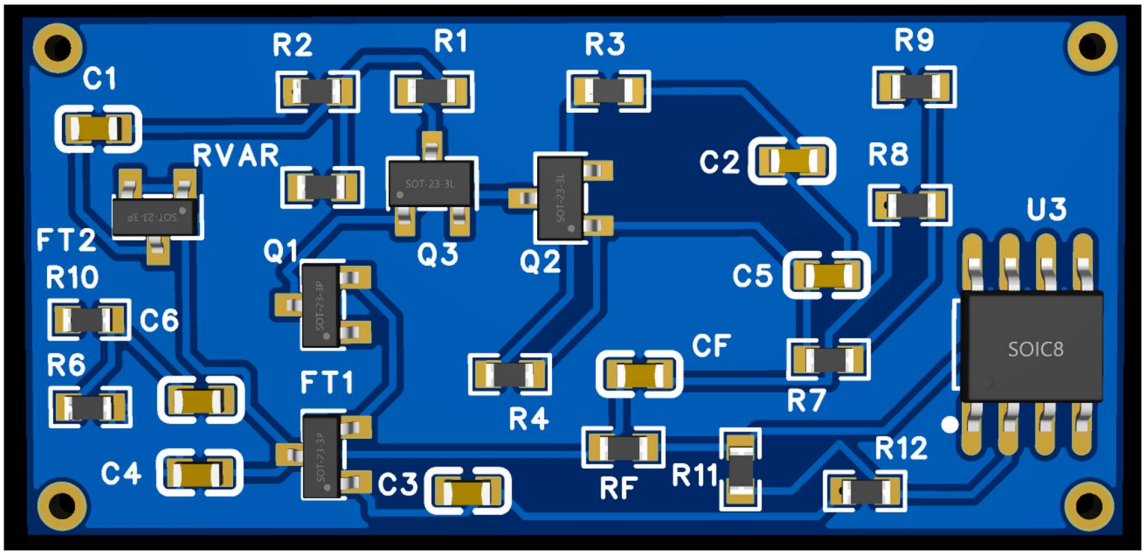

Figure 4.3: PCB board 3D view top layer

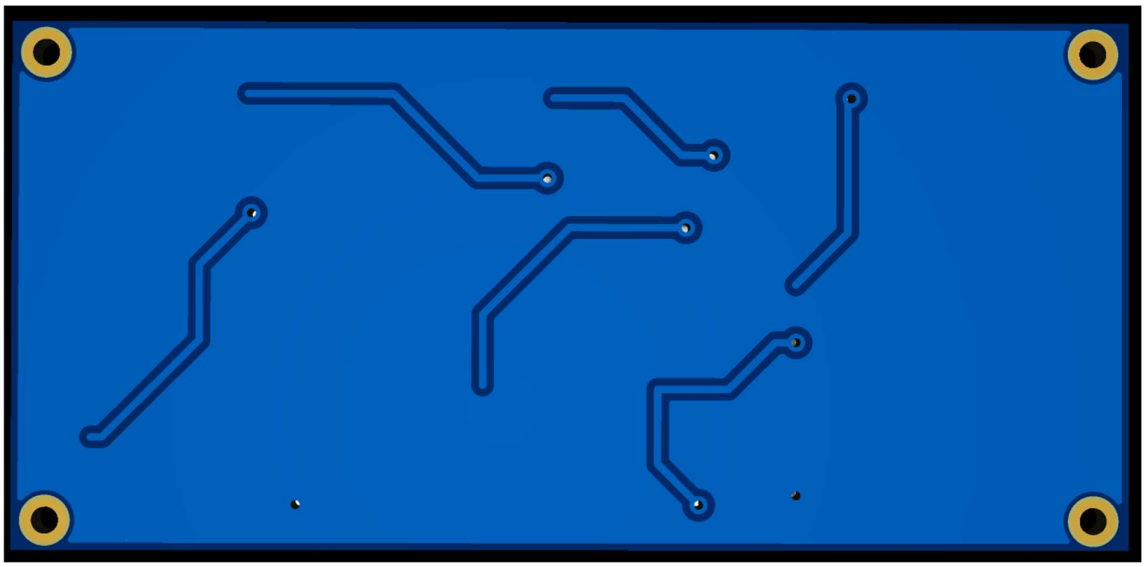

Figure 4.4: PCB board 3D view bottom layer

4.3 Summary

The feasibility of fabricating a preamplifier circuit as an integrated chip for HPGe detectors involves a careful consideration of the opportunities and barriers associated with chip fabrication [23]. The detailed process of chip fabrication encompasses schematic design, layout and physical design, design rule checks, parasitic extraction, post-layout simulation, and testing and validation [24]. The chip fabrication industry includes semiconductor foundries, EDA

companies, IDMs, fabless semiconductor companies, and IP providers, each playing a crucial role in the development and production of integrated circuits [25]. By thoroughly evaluating the specific requirements of a preamplifier circuit for HPGe detectors and considering the trade-offs between different fabrication processes, it is possible to determine the feasibility of chip fabrication for a particular application [26]. The chapter encompasses the development of the PCB design for the circuit, which necessitates implementation and verification under various conditions in real-time prior to proceeding with the chip design. The complexity and substantial cost associated with chip design fabrication mandate a meticulous approach, ensuring the elimination of errors throughout the process.

Chapter 5 – Conclusions

In conclusion, this Master's thesis aimed to investigate and analyze existing preamplifier designs for HPGe detectors and compare their performance characteristics. The primary objective of this research was to modify current designs and create new designs with improved parameters in terms of gain, rise time, and noise. The Orcad software was utilized to simulate and analyze the performance of the preamplifier circuits.

Through the study, several preamplifier designs were examined, and potential areas for modification and optimization were identified. The study focused on optimizing the preamplifiers SNR to improve their performance. The comparative analysis of the performance of the optimized designs and the current ones revealed that the optimized designs showed significant improvements in their gain, rise time, and noise parameters.

The final implemented preamplifier design yielded excellent performance characteristics, with a rise time of 3.58 ns and voltage of 15.276 V, and noise of 1301 eV with a 50 pF detector capacitance. These parameters represent a significant improvement over the previous design, which had a rise time of 6.68 ns and voltage of 13.42 V, and noise of 1441 eV. The optimized design thus offers superior performance in terms of speed, sensitivity, and noise reduction. Moreover, the complexity of the design has been kept simple, low cost, and with low power consumption, making it a promising candidate for practical applications in various fields, including nuclear physics, materials science, and medical imaging.

Furthermore, the study included the creation of the PCB design of the implemented final preamplifier circuit. The feasibility study of chip fabrication was conducted to assess the potential for successful chip fabrication. The results of the feasibility study showed that the PCB design should be verified in real-time conditions, to proceed with further chip design and fabrication.

Overall, this research has shown that the optimization of preamplifier designs can significantly improve the performance of HPGe detectors. The Orcad software proved to be an effective tool for simulating and analyzing the performance of the preamplifier circuits. The PCB design creation and feasibility analysis of chip fabrication further demonstrated the potential for applying the optimized preamplifier designs in practical applications. Future work will include further verification of PCB design in real-time conditions and chip design and possible fabrication processes.

In conclusion, this research provides valuable insights into the optimization of preamplifier designs for HPGe detectors, which can be useful for improving the performance of such detectors in various fields such as nuclear physics, materials science, and medical imaging. Further studies can be conducted to explore additional optimization techniques and to evaluate the performance of the optimized preamplifiers in practical applications.

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