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Flexible Design Scheme for a Simple Dual-Band Ultra-High Impedance Transformer and Its Application in a Balun

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ABSTRACT A dual-band impedance transformer for achieving very high impedance transformation (k) and frequency ratio (r) is presented in this paper. The design is accompanied by a thorough analysis and systematic design procedure for facilitating the rapid development of the prototypes. A number of case studies show the excellent design flexibility of the proposed design in regards to achieving ultra-high k and r . Two prototypes, with very high design specifications, working at concurrent $r = 5$, $k = 8.04$ and $r = 15$, $k = 20$ are fabricated to validate the proposed architecture and the design procedure. Subsequently, the application of the proposed impedance transformer is demonstrated in the design of a dual-band balun architecture with inherent impedance transformation capability. To evaluate the performance and the presented concept, an impedance transforming balun prototype is fabricated and the excellent agreement between the simulation and experimental results is a testament to the effectiveness of the proposed design.

INDEX TERMS Closed-form equations, dual-band, high frequency ratio, impedance matching, impedance transformer, microstrip line, ultra-high impedance transformation.

I. INTRODUCTION

Impedance matching or transformation is one of the key aspects often required in electronic circuits and systems. Its role is more significant in RF and Microwave Circuits and Systems considering the premium attached with the available power at high frequencies [1]–[4]. In hindsight, impedance transformation is essentially used for matching unequal impedance environments. There have been reports of many matching techniques to address the needs of variety of applications [5]–[8] and these can be broadly categorized into single-band and multi-band impedance transformation approaches [10], [12]–[24]. The last decade has seen emerging wireless applications and hence resulted in requirements of multi-band circuits and components. This effectively necessitated innovative multi-band impedance

transformation techniques [9]–[19]. Many of these designs report innovative techniques that can achieve high impedance transformation ratio (k) and high frequency ratio (r) so that they can find usefulness in the design of modern wireless communication system components. Furthermore, inherent impedance transformation is an important feature for the wireless system components as they discard the need for additional impedance transformers [25]–[33].

One of the important wireless applications that is commonplace is the dual-mode handsets and this needs appropriate matching at various circuit stages. In this context, a dual-band impedance transformer is characterized by its ability to provide matching between wide range of impedance values at varied range of frequency ratios. It provides the impedance matching techniques the desired scalability and flexibility to meet any design specification. It is important to mention that in the domain of the dual-band impedance transformers, r refers to the ratio of the second frequency (f_2) to the first

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frequency (f_1), and k refers to the ratio of the load impedance (Z_L) to the source impedance (Z_S).

Literature is replete with multiple design techniques to achieve the dual-band impedance transformation. For example, one of the most cited dual-band impedance transforming architecture with two stepped-transmission line was proposed almost two decades ago [12]. Though the proposed architecture was able to provide very high k and r theoretically, a case reveals that this impedance transformer faces fabrication challenges on FR4 substrate for k beyond 8.0 at $r = 3$. Recently, a real-to-real dual-band impedance transformer [13] was reported which utilizes slow wave architectures to achieve the impedance transformation at two arbitrary design frequencies. Another recent impedance transformer, based on a novel dual-transmission line approach [14], provides high k at high r . Several short-open stubs based architecture were also reported recently to mitigate the high impedance transformation challenges [15]–[17]. The short/open-circuited stubs, used at the ports of a single transmission line (TL), provide the dual-band complex impedance transformation [15]. Other examples with similar stub based architectures are of three stepped transmission line with three short-/open-circuited shunt stubs [16], and three stepped transmission line with two short-/open-circuited shunt stubs [17]. In these designs, the role of the stubs is to provide a transmission zero in addition to the required impedance matching. A ladder based network for the impedance transformation can be used for the multi-band impedance transformation, but it suffers from increased size and design complexities with the increasing number of bands [18]. Furthermore, sometimes these dual-band impedance transformers can be augmented by load healing technique to enhance the range of k to some extent [19]. Overall, it can be inferred that the available techniques are able to meet the needs of many applications but are often limited for applications requiring concurrent high k and high r .

In this paper, therefore, a simple structure of dual-band impedance transformer capable of achieving very high k at two arbitrarily distant frequencies is proposed. The proposed design is also capable of providing high k and high r concurrently. The design analysis augmented with a systematic design procedure is provided for facilitating quick prototyping. A number of design examples are included to comprehensively elaborate on the flexible design procedure, performance enhancement, and advancement in the domain of dual-band impedance transformer state-of-the-art. Two prototypes at distinct design specifications are presented and the excellent agreement between the measurement and the EM simulation results demonstrate the effectiveness of the proposed impedance transformer at high and arbitrary r and k . Overall, the proposed impedance transformer is capable of providing a) real and complex impedance transformations, b) very high k , c) very high r , and, d) very high concurrent k and r . Subsequently, it is demonstrated that the proposed impedance matching technique is extremely important in

variety of systems to simplify their overall designs. One such important application is the design of a dual-band balun. A dual-band balun based around the proposed impedance matching approach is developed and it is shown that the design readily achieves all ports matching and isolation. This assertion is validated through a prototype of the designed balun embedded with the proposed impedance transformation. It is shown that excellent agreement exists between the measurement results and the EM simulation results and thus validates the presented concept.

The next section presents the design of the proposed impedance transformer and its corresponding analysis. Further, Section III plays an important role to highlight the design flexibility of the proposed impedance transformer. A systematic and flexible design procedure is explained through a design flow chart and many design examples are discussed correspondingly. The section IV evaluates the performance of the proposed impedance transformer at very high design specifications, i.e., concurrent high r and k . The features of the proposed design are also compared with the recently reported dual-band impedance transformers in this section. Subsequently, in Section V the application of the proposed impedance transformer is demonstrated in a dual-band impedance transforming balun with the experimental results. Finally, section VI concludes the paper.

II. PROPOSED IMPEDANCE TRANSFORMER

The proposed impedance transformer, shown in Fig. 1, consists of a simple architecture with one coupled-line and two open-/short-circuited stubs. These two stubs have the characteristics impedance and electrical length as Z_a (in Ω), θ_a (in $^\circ$) and Z_b (in Ω), θ_b (in $^\circ$) respectively. The coupled-line has even and odd mode impedances as Z_e (in Ω) and Z_o (in Ω), respectively and the electrical length is θ_c (in $^\circ$). Terms Y_a , Y_b , and Y_c denote the respective admittances.

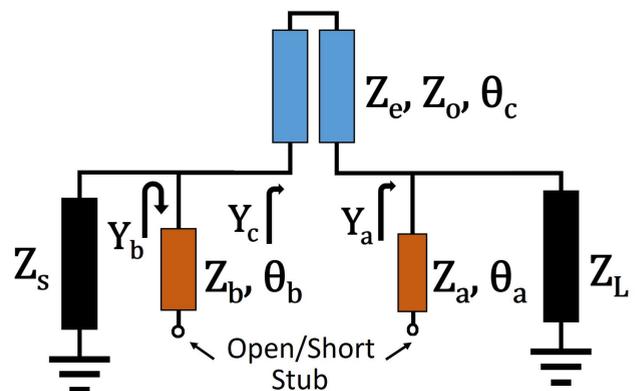


FIGURE 1. Proposed circuit for the dual-band impedance transformer.

The expressions for Y_a , and Y_c are deduced following the TL theory and are mentioned in (1) and (2), respectively [34]. The electrical lengths follow the expression (6) for the dual-band operation at two arbitrary frequencies where r is the frequency ratio [35].

$$Y_a = \frac{1}{Z_L} + \frac{1}{jZ_a \tan \theta_a} \text{ for short circuit}$$

$$Y_a = \frac{1}{Z_L} + \frac{j \tan \theta_a}{Z_a} \text{ for open circuit} \quad (1)$$

$$Y_c = \frac{C_1 + D_1 Y_a}{A_1 + B_1 Y_a} \quad (2)$$

here,

$$A = D = \frac{Z_e \cot \theta_c - Z_o \tan \theta_c}{Z_e \cot \theta_c + Z_o \tan \theta_c} \quad (3)$$

$$B = \frac{2jZ_e Z_o}{Z_e \cot \theta_c + Z_o \tan \theta_c} \quad (4)$$

$$C = \frac{2j}{Z_e \cot \theta_c + Z_o \tan \theta_c} \quad (5)$$

$$\theta_i = \frac{(1+n)\pi}{1+r}; \quad n \in (0, 1, 2, \dots); i \in [a, b, c] \quad (6)$$

The real and imaginary parts of Y_c are equated with $1/Z_S$ and negative of Y_b respectively for the required impedance transformation. These two conditions are expressed in (7) and (8), and solution of these provide the design parameters of the proposed impedance transformer. To solve (7), any two variables from Z_e , Z_o , and Z_a can be considered to be independent as per the suitability and can be chosen in the range of $[20 \Omega - 150 \Omega]$ for the realizable design parameters.

$$\text{Re}[Y_c] = \frac{1}{Z_S} \quad (7)$$

$$\text{Im}[Y_c] = -Y_b \quad (8)$$

where,

$$Y_b = \frac{1}{jZ_b \tan \theta_b} \text{ for short circuit}$$

$$Y_b = \frac{j \tan \theta_b}{Z_b} \text{ for open circuit} \quad (9)$$

III. DESIGN FLOW CHART AND CASE STUDIES

A. DESIGN FLOW CHART

To enable quick prototyping of the proposed impedance transformer, a design flow chart is provided in Fig. 2. The design flow chart is summarised below for the better understanding of the design procedure.

- 1) Compute r and k based on specified frequencies of operations and port terminations Z_L and Z_S .
- 2) Calculate electrical lengths θ_a and θ_c using (6). Initially, keep $n = 0$ for minimized architecture. Assume any combination of open/short-circuited stubs.
- 3) Use eq. (7) to find the unknown design parameter. Here, any two variables out of Z_a , Z_e , and Z_o can be chosen as independent variables. However, the selection of Z_e and Z_o may be opted with high coupling coefficient for the wider bandwidth [28].
- 4) In case the calculated parameter is not realizable, increment n in step 2. The selection of open- (or short-) circuited stub (Z_a , θ_a) can also be altered.

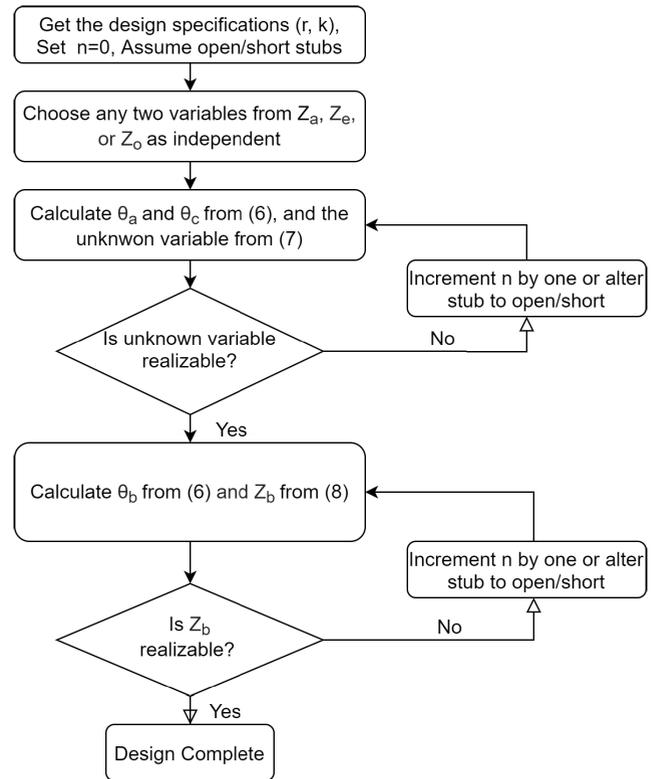


FIGURE 2. Flow chart for the quick prototyping of the proposed IT.

- 5) Further, calculate electrical length θ_b , keeping $n = 0$. Solve eq. (8) to calculate Z_b .
- 6) In case Z_b is not realizable, increment n in step 5. Again, the selection of open- (or short-) circuited stub (Z_b , θ_b) can also be altered.

The proposed design and the flow chart envisages the following important aspects: 1) the proposed design has two stubs with the choices of being open- or short-circuited, 2) the design analysis demonstrates that there are two independent design variables, 3) the choice of selecting two independent design variables out of three Z_a , Z_e , and Z_o , and, 4) the independent selection choices of n for θ_a , θ_b , and θ_c in (6). Owing to the possibilities in computing the design parameters, the design procedure validates the enhanced design flexibility of the proposed impedance transformer. It makes the proposed design extremely suitable for a very wide range of design specifications in terms of r and k .

B. CASE STUDIES: IMPEDANCE TRANSFORMER AT VARIOUS FREQUENCY RATIOS

It has been explained in the last sub-section that the design procedure is very flexible. Now, variety of case studies are discussed in order to show its effectiveness and design flexibility in practical scenarios. In essence, the proposed impedance transformer is assessed and evaluated for a wide range of possible k for varied values of arbitrarily selected r .

At first, the impedance transformer is designed for the varying r for a fixed k of 2. This example enables evaluation

TABLE 1. Design examples with variation in r ($k = 2$, $Z_S = 50\Omega$ is fixed for all cases) [Var*: Design parameters, S: short-circuited, O: open-circuited].

Var*	r=2 case 1	r=4 case 2	r=6 case 3	r=8 case 4	r=10 case 5	r=15 case 6	r=20 case 7	r=30 case 8
$Z_a(\Omega)$	65.8	105	65	46.9	35.3	23.6	133.8	40.4
$\theta_a(^{\circ})$	60(S)	36(O)	25.7(O)	20(O)	16.4(O)	11.25(O)	77.1(S)	46.4(O)
$Z_e(\Omega)$	86	94	107	121	140	160	55.6	67
$Z_o(\Omega)$	56	67	84	95	109	140	37.3	54.2
$\theta_c(^{\circ})$	60	36	25.7	20	16.4	11.25	34.3	5.8
$Z_b(\Omega)$	45.5	98	103	144	143.8	126.3	86.4	128.7
$\theta_b(^{\circ})$	60(S)	36(O)	25.7(O)	20(O)	16.4(O)	11.25(O)	34.3(S)	11.6(S)

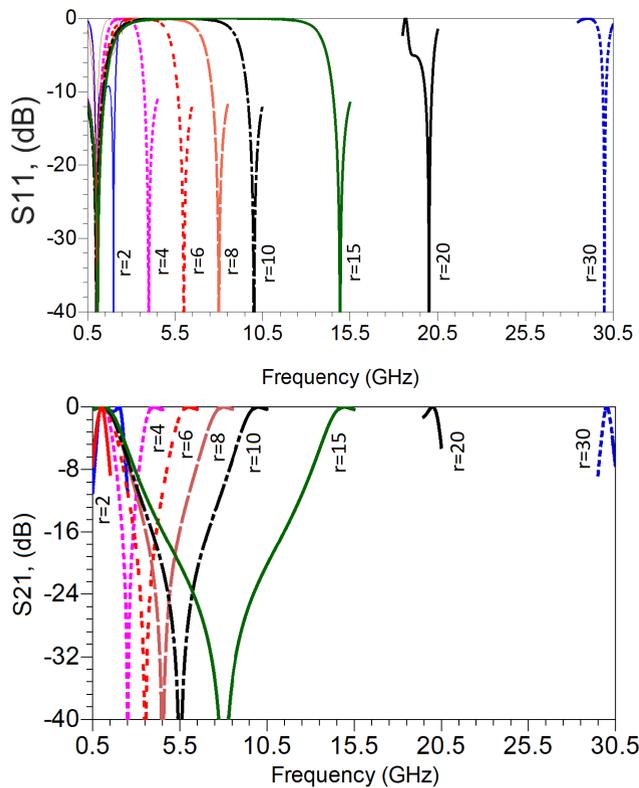


FIGURE 3. Simulation performance of the design examples of Table 1.

of the design for the identification of possible extreme values of r for a fixed value of k . A number of design examples mimicking this situation are listed in Table 1 along with the corresponding design parameters. It is clear that all the design parameters are realizable for cases varying from $r = 2$ to $r = 30$. The circuit simulation results for all these design cases are plotted in Fig. 3. The results for the cases 7 and 8 are depicted only around the design frequencies for clarity purposes. It is now safe to comprehend from these results that the impedance transformer achieves excellent performance for the values of r up to 30. Furthermore, the proposed impedance transformer is capable of achieving fractional bandwidth (FBW) in excess of 100% at the first frequency for all the cases except cases 7 and 8. The FBW for case 7 is 38%, however, it is reduced to only 19% for case 8 at the first frequency. Apparently, the enhanced design flexibility makes it possible to have the realizable design parameters at such

high values of r . But it should be noted that there is a trade-off between the achievable r and the FBW as can be seen from the deteriorating FBW of only 2% at the second frequency, i.e. 20 GHz, in the design case 7. However, this constraint can be circumvented and r of more than 30 can also be achieved if the chosen design frequencies are at the lower RF spectrum (for example, 200 MHz and 6 GHz).

C. CASE STUDIES: IMPEDANCE TRANSFORMER AT VARIOUS IMPEDANCE TRANSFORMATION RATIOS

Now, the effectiveness and design flexibility of the proposed impedance transformer is evaluated for varying k for a fixed r of 4. The r is fixed at 4 to assess the concurrent impedance transformation at two distinct frequencies. Multiple design examples are listed in Table 2 with the calculated design parameters. Again, all the design parameters are realizable for the cases varying from $k = 0.1$ to $k = 20$. The circuit simulation results of the design examples are also depicted in Fig. 4. These results demonstrate the excellent performance of the impedance transformer at all the k . It should be noted that the operational FBW, as per required reflection coefficient (Γ_m), of the proposed impedance transformer reduces at the higher k following the conventional theory (10) [34]. Here, $\Delta f / f_o$ is the FBW and f_o is the first frequency of operation. Again, the enhanced design flexibility enables the impedance transformer to have the realizable design parameters at higher k but, for an FBW of 3%, impedance transformer is operable for k varying from as low as 0.1 to as high as 20. However, employing any bandwidth enhancement technique [36]–[38] will further enhance the range of achievable impedance transformation and frequency ratios. It is also practically evaluated that the different combinations of the open-/short-circuited stubs in the proposed design have the potential to improve the bandwidth of the proposed design.

$$\frac{\Delta f}{f_o} = 2 - \frac{4}{\pi} \cos^{-1} \left[\frac{\Gamma_m}{\sqrt{1 - \Gamma_m^2}} \frac{2\sqrt{Z_S Z_L}}{|Z_L - Z_S|} \right] \quad (10)$$

TABLE 2. Design examples with variation in k ($r = 4$, $f_1 = 1\text{GHz}$ is fixed for all cases) [Var*: Design parameters, S: short-circuited, O: open-circuited].

Var*	k=0.05 case 9	k=0.1 case 10	k=0.5 case 11	k=5 case 12	k=10 case 13	k=15 case 14	k=20 case 15
$Z_a(\Omega)$	154.9	84.9	120.5	94.2	93.7	98.7	97.2
$\theta_a(^{\circ})$	144(O)	108(O)	36(O)	36(O)	108(S)	108(S)	108(S)
$Z_e(\Omega)$	20	27	52	120	156	150	141.5
$Z_o(\Omega)$	19	25.3	31	87	80	85	85.5
$\theta_c(^{\circ})$	108	72	36	36	36	36	36
$Z_b(\Omega)$	46.1	62.6	68.9	38.3	62.5	46.3	36.6
$\theta_b(^{\circ})$	72(O)	108(O)	36(O)	36(O)	216(S)	216(S)	216(S)

D. CASE STUDIES: COMPLEX IMPEDANCE TRANSFORMATION

Furthermore, the capability of the proposed impedance transformer for the complex loads is also tested at the two operating frequencies simultaneously. Table 3. A design example

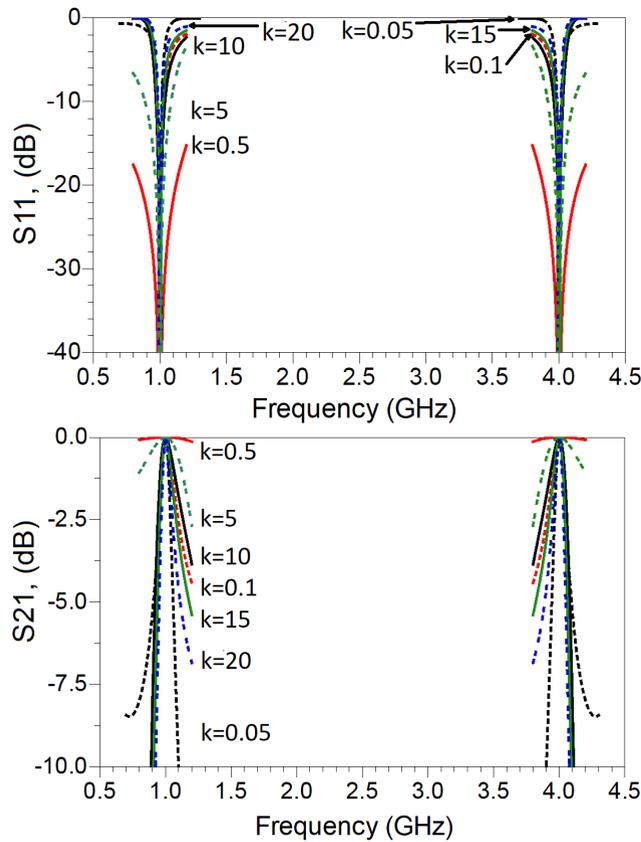


FIGURE 4. Simulation performance of the design examples of Table 2.

TABLE 3. Arbitrary design examples [*Calculated as the ratio of real parts of the port impedances, S: short-circuited, O: open-circuited].

Design Parameters	r=4; k=5* case 16	r=5; k=8.04 case 17	r=15, k=20 case 18
$Z_L(\Omega)$	$150+j*20$	402	1000
$Z_S(\Omega)$	$150+j*20$	50	50
f_1 (GHz)	1	0.8	0.3
f_2 (GHz)	4	4.0	4.5
$Z_a(\Omega)$	149.8	106.1	89.8
$\theta_a(^{\circ})$	288(S)	30(O)	22.5(O)
$Z_e, Z_o(\Omega)$	78, 45	126, 71	105, 70
$\theta_e(^{\circ})$	36	30	33.75
$Z_b(\Omega)$	77.7	66.7	97.4
$\theta_b(^{\circ})$	36(S)	120(O)	11.25(S)

is evaluated working at a high r of 4 and a widely separated complex port impedance of $150 + j*20 \Omega$ at the load. The design example with design parameters is provided in case 16 in Table 3.

The design cases 17 and 18 are also listed to demonstrate the design flexibility at concurrent very high design specifications, i.e., $r, k = 5, 8.04$ and $r, k = 15, 20$, respectively. So many design examples with arbitrarily high design specifications, as per authors' knowledge, are very rare in the reported literature. For example, a dual-band stepped impedance transformer [12] provides very high r and k , but working at higher k and r simultaneously brings inherent fabrication challenges in this design. Designing of this

well-known stepped impedance transformer for the design specifications of $r = 4$, source impedance 50Ω , and load impedance 500Ω (i.e. $k = 10$) results in characteristics impedances of 119.6Ω and 209.1Ω for the TLs in this design. However, the calculated characteristics impedance of 209.1Ω is practically not realizable in microstrip technology. On the other hand, for the proposed impedance transformer at the same $k = 10$, the characteristics impedances are within the realizable range of the microstrip technology i.e. within $[20 \Omega, 150 \Omega]$ for a very high r as can be seen in case 13 in Table 2. All the design parameters listed in Tables 1, 2, and 3 for the three cases are within the microstrip TL realizable limits.

IV. FABRICATION AND MEASUREMENT OF THE PROPOSED IMPEDANCE TRANSFORMER

To validate the working of the proposed impedance transformer, two different prototypes working at very high design specifications, i.e. cases 17 and 18, are fabricated. The first prototype, i.e. case 17, working at 0.8 and 4.0 GHz (i.e. $r = 5$) is fabricated on Rogers RO5880 substrate with a substrate thickness of 1.57 mm, ϵ_r of 2.2, loss tangent of 0.0009, and copper cladding of $35 \mu\text{m}$ on both sides of the substrate. The source and load impedances of the impedance transformer are kept 50Ω and 402Ω (i.e. $k = 8.04$), respectively. The design parameters of the impedance transformer are calculated and provided in Table 3. The load of the impedance transformer is a 402Ω resistor CRCW0603402RFKEA which is shorted to ground through a via on the printed circuited board (PCB) and a 50Ω SMA connector is soldered at the source. The size of the fabricated prototype is $0.018 \lambda_g^2$. The second prototype, i.e. case 18 for demonstration of extreme r and k , is specified to operate at 0.3 and 4.5 GHz (i.e. $r = 15$) and is fabricated on Rogers RO4350B substrate with a substrate thickness of 1.524 mm, ϵ_r of 3.66, loss tangent of 0.0037, and copper cladding of $35 \mu\text{m}$ on both sides of the substrate. The source and load impedances are chosen to be 50Ω and 1000Ω (i.e. $k = 20$), respectively. The design parameters of the impedance transformer are calculated and provided in Table 3. The load of the impedance transformer is a 1000Ω resistor CRCW04021K00FKED shorted to ground through a via on the printed circuited board (PCB) whereas SMA connector mimics the 50Ω source impedance. The size of the fabricated second prototype is $0.0026 \lambda_g^2$.

These prototypes for cases 17 and 18 are depicted in Figs. 5 and 7, respectively. The corresponding measurement and EM simulated results are depicted in Figs. 6 and 8. An excellent agreement between the simulation and the measurement results validate the proposed design along with the design process. Apparently, the measured return losses (S_{11}) of -20.5 dB at 0.8 GHz (-26.3 dB at 0.292 GHz) and -18.5 dB at 4.0 GHz (-23.5 dB at 4.468 GHz) for the first (second) prototype demonstrate extremely good performances at the chosen frequencies for the respective designs. The unwanted resonance frequencies may be observed in Fig. 8 due to the multifold electrical lengths

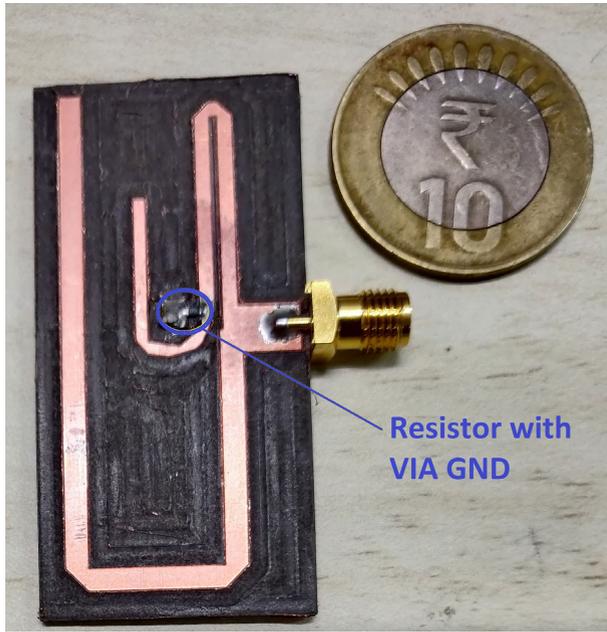


FIGURE 5. Fabricated prototype of the impedance transformer with $r = 5$ and $k = 8.04$.

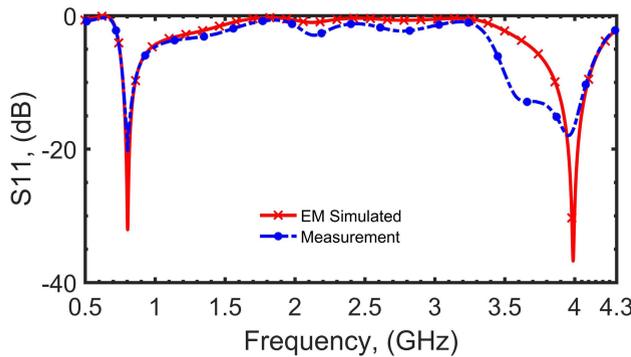


FIGURE 6. Measurement results of the fabricated prototype for $r = 5$ and $k = 8.04$.

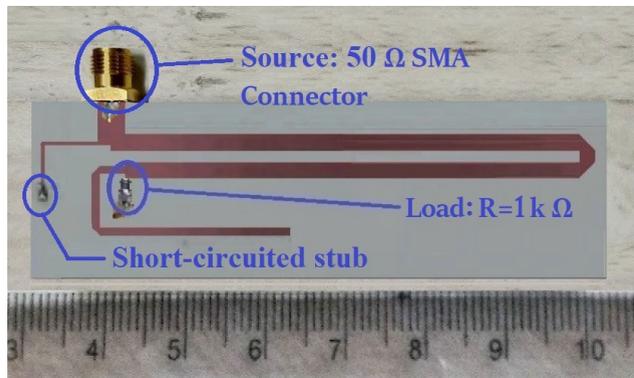


FIGURE 7. Fabricated prototype of the impedance transformer with $r = 15$ and $k = 20$.

(i.e., $n \geq 1$) and can be easily filtered by the existing frequency selective multiband systems. It is imperative to note that any design example in Tables 1, 2, and 3 or any other

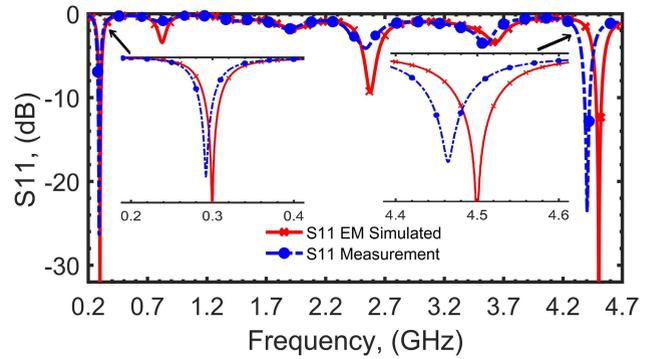


FIGURE 8. Measurement results of the fabricated prototype for $r = 15$ and $k = 20$.

example conforming to extreme cases can be prototyped for validation of the presented concept, but here, the selected example for prototyping is regulated by the available lab resources. However, the proposed circuit is discussed within the scope of microstrip technology and can achieve the highest operable frequencies with some precautions [39].

Table 4 compares the features of the proposed impedance transformer with the recently reported highly featured architectures. Despite utilizing the planar TL, coupled-lines, and stubs combinations by most of the recently published reports [13], [15]–[18], it is apparent that the proposed design has extended the range of realizable design specifications significantly. Several modifications in the architectures are reported to achieve very high k [14], [15], [19] and very high r [13], [14]. However, achieving the concurrent high k and r have been rare in the reported literature. Though the load

TABLE 4. Comparison with state-of-the-art impedance transformers capable of high k and r [*Calculated as the ratio of real parts of the port impedances, **Calculated as the ratio of the maximum to minimum operating frequency].

Ref	Technology	Max. r of examples	Max. k of examples	Specifications of the fabricated prototype (f_2 GHz/ f_1 GHz, k)
This Work	Coupled line with stubs	20	20	(4.5/0.3, 20) , (4.0/0.8, 8.04)
[12]	Two Section Stepped TL	7	20	Not Provided
[13]	Coupled-lines	3.88	4	(2.4/0.9, 2)
[14]	Dual-Transmission Line	5.2	10	(2.8, 10), (5.2/1.0, 10)
[15]	Planar TL with stubs	1.5	5*	(3.6/2.4, 5*)
[16]	Planar TL with stubs	1.66	1.35*	(1.5/0.9, 1.35*)
[17]	Planar TL with stubs	1.94	4	(2.1/0.9, 2.02*)
[18]	Coupled-line with ladder network	1.5**	9.13*	(3.0/2.0**, 9.13*)
[19]	T-Type network with load healing	2.5	5*	(2.0/1.0, 1.86*)
[40]	Planar TL with a coupled-line	2.5	15.36*	(2.61/1.45, 15.36*)

healing concept presented in [19] can enhance the range of k to some extent, but it was able to achieve only marginal improvement. The proposed circuit not only enhances the k and r individually but also leads to significantly enhanced concurrent k and r are also made possible. A design example of concurrent r, k of 15, 20 is fabricated, depicted in Fig. 7 and the measurement results are demonstrated to validate the design flexibility of the proposed impedance transformer. Moreover, all the design cases given in Tables 1, 2, and 3 demonstrate that the proposed impedance transformer is capable of providing a) real and complex impedance transformations, b) very high k , c) very high r , and, d) very high k and r concurrently in comparison to the recently reported impedance transformers in Table 4. It is, therefore, safe to convey that the proposed impedance transformer has the ability to achieve the highest k and r reported so far and thus enhances the existing state-of-the-art significantly.

V. APPLICATION OF THE PROPOSED IMPEDANCE TRANSFORMER IN AN IMPEDANCE TRANSFORMING BALUN

The ultrahigh k and r capability of the proposed impedance transformer make it suitable for its use in RF/Microwave components like power divider, balun, filter, coupler, etc [41]. This can effectively aid to miniaturize the overall size of the RF/Microwave system. For example, three impedance transformers are used in a receiver module as shown in fig. 9. By utilizing the proposed impedance transformer in a balun design makes it capable of providing the required impedance transformation inherently at the source and load. Therefore, a single inherent impedance transforming balun can replace all the components inside the red box in Fig. 9.

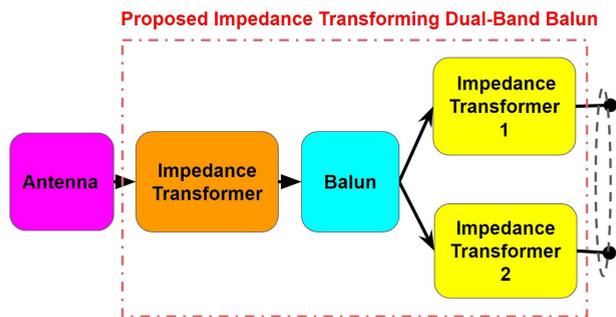


FIGURE 9. Block diagram of conventional receiver side antenna module.

A. DESIGN OF DUAL-BAND BALUN INCORPORATING THE PROPOSED IMPEDANCE TRANSFORMER

To verify the presented theory, a novel dual-band balun architecture is designed utilizing the proposed dual-band impedance transformer and is shown in Fig. 10. The source (input port) and the load (output ports) impedances of the balun architecture are $Z_S \Omega$ and $Z_L \Omega$ respectively. Here, all the electrical lengths are denoted by θ_i where $i = x, 1, 2, 3, 4$.

Apparently, the balun is a symmetric architecture [42] and therefore, can be analyzed using simplified even-odd mode analysis. The equivalent odd-mode circuit, shown in Fig. 11, reveals that the balun is utilizing the proposed impedance transformer for the required impedance transformation in the odd-mode.

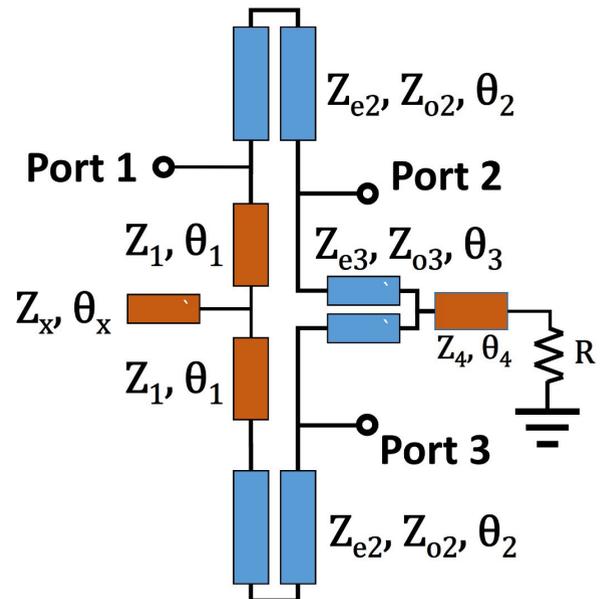


FIGURE 10. A dual-band impedance transforming balun architecture.

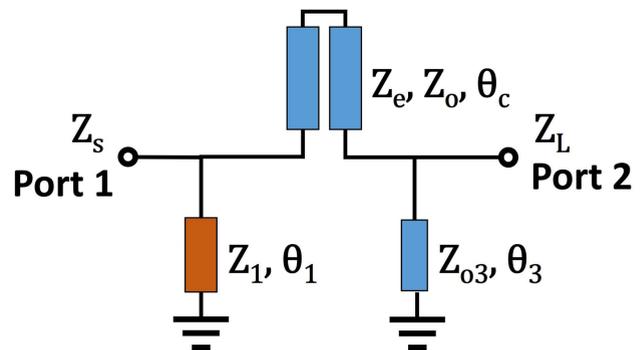


FIGURE 11. Odd-mode equivalent circuit of the proposed balun (the proposed impedance transformer).

The balun operates successfully if the conditions in (11) are met [43]. In addition, electrical lengths for dual-band designs are regulated by expression (12). Here, the term Z_{odd} is the odd-mode impedance at the input port, T_{even} is the transmission coefficient of signal in the even-mode, and n is an integer.

$$Z_{odd} = 2Z_S \quad \text{and} \quad T_{even} = 0 \tag{11}$$

$$\theta = \frac{(1+n)\pi}{1+r} \tag{12}$$

B. BALUN IMPLEMENTATION AND MEASUREMENT

To evaluate the effectiveness of the proposed design at high k and at high r , a design example with $k = 8$ at $r = 2$, is fabricated on RO5880 substrate with a thickness of 1.57 mm, ϵ_r of 2.2, loss tangent of 0.0009, and copper cladding of $35 \mu\text{m}$ on both sides of the substrate. The source and load impedances are chosen as $Z_S = 50 \Omega$; $Z_L = 400 \Omega$ working at arbitrary frequencies of $f_1 = 1 \text{ GHz}$ and $f_2 = 2 \text{ GHz}$. The design parameters for the example are mentioned in Table 5. Appropriate optimizations in the layout design are accounted for the non-idealities and discontinuities associated with TL. The prototype with the marked dimensions is depicted in Fig. 12. The prototype in fig. 12 includes two additional (redundant) impedance transformers at the output ports, inside the red box, to create 50Ω environment for measurement purposes. The intended prototype is smaller without these redundant impedance transformers.

TABLE 5. Balun implementation examples.

Design Parameters	Design Example with $k = 8$, $r = 2$
$Z_1 (\Omega), \theta_1 (^\circ)$	31.9, 60
$Z_X (\Omega), \theta_X (^\circ)$	47.9, 60
$Z_{e2} (\Omega), Z_{o2} (\Omega), \theta_2 (^\circ)$	140, 110, 60
$Z_{e3} (\Omega), Z_{o3} (\Omega), \theta_3 (^\circ)$	168.6, 80.3, 60
$Z_4 (\Omega), \theta_4 (^\circ)$	29.7, 60
$R (\Omega)$	39

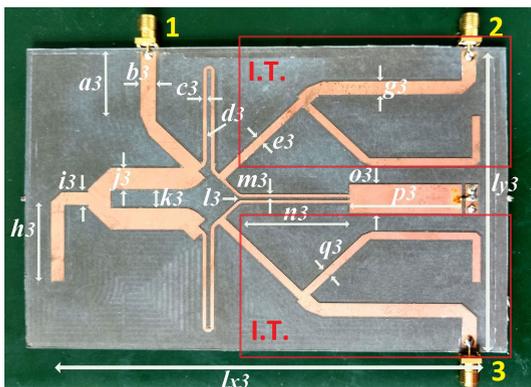


FIGURE 12. Fabricated balun prototype for $r = 2$ and $k = 8$. [$a_3 = 21.25$, $b_3 = 4.77$, $c_3 = 1.14$, $d_3 = 1.28$, $e_3 = 2.46$, $g_3 = 4.36$, $h_3 = 25.60$, $i_3 = 163.94$, $j_3 = 7.13$, $k_3 = 6.47$, $l_3 = 1.02$, $m_3 = 0.86$, $n_3 = 33.12$, $o_3 = 9.53$, $p_3 = 34.24$, $q_3 = 2.42$, $l_3 = 98.05$, $l_3 = 133.35$ (all in mm)] (includes two redundant impedance transformers (I.T.) in red boxes).

The measured and EM simulated performances are compared and depicted in Fig. 13. Apparently, return loss better than -21 dB at both the design frequencies demonstrates good matching at all the ports. The 10dB matching bandwidths in this case are better than 130 MHz @ 1 GHz and 2 GHz. Measured S_{21} is -3.5 dB @ f_1 and -3.8 dB @ f_2 whereas measured S_{31} is -3.3 dB @ f_1 / -3.8 dB @ f_2 in Fig. 13 (top) indicates good performance of this design. Furthermore, a high S_{22} of -26 dB is achieved at both the design frequencies as shown in Fig. 13 (middle). Finally, very

good phase relationship can be observed in both the simulated and measured results as depicted in Fig. 13 (bottom).

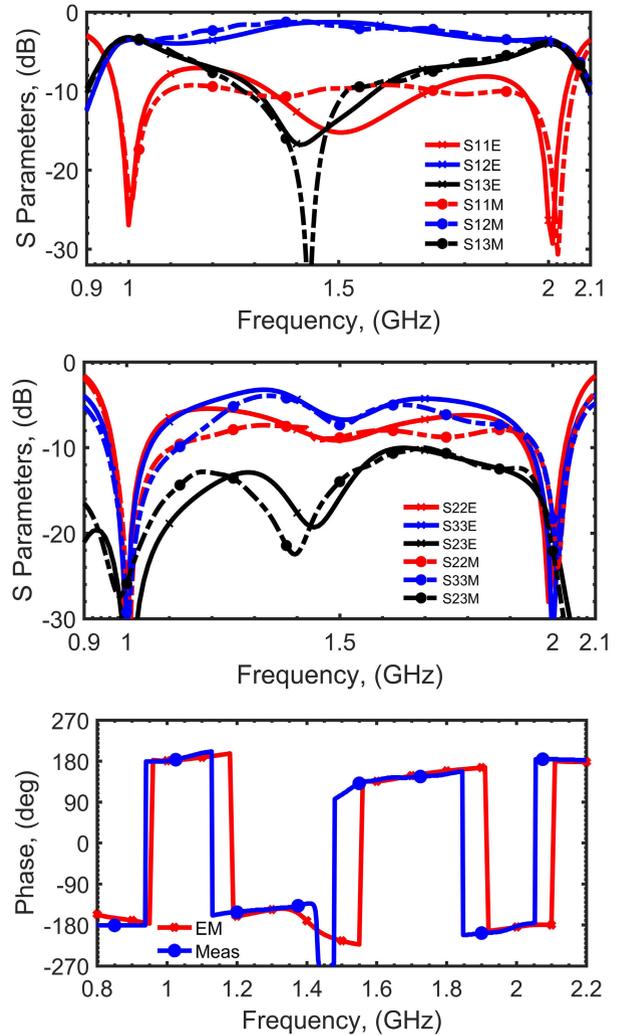


FIGURE 13. EM simulated vs measurement results for $r = 2$ and $k = 8$, Top: input return loss and insertion loss, Middle: output return losses and isolation, Bottom: phase difference; E: EM simulation results and M: measurement results.

VI. CONCLUSION

An analytical methodology of designing a dual-band high impedance transformer is proposed in this paper. The proposed architecture, with high design flexibility, has three main advantages: 1) the design is realizable for the real and complex loads, 2) the design is realizable at a very high k , 3) the design is realizable at a very high r , and 4) the design is realizable at very high k and r simultaneously. To facilitate the quick prototyping, the design analysis is augmented with a systematic design procedure. Two prototypes working at concurrent (r, k) of $(5, 8.04)$ and $(15, 20)$ are fabricated and the measurement results validate the proposed circuit at very high design specifications. The application of the proposed impedance transformer is also demonstrated using

an impedance transforming dual-band balun architecture and its measurement results.

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