FABRICATION AND INTEGRATION OF ONE- AND TWO-DIMENSIONAL MATERIALS FOR ADVANCED NANOSCALE DEVICES

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Abstract

As the miniaturization of electronic circuits reach physical limits, new materials and physical phenomenon need to be exploited to further increase device density and efficiency. A number of approaches have been proposed. One of the common approaches in the scientific community is the search to understand and practically fabricate novel materials and devices at the nanoscale. In this work, we present several nanofabrication processes and unique synthetic methods that we have developed to achieve novel 1D and 2D semiconducting, dielectric, and ferroelectric materials, relevant for the integration in advanced nanoscale devices.

In particular, **single-walled carbon nanotubes** (CNTs) were synthesized and integrated into bottom- and top-gate field effect transistors. We demonstrated a novel CNT surface pretreatment method that enables uniform and conformal ALD coating of suspended nanotubes with various dielectric materials. Obtained all-oxide TiO_2-Al_2O_3 compound high-κ dielectric showed an improved dielectric permittivity.

Another class of semiconductor that we investigated, was **transition metal dichalcogenide** (TMD) layered thin film materials. We developed a novel synthetic method that we termed "lateral conversion," which was used to grow WS_2, WSe_2, MoS_2 and $MoSe_2$ van der Waals materials. In this method, a metal-oxide layer is converted into TMD material using a chalcogenation reaction that propagates laterally between two inert silica layers. The method results in a multilayer structure with TMD material covered by a capping layer that protects it from the environment, contamination, and oxidation. It was shown that the technique provides control over the TMD position, shape, and thickness with sub-micron precision, at wafer scale.

A third class of materials that was studied in this work are **hafnia-based ferroelectric thin films**. The ability to integrate ferroelectric thin films into

electronic devices with atomic layer deposition (ALD) has been a long-standing dream. With the discovery of ferroelectric properties in ALD hafnium oxide, the realization of some advanced architecture devices became one step closer. Here, ALD was used to synthesize $Hf_{0.5}Zr_{0.5}O_2$, with precisely tuned stoichiometry. Next, the crystallization of initially amorphous $Hf_{0.5}Zr_{0.5}O_2$ was performed using widely researched rapid thermal annealing (RTA), as well as by using intense pulsed ion beams (IPIBs), which was done for the first time for such application. RTA-produced ferroelectric thin films, showed successful orthorhombic phase stabilization and annealing-temperature-dependent remnant polarization, whereas early IPIBs experiments demonstrated the ability to crystallize HfO_2, ZrO_2 and $Hf_{0.5}Zr_{0.5}O_2$ thin films, inducing different crystallographic phases.

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Declaration

I declare that the research contained in this thesis, unless otherwise formally indicated within the text, is the original work of the author. The thesis has not been previously submitted to this or any other university for a degree and does not incorporate any material already submitted for a degree.

Aidar Kemelbay
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Contents

List of Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BOE	Buffered Oxide Etch
CMOS	Complementary Metal-Oxide-Semiconductor
CNFET	Carbon Nanotube Field Effect Transistor
CNT	Carbon Nanotube
CPD	Critical Point Drying
CVD	Chemical Vapor Deposition
ELC	Extent of Lateral Conversion
EOT	Equivalent Oxide Thickness
FET	Field Effect Transistor
FIB	Focused Ion Beam
GAA	Gate-All-Around
GIXRD	Grazing Incidence X-Ray Diffraction
HRTEM	High Resolution Transmission Electron Microscopy
HZO	Hafnium-Zirconium Oxide
IC	Integrated Circuit
IPIB	Intense Pulsed Ion Beam
ITRS	International Technology Roadmap for Semiconductors
MFM	Metal-Ferroelectric-Metal
MIM	Metal-Insulator-Metal
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal Oxide Field Effect Transistor
NA	Numerical Aperture

NC	Negative Capacitance
O-Phase	Orthorhombic Phase
PEALD	Plasma Enhanced Atomic Layer Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
RPM	Revolutions Per Minute
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
SS	Subthreshold Swing
SWCNT	Single-Walled Carbon Nanotube
TEM	Transmission Electron Microscopy
TMD	Transition Metal Dichalcogenide
WLRM	White Light Reflection Microscopy
XPS	X-Ray Photoemission Spectroscopy
XRD	X-Ray Diffraction
XRR	X-Ray Reflectivity

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Nomenclature

ε	Dielectric permittivity
κ	Dielectric constant
μ_{FE}	Field effect mobility
ψ_s	Surface potential
ρ	Electrical resistivity
C	Capacitance
E_c	Coercive field
I_g	Gate leakage current
I_{sd}	Source-drain current
J	Beam current density
P	Power
P_r	Remnant polarization
V_g	Gate voltage
V_{sd}	Source-drain voltage

1. Introduction

Electronic devices have revolutionized modern society. They have had enormous impact on industry, manufacturing, information technology, healthcare, and more – pretty much every aspect our lives. We regularly carry smart phones in our pockets that would have been considered super-computers and filled a room only a few decades ago. In 1959, the invention of the metal-oxide semiconductor field effect transistor (MOSFET), and particularly later invention of the silicon-based transistor, launched a period of rapid growth in the field of electronics, with ever-increasing demands and expectations [1]. The semiconductor industry has been driven to continue delivering more and more complex and sophisticated devices by increasing the density of integrated circuits (ICs), while simultaneously decreasing their size, starting the miniaturization race. The challenges and achievements, associated with this race, can be understood by looking at two predictions that were made in 1960s-70s – Moore's Law and Dennard scaling, which were later followed by the semiconductor industry. The former predicted that the number of transistors in integrated circuits would double every two years, whereas the latter predicted even more ambitious developments. In addition to doubling the density, circuits would become 40% faster, while the power consumption would stay constant. Currently, the state-of-the-art has been able to keep pace with the Moore's Law, though it appears to be reaching fundamental limits within the current silicon paradigm. On the other hand, Dennard scaling has not been keeping pace since around 2006. In order to overcome existing obstacles and continue the scaling of transistors, while improving their performance and decreasing power consumption, novel materials and novel device architectures beyond silicon technology need to be developed. A group of experts from the semiconductors industry have reviewed possible solutions in the International Technology Roadmap for Semiconductors (ITRS), which include spin FETs, negative capacitance field effect transistors (FETs), nanoelectromechanical switches and all-spin logic devices [2]. The roadmap, among materials for the next generation electronic devices, lists carbon nanotubes,

various nanowires, III-Vs, and other materials.

The research presented here, investigates the synthesis of novel materials for next generation electronics, which includes fabrication of one- and two-dimensional semiconductors, advanced thin film high-κ dielectrics, and thin film ferroelectrics. Novel low-dimensional semiconductors possess unique physical properties, such as ballistic conduction, high charge carrier mobility and absence of short-channel effects, making them perfectly suitable for further aggressive device miniaturization. Together with high-κ dielectrics and ferroelectrics, it becomes possible to elucidate novel phenomena, like negative capacitance, integration of which will further contribute to future electronics size and power-supply down-scaling.

Specifically, this work focuses on three materials: single-walled carbon nanotubes, transition metal dichalcogenides, and ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. The synthesis and engineering of these materials contribute towards a common goal – the development of negative capacitance transistors and other advanced nanoscale devices.

Carbon nanotubes. We developed process flows for the synthesis of single-walled carbon nanotube (CNT) transistors, including a novel technique for atomic layer deposition (ALD) of oxides on the inert surface of defect-free nanotubes. The latter is important since ALD typically does not form continuous layers on the nanotube surfaces that are free of nucleation sites. The proposed method utilizes TiO_2-based pretreatment of CNTs, which results in nanotubes coated with a weakly interacting, continuous layer of titania. The pretreatment strategy enables subsequent ALD of high-κ dielectric, does not degrade the nanotube properties (that is typically expected from the surface functionalization), and increases the dielectric permittivity of the all-oxide insulator. We believe that this technique can be extended to coat CNTs with other ALD materials, such as metals, nitrides and sulfides.

Transition metal dichalcogenides. A novel transition metal dichalcogenide (TMD) synthesis method that we call "lateral conversion" was developed, which forms a structure with TMD material sandwiched between two silica layers. The technique is based on the chalcogenation of metal-oxide fims, and proceeds laterally between two inert layers forming 2D TMDs. The capping layer makes subsequent TMDs processing contamination-free, while it can also serve as a buffer layer for subsequent deposition of ALD thin films. ALD on pristine TMDs, similar to ALD on CNTs, is challenging due to the absence of nucleation sites on their surface; the developed technique overcomes this problem. The lateral conversion method utilizes standard lithographic approaches,

and enables wafer-scale synthesis of TMDs with few-layer precision, and complex lithographically defined features.

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. We fabricated ferroelectric thin films of $Hf_{0.5}Zr_{0.5}O_2$ (HZO), towards their future integration with CNTs and TMDs into negative capacitance transistors. As-synthesized HZO had an amorphous structure, so to induce the ferroelectricity, it was crystallized using two approaches: (1) conventional high-temperature annealing; and (2) a novel technique based on irradiation with intense pulsed ion beams. The former approach produced crystalline ferroelectric thin films. The latter allowed the crystallization of amorphous hafnia with an ultra-low thermal budget. We show that ion beams can controllably induce different crystallographic phases and is a promising method for producing ferroelectric HZO; ferroelectric measurements will be performed in future research.

Dissertation contents. Chapter 2 starts with a brief historical review of the state-of-the-art in the field of nanoscale metal-oxide-semiconductor (MOS) transistors, discussing their limitations and stating what needs to be done to overcome existing obstacles. Subsequent sections review some of the possibilities from two perspectives: changes that need to be made in device materials, and device architectures. CNTs and TMDs are discussed in the context of novel device materials, and their properties are reviewed. Next, ferroelectricity and the negative capacitance phenomena are introduced. Chapters 3 to 5 report the experimental details of three projects and the obtained results. Chapter 3 describes our fabrication of carbon nanotube transistors and a pretreatment process developed to uniformly cover the nanotube surface with high-κ dielectric. Chapter 4 presents the lateral conversion technique used to synthesis transition metal dichalcogenides. In chapter 5, the ALD synthesis and characterization of $Hf_{0.5}Zr_{0.5}O_2$ are discussed. Chapter 6 summarizes the obtained results and sets goals for future research.

2. State-of-the-art

This chapter discusses an operation principle of field effect transistors, performance requirements recognized by academia and industry, as well as future directions for transistor development.

2.1. Conventional FETs and scaling theory

Metal Oxide Field Effect Transistors (MOSFETs) were first developed in 1959 at Bell Labs by Martin Atalla and Dawon Kahng [1]. The first device was based on crystalline silicon capped with thermally grown silicon oxide. Since then, the MOSFET geometry, materials, and processes to synthesize them has significantly evolved, but the operating principle, in general, remains the same. A conventional FET consists of two highly doped regions called the source and drain connected by an oppositely and moderately doped semiconductor, which is the transistor channel (see figure 2.1). A third electrode, called the gate, is formed on top or under the channel and electrically separated from it using an insulating material. When no gate voltage is applied, the transistor can be represented as two p-n junctions connected back to back, and only leakage current can flow. If a gate voltage is applied, the semiconducting channel underneath is inverted, forming an inversion channel, which connects two highly doped regions. If source-to-drain voltage V_{sd} is applied, current starts flowing through the inversion channel and can be precisely modulated by changing the conductivity of the channel by applying an electric field from the gate terminal. For devices with such geometry, being able to fabricate transistors with perfect interfaces between components, ensuring good electrostatic coupling between gate and semiconducting channel, was a major obstacle. Silicon came to the rescue, due to the ability to grow oxide layers with perfect interfaces on the initial silicon substrate. The integration of thermally grown oxide lead to a reduction in the amount of surface states that screen applied electric field and deteriorates MOSFET performance. Moreover, Si can be controllably doped with

different chemical elements that can be use to obtain all major transistor components out of a single material.

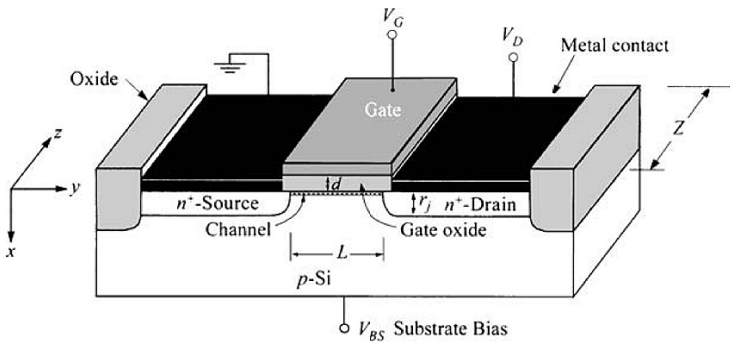


Figure 2.1. Schematic illustration of MOSFET [3].

Increasing computation complexity required more transistors to be integrated in one device. In 1960, the first IC consisting of 16 transistors was demonstrated. Since then, both industry and scientific community have invested enormous efforts to increase the density of ICs. In 1965, Gordon Moore, at the time a R&D director at Fairchild Semiconductor, predicted that the number of components in ICs would double every two years, which is today known as "Moore's Law". Ever-growing demand from electronics required aggressive downscaling of individual transistors in order to accommodate as many devices on as small a substrate as possible. In addition to the size scaling, it was (and still is) required to further improve transistor performance, while reducing its power consumption. In 1974 Robert H. Dennard formulated a goal, according to which – with each generation, transistor density should increase twice, and ICs should become 40% faster, while the power density (and power consumption) should stay constant [4]. Since then, Moore's Law and Dennard scaling have been used to guide the industry and set the targets. Currently, Moore's law is pushing towards its limits, and Dennard scaling was abandoned around 2006. Smaller transistors, more dense architectures, difficulties with reducing operating voltage, and higher clock speeds, have resulted in heating and short-channel effects, leakage current problems, as well as increased power consumption. As a result, new materials, new device architectures and new approaches beyond conventional MOSFET technology need to be developed for further electronics miniaturization and performance improvements. Some of the ideas, proposed toward realization of this goal, will be discussed in the next section.

2.2. Novel low power switches

The power required for transistor operation is mostly composed of dynamic and static power. Dynamic power, required to switch a MOSFET, is proportional to the operating voltage and has the following dependence [5]:

$$P_{dynamic} = V_{sd}^2 \times I_{av}, \tag{2.1}$$

where V_{sd} and I_{av} are source-to-drain voltage and average current, respectively. Static power or leakage power can be calculated as follows:

$$P_{static} = V_{sd} \times I_{off}, \tag{2.2}$$

where I_{off} is the off-state leakage current. Both equations constitute total power required for transistor operation and point to the conclusion that lowering operating voltage V_{sd} will lead to the reduction of total power consumption of the device.

The current flowing through the FET channel is proportional to:

$$I_{sd} \propto exp(qV_g/k_BT), \tag{2.3}$$

where k_B is the Boltzmann constant and T is the operation temperature [3]. The change in I_{sd}, in subthreshold region, as a function of applied gate voltage V_g is called subthreshold swing (SS) and defined as:

$$SS = \frac{\partial V_g}{\partial (logI_d)}, \tag{2.4}$$

By combining equations 2.3 and 2.4, one can calculate that at room temperature the physical limit of SS is 60 mV/dec, which means that at least 60 mV needs to be applied to increase the current ten times. Such limitation also imposes a lower limit on V_{sd} and as a result the power consumption of an individual transistor.

To further investigate SS, one can extend equation 2.4 to:

$$SS = \frac{\partial V_g}{\partial (logI_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_s}}_{\text{m}} \underbrace{\frac{\partial \psi_s}{\partial (logI_d)}}_{\text{n}} = \underbrace{(1 + \frac{C_s}{C_{ins}})}_{\text{m}} \underbrace{\frac{kT}{q} ln10}_{\text{n}}, \tag{2.5}$$

where ψ_s is a surface potential, C_s and C_{ins} are semiconductor and insulator

capacitances, respectively. Term m is called the body factor and represents coupling between the gate and channel, whereas n governs the conduction or injection mechanism of carriers into the channel. To lower SS value, m and n should be as small as possible. Below each case will be briefly discussed and different approaches will be studied that can be taken to achieve sub-60 mV/dec operation regime.

Tunnel FET. One type of device that satisfies the $n < 1$ requirement is tunnel FET (TFET). These devices have similar structures to conventional MOSFETs, but the conduction is based on carrier tunneling. In MOSFETs, the source-drain current is modulated by changing the conductivity of semiconducting channel, whereas in TFETs, it is based on quantum tunneling of charge carriers from valence to conduction band and vice versa. One of the early experiments demonstrated this effect in Schottky barrier carbon nanotube field effect transistors (CNFETs) [6], where band-to-band tunneling was achieved by using a dual-gate configuration. One of the gate electrodes was used to electrostatically dope a nanotube and another one was used to apply a local electric field to shift the conduction and valence bands of the nanotube. Once the conduction band bendt bellow the valence band, the band-to-band tunneling could facilitate the tunneling current, increasing I_{sd}. This approach allowed the reduction of SS to a value as low as 40 mV/dec. However, despite delivering good switching behavior, one of the main drawbacks of TFETs is low ON current, since the amount of charge carriers is limited by the tunneling effect, which is impractical for many applications.

Impact ionization MOS. Another type of transistor, which overcomes FET limitations, is an impact ionization MOS (I-MOS) device. A typical I-MOS structure consists of $p+$ and $n+$ regions (serving as source and drain respectively) that are connected by the intrinsic region. By applying a gate voltage through the gate electrode – partially overlapping intrinsic region, it is possible to control the formed inversion layer, which can reduce the effective channel length of the transistor. When high enough V_g is applied, V_{sd} starts to contribute to the electric field and increases the horizontal electric field outside the gate. At some point, the increasing vertical electrical field from V_g and the growing horizontal electric field from V_{sd} result in an avalanche breakdown, switching the device from the OFF to ON state, allowing charge carriers to surge into the channel, resulting in rapid I_{sd} growth with a very steep sub-60 mV/dec slope [7]. However, due to the close proximity of hot electrons to the oxide layer, reliability of such devices is challenging, since these electrons can be trapped, shifting the threshold voltage of

the transistor [8]. In addition, impact ionization transistors typically require high operating voltages, which negatively impact power consumption, even though the transport characteristics have a very steep slope.

Gate coupling improvement. Both TFET and I-MOS devices can improve the n term in equation 2.5, and have their own advantages and drawbacks. However, they represent a class of devices that are different from conventional MOSFETs that are predominantly used in the semiconductor industry. Many fabrication processes have been developed and studied in detail for MOSFETs by the industry and academia. So, in this work we discuss how to improve the MOSFET performance without suggesting to replace them. As a figure of merit, the *SS* will be mostly used in this work, with the aim to make it as small as possible. As previously discussed, the *SS* can be mathematically described with two terms - m and n (see equation 2.5). For MOSFETs the thermal factor $n = (kT/q) \times ln10$ is limited to 60 mV/dec (at room temperature), so to reduce the *SS*, the body factor m needs to be decreased. The body factor represents how good the electrostatic coupling between gate electrode and semiconducting channel in the FET is established. For m to be less than 1 (which will result in $SS < 60$ mV/dec), C_s/C_{ins} should have a negative value. This implies that either the semiconductor or insulator capacitance should have a negative value. The latter can be achieved if a ferroelectric material is integrated into the gate stack of a MOSFET, since in some circumstances ferroelectric differential capacitance can become negative. This idea was first proposed as an approach to lower *SS* in 2008 by Salahuddin and Data [9]. The authors suggested that this could be accomplished by integrating ferroelectric material into a FET's gate stack. A few years later, sub-60 mV/dec operation was experimentally demonstrated in numerous devices, using various ferroelectrics and channel materials (semiconductors). Briefly, incorporation of a ferroelectric provides internal gate voltage amplification, and a ferroelectric capacitor serves as a step-up voltage transformer [9]. The work we present here is aimed to further develop the negative capacitance transistor approach, by investigating novel materials and their co-integration into devices. A more detailed overview of the negative capacitance phenomena is presented in chapter 2.4.1, whereas the next section will discuss what semiconductors can be used to improve the MOSFET performance.

2.3. 1D and 2D nanomaterials for future electronics

The low-dimensional semiconductors that will be discussed and studied in this work are carbon nanotubes and transition metal dichalcogenides. These materials

have extraordinary mechanical, optical, thermal and chemical properties [10, 11], however, for this work we are primarily interested in utilizing their unique electronic properties in transistor applications. These alone will not significantly reduce the *SS* of FETs, but can help to overcome other problems, especially the short channel effects that start to dominate in conventional Si-based MOSFETs.

2.3.1 Carbon nanotubes

Carbon nanotubes are tubular structures consisting of carbon atoms arranged in a hexagonal structure with carbon-carbon bond length of 1.421 Å. This nanomaterial was first discovered in 1952 by Radushkevich *et al.* but did not receive proper attention until 1991 after publication by Sumlo Iijima, where double-walled and multi-walled CNTs were characterized using transmission electron microscopy [12]. Two years later, single-walled nanotubes were first reported in literature and studied [13]. Ever since, CNTs have been an ongoing subject of intense research due to their exceptional physical and chemical properties. In this work we focus on single-walled nanotubes only, so **CNT will refer to single-walled CNTs**, unless otherwise specified.

Chemical structure. Elemental carbon consists of a nucleus with 6 electrons around it. Two electrons occupy the *1s* orbital, forming the *K* shell and the remaining four electrons occupy the *2s* and *2p* orbitals, forming the *L* shell. In an excited state, each valence electron occupies *2s*, *2px*, *2py* and *2pz* orbitals. The fourth electron excitation arises from energy released during bonding. Further, during molecular interactions, the orbitals mix into hybrid orbitals to form chemical bonds, which is called hybridization. For neighboring C atoms in graphene, one *s* and two *p* orbitals mix, resulting in so-called sp^2 hybridization, oriented in the x-y plane. Such in-plane hybridization of *2s*, $2p_x$ and $2p_y$ orbitals leads to the formation of three σ-bonds, responsible for chemical bonding of C atoms. These bonds define the mechanical properties of graphene that depend on the rigidity of the bond. The remaining unhybridized out-of-plane $2p_z$ orbital is available for π-bonding; it has a small binding energy and governs the electrical properties of graphene. Thus, each carbon atom provides one electron that can be easily excited by thermal energy from valence to conduction band since they overlap. As a result, graphene is a good electrical conductor or quasi-metal.

For carbon nanotubes, which can be viewed as rolled-up graphene sheets, the situation changes significantly. Bending and curvature induction change the C-C

bond length and angle; π-orbitals start to overlap and are no longer perpendicular to σ-orbitals. Depending on the angle used to roll up the graphene sheet, CNT can have different chirality and the nanotubes possess different physical and chemical properties.

Carbon nanotube lattice. Crystal lattices can be built by defining primitive unit cells and translational symmetry [14]. For graphene, the unit cell consists of two carbon atoms, however the crystallographic structure of CNTs is more complex (see figure 2.2). In the circumferential direction, the CNT lattice vector can be represented by a chiral vector:

$$\boldsymbol{C_h} = n\boldsymbol{a_1} + m\boldsymbol{a_2}, \tag{2.6}$$

where *n* and *m* are integers, together called chirality - *(n,m)*; whereas $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are graphene lattice vectors. In the axial direction, the CNT lattice vector is called the translation vector and can be defined as:

$$\boldsymbol{T} = t_1\boldsymbol{a_1} + t_2\boldsymbol{a_2}, \tag{2.7}$$

where t_1 and t_2 are integers. Chiral indices *n* and *m* can be used to distinguish the following types of achiral (i.e. nanotube is superimposable on its own mirror images) CNTs: (1) armchair nanotubes with *(n,m = n)*; and (2) zigzag nanotubes with *(n,m = 0)*. All other *(n,m)* CNTs are chiral. The nanotube diameter can be calculated as:

$$d_t = \frac{|C_h|}{\pi} = \frac{\sqrt{C_h \cdot C_h}}{\pi} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi}. \tag{2.8}$$

Since chiral and translation vectors are orthogonal (i.e. perpendicular to each other), their dot product is $\boldsymbol{C_h} \cdot \boldsymbol{T} = 0$, from which t_1 and t_2 can be derived:

$$\begin{aligned} t_1 &= (2m+n)/p \\ t_2 &= -(2n+m)/p, \end{aligned} \tag{2.9}$$

where *p* is the greatest common divisor of *(2m + n)* and *(2n + m)*. The chiral angle is the angle between the chiral vector and the primitive lattice vector $\boldsymbol{a_1}$:

$$cos\theta = \frac{\boldsymbol{C_h} \cdot \boldsymbol{a_1}}{|\boldsymbol{C_h}||\boldsymbol{a_1}|} = \frac{2n+m}{2\sqrt{n^2 + nm + m^2}}. \tag{2.10}$$

The number of hexagons in one unit cell is calculated using the following equation:

$$N = \frac{|\boldsymbol{C_h} \times \boldsymbol{T}|}{\boldsymbol{a_1} \times \boldsymbol{a_2}} = \frac{2(n^2 + nm + m^2)}{p} = \frac{2|\boldsymbol{C_h}|^2}{a^2 p} \tag{2.11}$$

Electronic properties. The electronic properties of CNTs can be derived by using the so-called zone folding scheme [15]. The first Brillouin zones of CNTs and graphene are one- and two-dimensional, respectively. The energy dispersion of graphene can be used to construct the band structure of CNTs by cutting the two-dimensional electronic dispersion relation of graphene (figure 2.2b). The number of cutting lines is equal to the number of hexagons in the unit cell of a CNT, and their length is inversely proportional to the length of the unit cell, whereas the distance between the cutting lines is inversely proportional to the diameter of CNT.

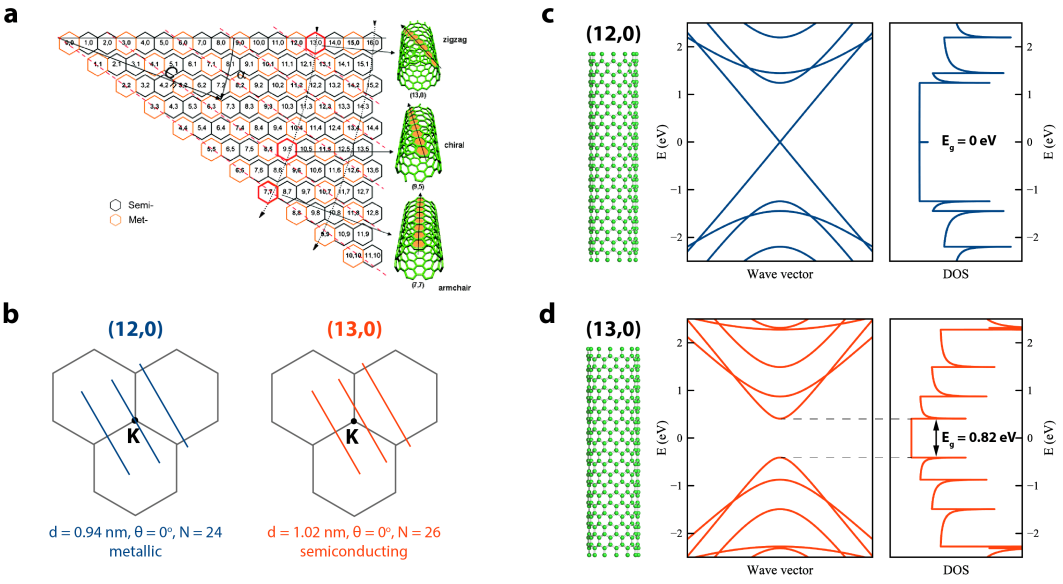


Figure 2.2. Chirality-dependent properties of carbon nanotubes. (a) Carbon nanotube chirality derivation from chiral angle, chiral and translation vectors. Reproduced from [16] with permission from the PCCP Owner Societies. (b) Zone folding scheme used to construct band-structure of CNTs from graphene. (c) Band structure and DOS obtained for two CNTs of different chirality simulated using the "CNTbands" software [17].

Graphene does not have a band gap since the valence and conduction bands of graphene touch each other at the *K* point in the Brillouin zone. If the cutting line, used to obtain the band structure of CNT from graphene, passes through the *K* point, the band gap of such a nanotube will be zero and the nanotube will be metallic. If *(n,m)* does not allow the cutting line to pass through the *K* point, a band gap will be created resulting in a semiconducting nanotube. Figure 2.2b shows cutting lines for

(12,0) and *(13,0)* zigzag nanotubes near graphene's *K* point. Since the chirality of a *(12,0)* tube allows one of the lines to go through the *K* point, the tubes possess metallic properties and the opposite can be observed for semiconducting *(13,0)* tubes. Band structure and density of states (DOS) for both chiralities, as well as their molecular structure are presented in figure 2.2c and d. These results were obtained using "CNTbands" simulator, available at https://nanohub.org/tools/cntbands-ext/, using P_z-orbital model [17].

Synthesis. The general approach to synthesize carbon nanomaterials is (a) via ablation of solid carbon or (b) pyrolysis of a carbon-containing gas such as ethylene or acetylene. As a result of such reactions, carbon atoms may arrange in a specific order to form fullerenes, graphene or carbon nanotubes. A possible undesirable byproduct is amorphous carbon. Since pyrolysis is a thermal decomposition process, typically requiring high processing temperatures at low pressures and good control over the rate that gasses are introduced into the reaction chamber. For carbon nanotubes, three main synthetic approaches based on ablation or pyrolysis exist: (1) arc discharge; (2) laser ablation; and (3) chemical vapor deposition (CVD).

Arc discharge is based on the creation of an electric arc containing carbon atoms, which can be achieved by applying high voltage between two graphite electrodes at high temperatures. Typically, the resulting product is a soot containing fullerenes, nanotubes and amorphous carbon. Next, this mixture needs to be purified to remove unwanted materials and leave CNTs only. **Laser ablation** utilizes a laser to vaporize graphite in a high temperature reactor. The resulting carbon vapor is carried using an inert gas (e.g. Ar) and condenses onto a water-cooled collector placed downstream. The quality and quantity of the material can be controlled by changing the laser power, reactor temperature, pressure, and catalyst nanoparticles. The latter can be used by alloying carbon targets with catalytic metals, such as Ni, Co, and their mixture.

Laser ablation and arc discharge are mostly used to synthesize large quantities of nanotubes, which can be used, for instance, to fabricate randomly oriented nanotube arrays. If additional techniques are employed, such as electrophoresis, horizontally aligned arrays can also be achieved. Both laser ablation and arc discharge require purification and very high reactor temperatures, which makes precise positioning of individual CNTs on a chip a challenging task. In this regard, chemical vapor deposition allows synthesis of nanotubes with much better control over their position on a wafer, and overall improved quality of the material.

Chemical vapor deposition. CVD is based on introducing carbon containing gas, such as CH_4 or C_2H_2, into a preheated reactor. The growth temperature can be greatly reduced by using catalyst nanoparticles in a process called vapor-liquid-solid growth. The process starts from carbon stock decomposition and dissolution into metal nanoparticles. At a specific temperature, carbon has a limited solubility in the metal. Once the metal nanoparticle is supersaturated, the carbon nanotube starts growing by one of two mechanisms. The first one is base growth, where the catalyst nanoparticle stays attached to the substrate and the CNT grows from it; the second is tip growth, during which the catalyst nanoparticle is at the growth front and precedes the precipitation of the CNT behind it. Typical CVD synthesis temperatures range between 750 and 900 °C. Growth processes with low thermal budget are typically required to minimize dopant redistribution in substrates; to eliminate diffusion of metal contacts that might exist on a substrate before the growth step, or to grow nanomaterials on flexible substrates, as well as in many other situations, where high temperature processing is undesirable or impossible.

CNT growth may take place "in air" or on-substrate, depending on how strong the interaction between the nanotube and substrate is. In the first case, tubes grow upwards and fall down either when the reaction has stopped or when the tube becomes too long and too heavy. To control the growth direction, high gas flow rates [18] or an electric field [19] can be used.

During on-substrate growth, CNTs can grow vertically – perpendicular to the substrate, or laterally along the substrate. Vertical CNT growth is often used to grow densely packed arrays of CNTs. For the types of devices discussed in this work, laterally grown CNTs are primarily considered. In this orientation, **graphoepitaxy**, crystallographic alignment with the substrate is possible. One of the first works that experimentally demonstrated this, used faceted nanosteps of sapphire that was cut at different angles with respect to *c*-plane [20] to guide nanotube growth in a given direction. Another graphoepitaxy example is CNT growth on single-crystalline quartz. This method was proven to promote highly horizontally aligned nanotube arrays. Figure 2.3a shows quartz crystal and different cuts that can be obtained from it, which are being used in numerous mechanical and electrical devices. **ST-cut quartz** shows particular utility, since on its surface, CNTs grow parallel to each other and along the *X* plane of the crystal. ST-cut is a type of rotated Y-cut with a cut angle of 42°45′. Figure 2.3d schematically shows a *(5,5)* single-walled nanotube on the surface of ST-cut quartz. Molecular mechanics simulations revealed that Van der Waals forces between quartz and nanotubes are responsible for the alignment, [21]

with *X* direction being the most energetically favorable in terms of CNT interaction with underlying Si atoms. The largest distance between silicon atoms and nanotube is in the *X* direction – best seen on the right image in figure 2.3d. As a result, the interaction with CNTs is minimized. Figure 2.3b shows how the interaction energy of ST-cut quartz with the nanotube depends on the orientation angle, with a global minimum at 0 degrees, i.e. along the *X* direction. Interestingly, nanotubes with alignment governed by Van der Waals forces, allows them to grow perpendicular to step edges and in some situations CNTs can climb over features 3 times higher than their diameter [21].

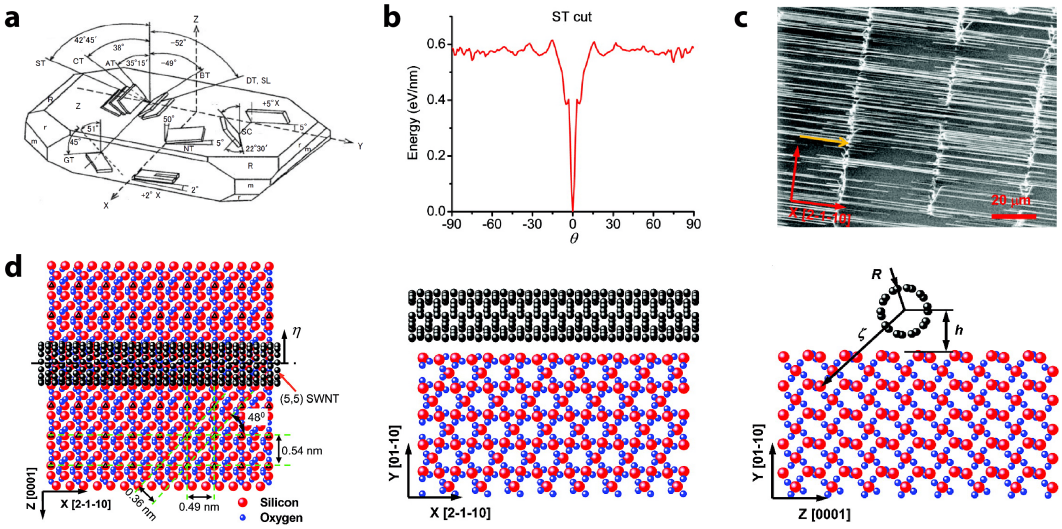


Figure 2.3. Graphoepitaxial growth of carbon nanotubes on the surface of quartz. (a) Different quartz crystal cuts available commercially [https://www.qiaj.jp/pages/frame20/page01-e.html]. (b) Nanotube orientation dependent interaction energy between CNT and ST-cut quartz. (c) SEM image of CNTs aligned along *X* direction of ST-cut quartz. (d) Schematic illustration of a *(5,5)* CNT on the surface of ST-cut quartz in three projections. (b-d) Adapted with permission from [21]. Copyright (2019) American Chemical Society.

In addition to the ability to grow nanotubes in predefined directions, it is important to control their location on the wafer and their chirality. The former can be achieved by patterning catalyst islands from which nanotubes will grow. The latter has yet to be achieved and is the so-called *"holy grail"* of CNT science. Developing a process that would enable CNT growth with predefined chirality, would immediately help nanotubes to move from academia to industry. While imperfect, many different CNT growth techniques have been developed that increase the chiral selectivity, yielding predominantly semiconducting nanotubes. For instance this was achieved by controlling catalyst type [22]; introducing methanol [23] or vapors of water [24] during the synthesis, or by selectively destroying metallic nanotubes with UV and

other radiation [25, 26]. It is also possible to perform diameter-dependent etching [27, 28], or etching of only metallic nanotubes, which can be selectively exposed with a thermocapillary polymer [29]. Another method is to burn metallic nanotubes using electrical breakdown after integration into devices by applying source-drain voltage only [30] or both source-drain and gate voltages [31].

While synthesis of single-chirality nanotubes is still challenging, it is at least possible to control the diameter distribution of CNTs. This can be done by growing them from catalyst nanoparticles of known size. Low diameter nanoparticles (below ~2 nm) define nanotube diameter and can be used to synthesize almost exclusively single-walled nanotubes. In addition to diameter control, nanoparticles density can control the density of nanotubes. Thus, growing CNTs on quartz, from lithographically defined catalyst islands with nanoparticles of known size, allows control of their growth direction, location on the wafer, and diameter distribution, respectively. This, among other issues, is still not enough to end the silicon hegemony, but sufficient for fundamental studies.

Carbon nanotube field effect transistors (CNFETs). A typical CNFET device consists of a CNT that is clamped with metallic pads from both sides, serving as source and drain electrodes. Gate electrodes can be located in close proximity to the nanotube and separated from it with dielectric. The nanotube itself plays the role of the semiconducting channel, hence the requirement of growing purely semiconducting tubes, discussed previously. CNFETs are objects of intense research due to several compelling electrical properties of CNTs: ballistic electron transport (i.e. without scattering with defects, phonons, etc.) over micrometers range [32, 33]; high field effect (>79'000 cm^2/Vs) and intrinsic (>100'000 cm^2/Vs) [34] mobilities at room temperature; high current densities, and absence of short-channel effect in devices as small as 9 nm [35].

Many different CNFET geometries exist and can be divided into two categories: transistors with nanotubes (1) on-substrate or (2) suspended. Devices with on-substrate nanotubes are easier to fabricate, but they typically suffer from unwanted interactions with the underlying substrate. Fixed oxide trapped charges can screen electric fields from the gate electrode, and shift threshold voltage of the transistor as a result. Another undesirable interaction is the interaction with water molecules present on the surface of the substrate. This may result in hysteretic behavior (i.e. forward and backward gate voltage sweeps have different threshold voltages), which is unacceptable for many practical FET applications, but can be

used to fabricate memory devices [36]. Higher quality oxides and/or passivation layers can be engineered to overcome the above-mentioned problems. Typically, this is realized by fabricating top-gated devices using high-κ dielectrics such as HfO_2, Al_2O_3 and others. In addition to a higher quality interface with the nanotube, top gated devices allow switching of individual transistors in ICs, unlike common bottom gate devices.

In contrast to on-substrate devices, **nanotubes suspended in air** may offer an unaltered conduction (in terms of nanotube-substrate interaction) with hysteresis-free performance [37]. Most suspended devices are fabricated with a bottom gate, which decreases the efficiency of the electric field due to the low dielectric permittivity of air and/or relatively high distance from the nanotube. Another drawback of such a device is its fragility due to the suspension of a-few-atoms-thick nanomaterial at its "heart". However, one of the most important advantages of suspended nanotube configuration is the ability to integrate a gate electrode around the nanotube. Such configuration is typically called a **gate-all-around (GAA) geometry**, which is natural to CNTs, and provides the best electrostatic coupling between the semiconducting channel and the gate. By integrating the GAA structure with the incorporation of a thin, high-k dielectric, it should be possible to achieve ideal near-60 mV/dec *SS* switching behavior. Although the ideal limit has not yet been demonstrated experimentally, *SS* reaching a close-to-perfect 99 mV/dec operation has been shown [38].

In terms of **conduction mechanism**, two types of CNFETs exist: ohmic and Schottky barrier transistors. If the charge carriers can travel through the metal - nanotube (semiconductor) junction freely, the contact is called ohmic and the electron transport depends on the nanotube properties, i.e. the gate electrode changes the conductivity of the CNT only. If charge carriers should undergo injection into the channel through the barrier formed at the interface between semiconductor (CNT) and metallic electrode, the device is called a Schottky barrier CNFET (sb-CNFET). In this case, an electric field is needed to lower the barrier and channel resistance to turn on the transistor. With decreasing CNT channel lengths, the Schottky barrier starts to dominate and the metal-to-nanotube junction becomes more important for the conduction mechanism.

Carbon nanotubes are ambipolar in nature (i.e. can conduct both electrons and holes at positive and negative gate voltages respectively), however, in real-world devices, the contact material typically defines the polarity of sb-CNFET due to Fermi level

mismatch. If a high work function metal is used for the electrodes, such as Au or Pd, the CNFET will be p-type [39]; and if a low work function metal is used, such as Sc or Er, the CNFET will be n-type [40]. Another approach to control the polarity of the CNTFET, is to engineer an environment around it. For instance, it was shown that non-stoichiometric HfO_2 deposited on single-walled CNT bundles, results in n-type doping [41], despite using high-work function Pt source/drain electrodes. In addition to conductivity control, CNT passivation eliminates its interaction with the ambient environment, reducing the device-to-device variability.

2.3.2 Transition metal dichalcogenides

Transition metal dichalcogenides (TMDs) are another class of materials having extraordinary physical and chemical properties and are finding more and more applications in electronic and optical devices. TMD materials have a chemical formula of ME_2, where M is a transition metal, such as Mo, W, Pt or Pd; and E is one of the chalcogen atoms from group 16 of the periodic table, such as S, Se or Te. The structure and properties of TMDs are discussed in the following section.

Structure. TMDs may have different structures, but two of the most stable ones typically observed are octahedral 1T and trigonal prismatic 2H phases (figure 2.4a). The former has "ABC" stacking of atoms, whereas the latter has "ABA". In the 2H phase, chalcogen atoms are located in the same position in each layer of the stacked material, which is in contrast to the 1T phase, where chalcogen atoms are at an angle with regards to their "relatives" in the previous/next atomic plane.

Due to a wide variety of possible transition metal - dichalcogenide combinations, a lot of new materials have been predicted and experimentally shown, with many unique and tunable properties. Figure 2.4b shows different TMD materials, among which MoS_2 is one of the most studied materials with promising characteristics for electronic devices. Similar to graphene, many TMDs have two-dimensional (2D) layered structures, and have desirable quantum confined properties when isolated as few- to single-layers. Further, most of the monolayer TMDs are inherently semiconducting and no additional band gap engineering is typically required, unless specific properties need tailoring.

Electronic properties. Figure 2.4c shows how the band structure of MoS_2 varies with the number of layers. Monolayer MoS_2 is a direct band gap semiconductor with a theoretical band gap of 1.7 eV [42]. Thicker MoS_2 becomes an indirect band gap semiconductor and loses some of its compelling properties, such as

strong photoluminescence, important for optoelectronic applications [43]. Another MoS_2 property that emerges only in monolayer material is the valley polarization phenomena, which arises due to inversion symmetry breaking and spin-orbit coupling [44]. Figure 2.4d schematically shows monolayer 2H MoS_2 band structure. Other TMDs also show thickness-dependent properties. For instance, the band gap of WS_2 changes from direct to indirect and increases with growing number of layers, while for Pt-based dichalcogenides, it is only indirect [45].

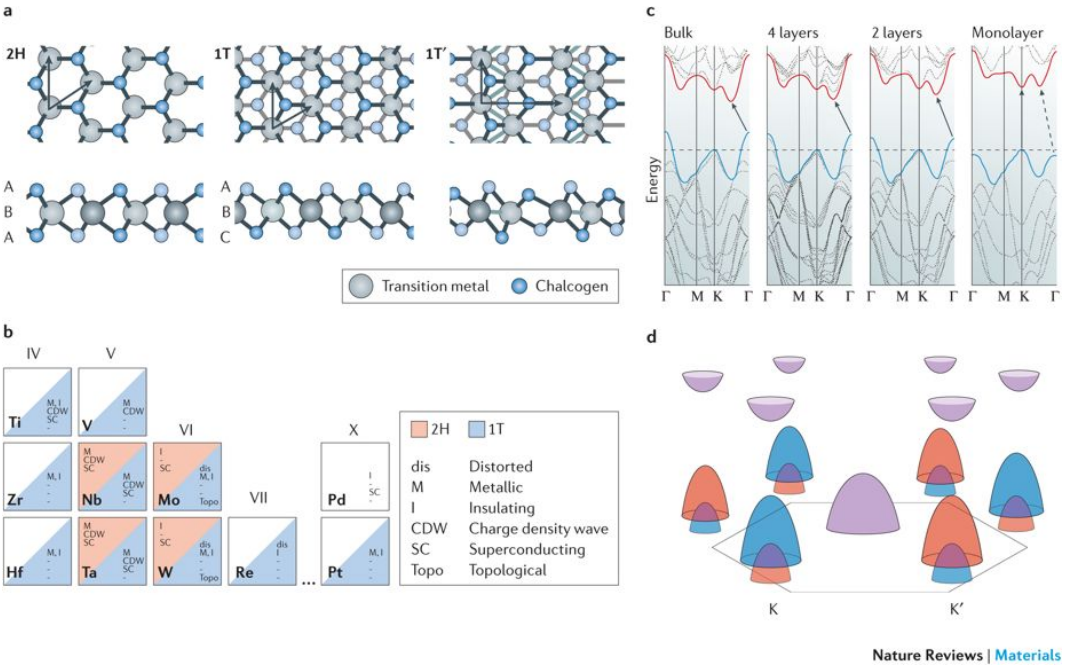


Figure 2.4. Transition metal dichalcogenides structure and electronic properties. (a) Octahedral and trigonal phases of TMDs. (b) A family of TMD materials having different physical properties. (c) Layer-dependent band structure of 2H MoS_2. (d) Schematic illustration of a monolayer 2H MoS_2 band structure. Reprinted by permission from Springer Nature [46]: Journal Publisher - Nature, Nature Reviews Materials © 2017.

Screening length. Besides leakage current and power dissipation problems, aggressive miniaturization of electronics leads to appearance of short-channel effects. One of the ways to quantitatively evaluate them is to estimate the screening length of FETs, using the following equation:

$$\lambda = \left(\frac{\varepsilon_{body}}{\varepsilon_{ox}} \times W_{DM} \times t_{ox} \right)^{1/2}, \tag{2.12}$$

where ε_{body} and ε_{ox} are dielectric permittivities of semiconducting channel and dielectric (oxide), respectively. W_{DM} is maximum doping dependent depletion width and t_{ox} is dielectric thickness [47]. Once the channel width l_c becomes comparable

with the screening length λ, charge carrier concentration starts to be more controlled by the drain electrode, rather than by the gate voltage. In general, for successful MOSFET down-scaling l_c should be ~2 times larger than λ. For 2D TMDs, W_{DM} becomes equal to the thickness of the material, so a low screening length can be obtained by using a-few-atoms-thick TMDs with high-κ dielectric thin films.

Synthesis. The first scientific study of TMDs, particularly MoS_2, dates back to 1923. In this work [48] the authors characterized the crystal structure of molybdenite using X-ray diffraction, and were able to study the arrangement of atoms in the crystal. After 40+ years of work, by 1970, about 60 TMDs were discovered, ~20 of them having layered structures [49]. However, the rapid resurgence in interest in TMDs resumed some 40 years later, after the well-known experimental demonstration of graphene. Mechanical exfoliation of graphene, TMDs, and other materials became a hot topic since the technique enabled the synthesis of high-quality monolayers on scales sufficient for fundamental studies [11, 50, 51]. Chemical exfoliation is another way of producing mono- and a few-layer TMDs [52, 53]. This is typically achieved by ultrasonication of TMD powder in an appropriate solvent. Intercalation with different atoms can be used to facilitate the process, which may require additional purification steps, otherwise intercalated material can cause phase changes, converting the semiconducting 2H phase into the metallic 1T phase [54].

The main drawback of any exfoliation approach is associated with the difficulty of scaling up the process. Precise, wafer-scale fabrication is still challenging using this method. Thus, bottom-up approaches need to be explored to make TMD fabrication compatible with very large scale integration (VLSI), which is also applicable to other nanomaterials and systems. Currently, chemical vapor deposition (CVD) is a prevalent method for large area growth of TMDs. This can be achieved by introducing transition metal and chalcogen vapors in the reactor, which can form TMDs on the substrate surface. One of the most cost-effective and widely used techniques for synthesizing TMDs involves the direct vaporization of sulfur and transition metal containing powders by heating. The vapors are carried by inert gas (e.g. Ar or N_2), forming TMDs on a substrate located downstream inside the reactor, or above a boat containing the transition metal powder [55]. Metal organic chemical vapor deposition (MOCVD) has also been used to synthesize high quality wafer-scale MoS_2 using gas phase precursors [56]. The resulting material had a high electron mobility of 30 $cm^2V^{-1}s^{-1}$ at room temperature and was uniform across a 4 inch wafer.

Another related method is atomic layer deposition (ALD) [57]. In the referenced example, gas phase $Mo(CO)_6$ and H_2S were used to produce MoS_2. Additional high-temperature annealing in H_2S atmosphere was required to improve the material's properties and stoichiometry. One of the problems with ALD of sulfides is that it requires dedicated reactor, as sulfur can cause contamination of the reactor and other materials that will be grown in the same chamber.

Yet another approach is to pre-deposit a thin film seed-layer of metal (M) [58] or metal oxide (MO_x) [59, 60], which can be later chalcogenated. This approach allows precise control over the location of the future TMD material, since the seed layer can be lithographically patterned by performing lift-off or dry/wet etching. Metals or metal oxides can be deposited using physical vapor deposition (PVD) processes, such as electron beam and thermal evaporation, or sputtering. PVD typically allows uniform thin film deposition with a thickness of 5+ nm and a precision of ~1 nm. As a result, the final material is 5 ± 1 nm or thicker. After conversion, depending on the seed layer and chalcogen type, the final thickness of the TMD is even higher, resulting in a multilayer or bulk material. Thus, for monolayer and a few layer TMDs, the seed layer should be super-thin and for reproducible results, run-to-run thickness reproducibility should be sub-1 nm. **Atomic layer deposition (ALD)** is a perfect solution to meet the imposed seed layer thickness requirement, since it allows angstrom-level precision growth of (mostly) oxides on a wafer scale. In addition, ALD can uniformly and conformally cover high aspect ratio structures, which may enable 3D integration of TMDs into devices. ALD was used to grow WO_3 of different thickness ranging from 1 to 3 nm, resulting in a uniform and pinhole-free thin film on the surface of 4 inch wafer. It was shown that by changing thickness and converting the resulting oxide into sulfide, it is possible to control the number of layers in WS_2 and achieve monolayer material [61].

2.4. Ferroelectricity and negative capacitance

Introducing the negative capacitance (NC) FET concept requires revisiting the equation 2.5 that estimates the slope of the FET transfer curve. Two conclusions were made: terms m and n, which are body factor and conduction/injection mechanisms respectively, need to be minimized to achieve steep slope performance. Since NCFETs are still FETs, n is limited to 60 mV/dec (at room temperature), so

the subthreshold swing of a FET can be rewritten as:

$$SS = \frac{\partial V_g}{\partial (logI_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_s}}_{\text{m}} \times 60\,mV/dec. \tag{2.13}$$

Thus, for FET's sub-Boltzmann operation m should be less than 1. A possible solution for that lies in the utilization of a material with negative capacitance in the FET gate stack. In the next section, NC phenomena, and what materials can deliver it, will be discussed and reviewed.

2.4.1 Negative capacitance

A typical FET gate stack is a multilayer structure, consisting of a gate electrode and a semiconducting channel, separated with an insulator. This configuration can be treated as two capacitors connected in series, among which gate voltage V_g is divided. The ratio between the gate voltage V_g and the potential at the surface of the channel ψ, from equation 2.13 can be calculated using the following equation:

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}}. \tag{2.14}$$

If C_{ins} will be negative, the m term in equation 2.14 will become less than 1 and it will be possible to achieve sub-60 mV/dec operation. To demonstrate the behavior of a regular (positive) or a negative capacitors, the following relationship can be used:

$$C = \frac{dQ}{dV}, \tag{2.15}$$

which means that for C to be negative, the amount of charge should decrease, while increasing the applied voltage (figure 2.5a). Capacitance can also be explained from the potential energy point of view:

$$C = \left(\frac{d^2U}{dQ^2}\right)^{-1}. \tag{2.16}$$

Figure 2.5b compares energy landscapes of a positive and negative capacitors. One

class of materials that can obtain negative capacitance values are ferroelectrics. Ferroelectric materials possess spontaneous polarization, which can be reversed by applying an electric field. Ferroelectric capacitors show a complex energy landscape, depicted in figure 2.5c, and unlike regular dielectric material, with a quadratic relation between energy and charge, ferroelectrics have two energy minima. From the *Q-U* relationship around $Q = 0$ (denoted with dashed rectangle), we can see that the curvature is oriented downwards, confirming that the ferroelectric material has a region that can have a negative capacitance (compare with the energy landscape of a negative capacitor in figure 2.5b). To demonstrate the microscopic origin of ferroelectric material polarization, figure 2.6a shows the unit cell of a ferroelectric orthorhombic phase of HfO_2. Two polarization states are demonstrated, where oxygen atoms displace depending on the direction of the applied field.

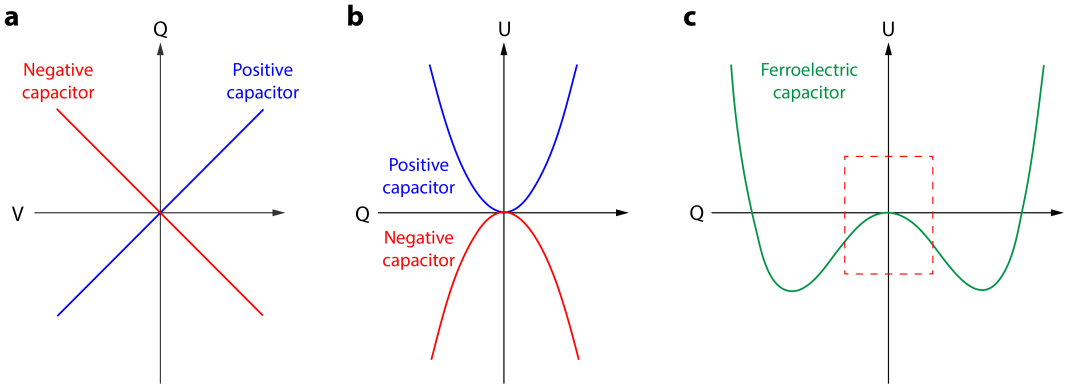


Figure 2.5. Comparison between negative, positive and ferroelectric capacitors. (a) Voltage-charge characteristics. Energy landscape of (b) positive and negative, as well as (c) ferroelectric capacitors. The region under the red box in (c) signifies negative capacitance region.

Landau theory of phase transitions [62] shows that the free energy $U = U(P)$ of a ferroelectric can be represented using the following dependence:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - EP, \tag{2.17}$$

where α, β and γ are material dependent coefficients, out of which β and γ are temperature independent. Coefficient α can be further written as:

$$\alpha = a_0(T - T_C), \tag{2.18}$$

where a_0 is a temperature independent quantity, T is the temperature and T_C is the Curie temperature. When $T_C > T$, α becomes negative, which gives the negative curvature to the energy landscape of a ferroelectric material (region under red box in figure 2.5c).

The equilibrium position can be determined by finding the extremum of U:

$$\frac{dU}{dP} = 0, \tag{2.19}$$

which, by combining with equation 2.17. will result in:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5. \tag{2.20}$$

This equation represents the dependence between the external electric field and the polarizability of ferroelectric. Figure 2.6b shows the polarization-voltage characteristic of hafnium oxide, a ferroelectric that can be represented by this equation. The point where the hysteresis loop intersects with the Y-axis is the remnant polarization P_r of the ferroelectric, whereas the intersection with X-axis gives the coercive field E_c, required to switch the polarization.

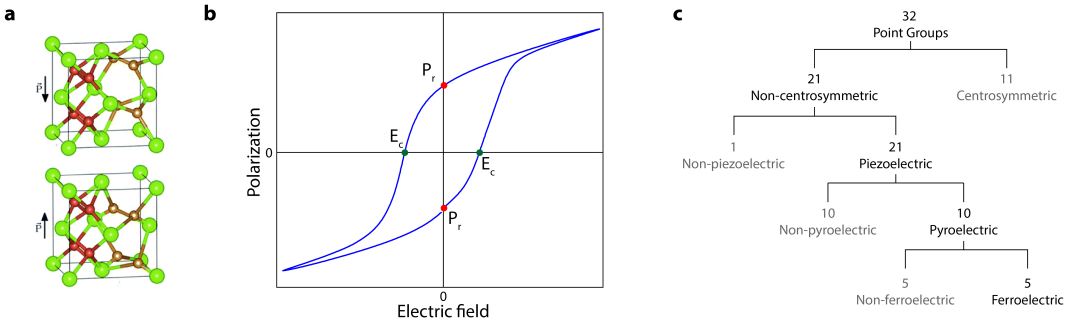


Figure 2.6. Ferroelectricity and structural requirements for it. (a) Two metastable polarization states of hafnium oxide unit cell. Reproduced from the Royal Society of Chemistry [63]. (b) Typical ferroelectric hysteresis loop of doped hafnium oxide sample fabricated in this work. (c) Crystallographic families review and the ferroelectric properties.

By combining equations 2.16, 2.17 and 2.18, considering that for ferroelectrics $Q = P$ [9], one can obtain the following equation for capacitance at $P = 0$:

$$C = \frac{1}{2\alpha} = \frac{1}{2a_0(T - T_C)}. \tag{2.21}$$

For the situation when $T_c > T$, the capacitance becomes negative. As an example, for doped HfO_2 the Curie temperature was reported to be around 450 °C [64], which makes it technologically relevant for many applications.

The negative capacitance behavior was predicted by Landau in 1940 but was not experimentally measured until recently [65, 66]. The reason why it was (and still is) difficult to register this phenomenon is due to the unstable nature of negative capacitance, in which the ferroelectric self-charges and the polarization wants to be at one of the minima of the energy landscape (see figure 2.5c). The next section discusses the structural requirements for a material to have ferroelectric properties.

2.4.2 Ferroelectric material structural considerations

For a material to have ferroelectric properties, it should exhibit reversable spontaneous polarization, which arises from dipoles aligning under an applied electric field. When the field is turned off, the ferroelectric material has a non-zero remnant polarization. If a high enough electric field of opposite magnitude is applied, it should be possible to switch the polarization, which will also stay when the electric field is switched off.

From a structural point of view, ferroelectric material should have a specific crystalline structure. All crystals can be divided into 32 crystallographic point group classes (figure 2.6c), 11 of which are centrosymmetric, non-polar and cannot have ferroelectric properties. The remaining 21 classes do not have center of symmetry and can be further divided into piezoelectric (20 classes) and non-piezoelectric (1 class). Piezoelectricity is the ability of a crystal to polarize electrically under applied strain. Half of the piezoelectrics do not have spontaneous polarization since their dipoles are aligned along different axes, cancelling the effect of each other. Only 10 classes, called pyroelectrics, have a unique polar axis that can contribute to spontaneous polarization and form permanent dipoles. There is no crystallographic difference between ferroelectrics and pyroelectrics. However, only ~5 out of 10 pyroelectric classes can be practical for ferroelectric application since only these classes can withstand electrical field cycling, required for polarization switching, without dielectric break-down.

Perovskite-type ferroelectrics are the most widely studied ferroelectric materials. The list includes $Pb(Zr_{0.2}Ti_{0.8})O_3$, $BaTiO_3$, $SrTiO_3$, and others. The spontaneous polarization in these materials originates from the distortion of the oxygen octahedra

[63]. Perovskite materials have very high remnant polarization and dielectric constants, and are widely used in memory devices. However, perovskite-type ferroelectrics have scaling problems since they loose their ferroelectric properties once their thickness becomes less than ~70 nm [67, 68]. In this context, HfO_2-based ferroelectrics are strong candidates for electronic applications, delivering high remnant polarization and low leakage current in ultra-thin films. One of the main advantages of ferroelectric hafnia is the possibility to synthesize it using ALD. ALD of doped and non-doped HfO_2 is a low-temperature, silicon-technology-compatible process that enables 3D integration of ferroelectric capacitors [69] and makes HfO_2 a unique ferroelectric material system.

2.4.3 Ferroelectric HfO_2

HfO_2, or hafnia, is a well-known high-κ dielectric, that has been used in the semiconductor industry for decades. It has a dielectric constant of $\kappa = 25$ and a band gap of $E_g = 5.8$ eV, which makes it a great choice as an insulator in FET gate stacks. Its high dielectric constant helps to maximize breakdown voltage, and its large bandgap minimizes tunneling current. Crystallized and/or doped hafnia possesses an even higher dielectric constant than amorphous hafnia, which can further support equivalent oxide thickness (EOT) scaling [70]. In 2011, a research group from Namlab (Germany) discovered ferroelectric properties in hafnia, while studying its electronic properties as a function of doping [71]. The reported thin film showed a ferroelectric hysteresis loop, with remnant polarization above 10 $\mu C/cm^2$, and a coercive field of 1 MV/cm^2. Yttrium doped HfO_2 was deposited using ALD, and by changing the number of YO_x cycles, it was possible to achieve different dopant concentrations - ranging from 2.3 to 12.3 mol%. This work demonstrated synthesis of ferroelectric hafnia, with properties that could be tailored using several parameters. Today, more than 400 papers about ferroelectricity in hafnia have been published, and this number continues to grow.

Many applications are proposed for ferroelectric hafnia, which includes ferroelectric and negative capacitance field effect transistors, memory devices and others. Compared to existing ferroelectrics with perovskite type structures, hafnia is not affected by the size-effect, which was preventing continuous downscaling of thickness in conventional ferroelectric thin films [72]. Ferroelectricity has been observed in doped HfO_2 films as thin as 2.5 nm [73], which allows for further miniaturization of electronics and has already enabled fabrication of CMOS-compatible hafnia-based ferroelectric FETs [74], as well as

three-dimensional capacitors [69].

The origin of ferroelectricity in HfO_2. At standard temperature and pressure, as-obtained bulk HfO_2 consists predominantly of the monoclinic phase, and if annealed goes through structural changes, transforming from monoclinic to tetragonal at ~1700 °C, and to cubic phase at ~2500 °C [75]. Figure 2.7 shows unit cells of these three phases, which have inversion symmetry, therefore polar, and do not possess ferroelectric properties.

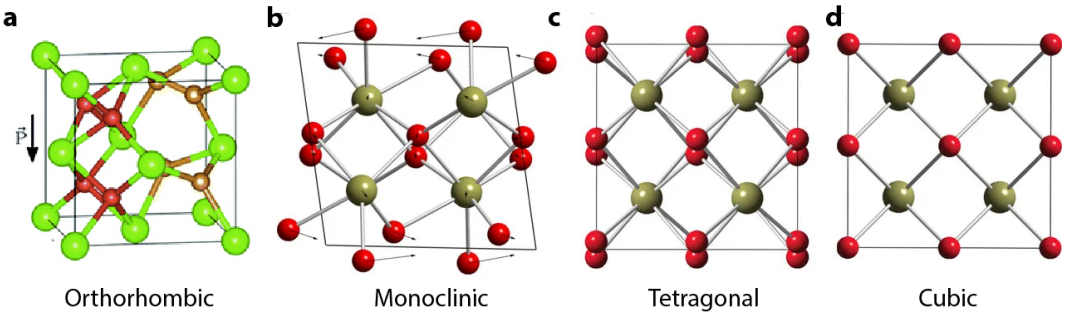


Figure 2.7. Hafnium oxide polymorphs. (a) orthorhombic, (b) monoclinic, (c) tetragonal and (d) cubic phases of HfO_2. Adapted with the permission from the Royal Society of Chemistry [63] and from an open access article [76] based on CC BY license.

Besides the structural difference between HfO_2 polymorphs, there is also a significant difference in dielectric constant, which was reported theoretically [77] and later shown experimentally [78, 79]. The phase-dependent dielectric constant evolution of hafnia was studied by Boscke *et al.* with the aim to maximize it [71]. The authors discovered hysteretic behaviour of the polarization under applied electric field of Si doped HfO_2 that is characteristic to ferroelectric materials. This was the first demonstration of ferroelectricity in hafnia, which was explained by the formation of a non-centrosymmetric orthorhombic phase (space group *Pca21*) that was evidenced by XRD measurements. The structure of HfO_2 is similar to the structure of ZrO_2, for which the existence of the orthorhombic phase was predicted by Kisi *et al.* [80]. Later, Huan *et al.* simulated different hafnia polymorphs using a first-principles based structure search algorithm, and figured out that two orthorhombic polar phases belonging to the *Pca21* and *Pmn21* space groups may indeed exist in HfO_2 and possess ferroelectricity [81]. It is believed that the non-centrosymmetric orthorhombic hafnia can switch between two states by applying an electric field (see figure 2.6a), which results in significant spontaneous polarization. In addition, it was shown that by increasing the orthorhombic phase fraction in HfO_2, it is possible to increase its remnant polarization, further confirming this phase is responsible for the ferroelectricity [82].

Many synthetic parameters have an impact on the stabilization (maximization) of the ferroelectric orthorhombic phase in HfO_2. These parameters include thermal budget (annealing temperature and time), dopant concentration, film thickness, effect of electrodes, cool down rate and many other. Figure 2.8 shows some of the trends that are known today and should be optimized to induce ferroelectricity in HfO_2 [83], details of which are discussed below.

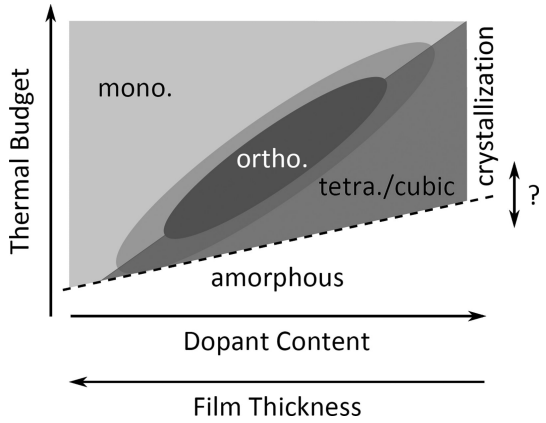


Figure 2.8. Ferroelectric window of HfO_2 and its dependence on fabrication conditions. Reprinted from [83], with the permission of AIP Publishing.

Ferroelectric thin film HfO_2 growth methods. Various techniques have been used to synthesize pure and doped HfO_2. By far, the most widely used method is ALD. ALD relies on sequential pulsing of gas phase precursors that react on the surface of a substrate in a self-limiting manner. This enables the growth of thin films with sub-monolayer precision and conformal coating of high aspect ratio structures. The resulting thin films are uniform and pinhole-free. Different ALD precursors can be used to synthesize HfO_2, among which TEMAH (tetrakis(ethylmethylamido)hafnium(IV)) and TDMAH (tetrakis(dimethylamido)hafnium(IV)) are the most widely used. As an oxygen source, water, ozone, or oxygen plasma can be used. The typical reaction temperature using these precursors, is in the range of 240-280 °C. In general, the growth rate is around 1 Å/cycle, and the resulting thin films are amorphous, or in some cases nanocrystalline. Additional pulsing of other metal-oxide precursors (e.g. Al_2O_3, SiO_2, ZrO_2) can be used to precisely dope hafnia, which is crucial for ferroelectric phase stabilization during subsequent processing steps.

Another popular technique used to synthesize pure or doped HfO_2, **is radio frequency (RF) sputtering**. This method relies on Ar ions formation by glow discharge and acceleration towards a target material. The collision results in ejection of target atoms, flying towards the sample and forming a thin film. HfO_2 can be

deposited directly from a hafnia target or by using metallic Hf in the so called reactive sputtering regime. A controlled amount of oxygen is introduced into the chamber to react with Hf atoms, forming HfO_2 on the substrate. Multiple materials can be co-sputtered at the same time. The deposition rate of each material can be controlled individually by varying source power or tuning the shutter open time, giving control over the dopant concentration in the final film. As-sputtered thin films are typically amorphous and require additional post-deposition processing to crystallize them, just like ALD films.

Sputtering has been used to grow Y:HfO_2 [84, 85], Gd:HfO_2 [86], $Hf_xZr_{1-x}O_2$ [87, 88, 89], as well as pure ferroelectric HfO_2 [90].

Pure or doped hafnia can be grown using numerous other techniques, each having their own advantages and disadvantages, discussed elsewhere. The list includes metalorganic chemical vapor deposition [91], chemical solution deposition [92], pulsed layer deposition [93, 94], and others.

Both sputtering and ALD can be also used to grow device electrodes, such as TiN and TaN, depicted in figure 2.9a. While ALD is a long, relatively high temperature process, sputtering avoids prolonged annealing of HfO_2 during the deposition of the top electrode.

Impact of dopant type. As it was discussed above, the non-centrosymmetric orthorhombic phase is believed to be responsible for ferroelectricity in HfO_2. The incorporation of various dopants in hafnia can help stabilize the orthorhombic phase and reduce the fraction of competing phases. The dopant list includes Al [95], Si [96, 97, 98], La [99, 100], Gd [101], Y [102], Sr [103], and Zr [89, 104, 105]. It has been shown for all these dopants, that there is an optimum dopant concentration. Initially, as the dopant concertation increases, remnant polarization increases, reaching a peak value and subsequently decreasing as the dopant concentration increases further. Remnant polarization evolution (i.e. polarization value when the external electric field is switched off), as a function of dopant concentration, was also correlated with crystallization changes in HfO_2 using grazing incidence X-ray diffraction (GIXRD). It was shown that the dominant-phase changes from monoclinic to orthorhombic to tetragonal, directly impacting the ferroelectricity in HfO_2.

Park *et al.* explained the dopant-dependent orthorhombic phase stabilization using the classical nucleation theory [106]. According to this work, if the monoclinic

phase is formed, its transformation into metastable phases, such as tetragonal and orthorhombic, is unlikely. The calculations showed that the doping concentration should be high enough to suppress the monoclinic phase, making its formation energetically less favorable during the annealing step. If so, a second most stable tetragonal phase is formed, which can undergo a second phase transition into monoclinic or orthorhombic phase during the cool down step. If the doping concentration is too high, the tetragonal phase is still energetically more favorable, but formation of the orthorhombic phase is suppressed. Park *et al.* conclude that in general the process governing stabilization of the ferroelectric orthorhombic phase starts with nucleation of the tetragonal phase during annealing, followed by a second phase transformation into the orthorhombic phase during cool down.

The effect of annealing. As synthesized, undoped or doped HfO_2 is typically amorphous, or in some cases nanocrystalline, and cannot be ferroelectric. Additional annealing is required to crystallize and stabilize the ferroelectric phase. For this, rapid thermal annealing (RTA) systems are typically used, providing high heating and cooling ramp rates (20 – 250 °C/min).

A typical device architecture for ferroelectric measurements, is hafnia sandwiched between two electrodes, as schematically depicted in figure 2.9a). Metals, such as W, Pt, Au, or synthetic metals, such as TiN or TaN, can be used. It was shown that the orthorhombic phase is more efficiently stabilized in the presence of a capping layer (top electrode); i.e. annealing should be performed after the metallization step [107, 108]. It is believed that the mechanical confinement provided by the top layer, makes the transformation to the orthorhombic phase more energetically favorable. It was shown that the metal-oxide interfacial effects are equally important.

In terms of structural changes, i.e. crystallization itself, a sample-specific temperature needs to be found to maximize the orthorhombic phase fraction. Typically, this temperature lies in the range between 450 and 1100 °C. The sweet spot highly depends on other synthetic parameters depicted in figure 2.8. The annealing duration can vary from 1 second to minutes. The annealing environment is typically inert gas (N_2 or Ar) at atmospheric pressure.

Park *et al.* used *in-situ* high temperature XRD to study the annealing temperature-dependent crystallization of doped HfO_2 [110]. Based on these measurements, the authors hypothesize that orthorhombic phase is formed from the crystallites with tetragonal or cubic structure during the cool down step. Later these experimental observations were theoretically explained by the same group

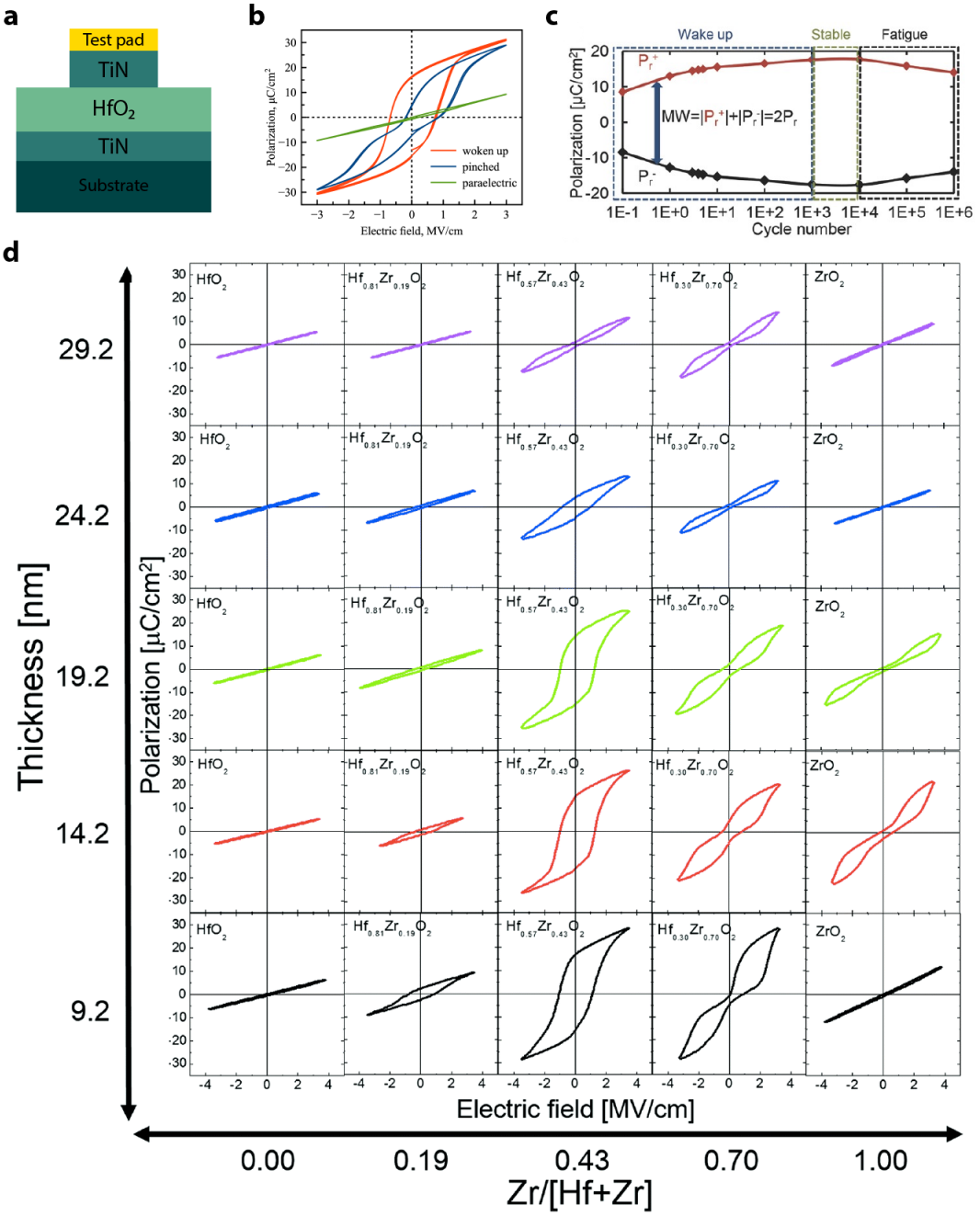


Figure 2.9. Ferroelectric characterization of HfO_2 capacitors. (a) Typical metal-insulator-metal capacitor configuration fabricated for ferroelectric measurements. (b) An example of the ferroelectric measurement of one of the fabricated $Hf_{0.5}Zr_{0.5}O_2$ devices in this work. (c) Evolution of the remnant polarization of ferroelectric Si:HfO_2 after electric field cycling. Reproduced with permission of Wiley-VCH from [109]. (d). Ferroelectric hysteresis loop evolution of $Hf_xZr_{1-x}O_2$ as a function of thickness and dopant concentration. Reproduced from [104] with permission from The Royal Society of Chemistry.

using classical nucleation theory [106]. The work showed that at a specific annealing temperature, the tetragonal phase formation is energetically favorable, and transforms into the orthorhombic phase during cool down.

Since in RTA systems it is typically difficult to control the cooling rate, it is highly challenging to study its impact on the formation of the orthorhombic phase. This problem motivated us to perform annealing of doped HfO_2 using intense pulsed ion beams (IPIBs). The details of this technology and the obtained preliminary results are given in section 5.3. Briefly, IPIBs transfer energy from pulsed ion beams to samples within tens-to-hundreds of nanoseconds, heating the materials at the same time scale. By changing the irradiation parameters or substrate type (through which most of the heat dissipates), it is possible to control the annealing time, as well as heating and cooling rates. Another motivation comes from the ability to perform ultra-low thermal budget annealing since very high temperatures (up to ~2000 °C) can be achieved in the nanoseconds regime.

A somewhat similar approach to stabilize ferroelectricity in hafnia using low thermal budget annealing was explored using a millisecond flash lamp to crystallize HfO_2 and induce ferroelectricity [111]. The polarization and coercive field showed light intensity dependence, reaching a maximum remnant polarization value of P_r = 21 $\mu C/cm^2$. This technique shows another approach to stabilize ferroelectricity in hafnia using low thermal budget annealing.

Other considerations. Many of the as-obtained ferroelectric HfO_2 capacitors demonstrate pinched hysteresis after the annealing step. As an example, the *P-V* hysteresis loop of one of the $Hf_{0.5}Zr_{0.5}O_2$ samples fabricated in this work is shown in figure 2.9b. The experimental details will be discussed in the next chapter. The green curve demonstrates the results obtained before annealing, showing the paraelectric nature of the material. Annealing stabilized the orthorhombic phase (blue curve), but the hysteresis loop is pinched. After cycling the electric field 10'000 times, the pinching was eliminated, producing a typical ferroelectric hysteresis loop (red curve).

It is believed that the root cause for the pinching are oxygen vacancies trapped in the interfacial layer or domain walls of the polycrystalline hafnia [109]. These trapped charges locally alter the electrical field, pinching the *P-E* loop. Electric field cycling can promote charge redistribution improving the polarization response. In literature, this is referred as the **"wake up" effect**. Moreover, cycling-induced vacancy diffusion results in phase transformation, with woken-up material containing more

orthorhombic phase, further improving the remnant polarization. Figure 2.9c shows the evolution of the remnant polarization of ferroelectric Si:HfO_2, which clearly demonstrates its improvement due to the wake up effect [109]. However, after ~10'000 cycles, the remnant polarization of this particular device started to decrease, which is a consequence of the aging mechanism (fatigue) [112].

Another process to consider in high temperature annealing, is the oxidation of the metallic electrodes or the formation of an interfacial layer due to interdiffusion of the layers, which can impact the ferroelectric properties of the metal-insulator (hafnia)-metal stack. This, for instance, was shown for La doped HfO_2 sandwiched between two TiN electrodes [82]. After annealing at 800 °C, a thin TiO_x layer was formed, and nonuniform oxygen distribution was observed. This and other undesired effects degrade polarization switching by creating trap sites and screening the external electric field.

Thin film thickness also plays an important role in ferroelectric phase stabilization as well. Figure 2.9d shows *P-E* hysteresis loops for $Hf_xZr_{1-x}O_2$ of different thickness and stoichiometry [104]. The best ferroelectric switching was observed for a 9.2 nm thick film of $Hf_{0.57}Zr_{0.43}O_2$ with a remnant polarization of P_r = 16.5 μC/cm^2. Thus, the optimum ferroelectric performance for HZO is when the Hf-to-Zr ratio is ~1:1 and the thickness of the film is around 10 nm.

2.5. Experimentally demonstrated negative capacitance

The previous sections of this chapter discussed the concept of negative capacitance, the ferroelectric materials required for it, as well as one of the most promising ferroelectrics for this application – HfO_2. In this section, a quick review of experimentally demonstrated negative capacitance and reported negative capacitance (NC) transistors is presented.

The first indirect measurement of negative capacitance in ferroelectrics was shown for $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT), which was connected in series with a regular dielectric $SrTiO_3$ (STO). The total capacitance of the bilayer was measured to be higher than the capacitance of STO alone, indicating a negative capacitance of PZT [113].

Another piece of evidence of NC in ferroelectrics came from transient measurements [114], where ferroelectric capacitor charging was studied as a function of time with (sub-) microsecond precision. Such measurements showed that when a rising voltage is applied across a ferroelectric-dielectric stack, there is a small period

of time when voltage across the ferroelectric layer decreases, pointing toward the negative capacitance effect.

More recently, the "S" shaped *P-E* curve, that was predicted by Landau ~80 years ago, was experimentally measured for ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ [65]. Hoffmann *et al.* were able to register the negative capacitance regime while switching HZO from one polarization state to another. The demonstrated negative capacitance had a transient nature (i.e. it was observed for a limited period of time during the switching), but served as direct evidence and a proof-of-concept.

In addition to indirect and direct measurements of negative capacitance in ferroelectrics, the latter materials were integrated into FET gate stacks to demonstrate the long-desired sub-60 mV/dec operation. It is important to note that the ferroelectric negative capacitance is unstable/transient and only appears in a limited region of the polarization switching event. It was proposed that the negative capacitance can be stabilized by connecting it in series with a positive capacitor [9].

Utilization of the NC effect in FETs was first proposed in 2008 by Salahuddin and Datta [9]. Table 2.1 presents an overview of experimentally demonstrated NCFETs and includes the following information (from left to right): FET type and/or channel material, *SS* with NC effect, *SS* before the integration of NC, I_{On}/I_{Off} ratio before NC integration, NC effect span (compare with I_{On}/I_{Off} ratio), NCFET hysteresis (not to confuse with ferroelectric hysteresis), ferroelectric material used, its thickness, deposition method, post-processing (annealing), ferroelectric integration type, and the corresponding reference. Ferroelectric integration type is the approach taken to insert the NC: directly into the multilayer gate stack as one of the layers (internal integration); or as a separate capacitor connected to the gate electrode using wire-bonding (external integration).

Many devices with the NC behavior, resulting in a sub-60 mV/dec performance, have been reported to date, starting from conventional FinFETs, to one- and two-dimensional materials-based transistors. The list of ferroelectrics that have been used is also diverse, and includes perovskite structure type thin films, polymers, and hafnia-based materials. However, many of the reported devices have a number of problems, resulting from the transient nature of the NC. First, and probably the most important one, is the limited range of the sub-60 mV/dec operation that typically spans across a few orders of magnitude of source-drain current. This can be explained by the transient negative capacitance, which improves the electrostatics

only within a small portion of the operation range. Another problem observed in devices published so far, is a hysteretic behavior of the I_d-V_g characteristics. The source of the hysteresis needs to be examined carefully, since ferroelectric polarization switching may cause such behavior. If this is indeed the case, negative capacitance from such ferroelectric is not stabilized and has only a transient effect. Moreover, many of the reported *P-E* hysteresis loops have a far from perfect pattern: cigar-shaped loops and loops without polarization saturation can be caused by leaky dielectric [115]. Leaky dielectric permits charge carrier injection from the gate electrode into the FET channel, which can result in sub-60 mV/dec operation. Some of the papers do not show *P-E* for their ferroelectrics and/or leakage current data at all, which allows question of the root cause of the sub-60 mV/dec performance.

Table 2.1. An overview of experimentally demonstrated negative capacitance field effect transistors.

FET type	**SS w. NC, mV/dec**	**SS w/o NC, mV/dec**	**I_{on}/I_{off} ratio w/o NC**	**NC effect span**	**Hysteresis of FET w. NC, V**	**FE material**	**FE thickness, nm**	**FE deposition method**	**FE post-processing**	**FE integr.**	**Ref.**
Si FinFET	sub-20	-	10^7	-	0.48	PZT	60	-	None	Ext.	[116]
Si FinFET	8.5	-	10^{10}	-	up to 4	$BiFeO_3$	250	Epitaxy	None	Ext.	[117]
Si FinFET	55	87		-	0	HZO	5	ALD	RTA, 600 °C	Int.	[118]
Si planar	45	73	10^5	-	0.2	HZO	70	-	-	Ext.	[119]
Si FinFET	52	-	-	-	0.8	HZO	1.5	ALD	RTA, 700 °C, Ar, 30 s	Int.	[120]
Si planar	23-50	-	-	-	near 0	HZO	9.5	ALD	RTA, 600 °C, N_2, 30 s	Int.	[121]
GeSn Planar	40	-	10^4	-	0.4	HZO	6.5	ALD	RTA, 350 °C	Int.	[122]
Si planar	18	92	10^5	10^5	4	PVDF	18.77	SC	-	Ext.	[123]
MoS_2	11.7	113	10^5	10^4	observed	PVDF	200	SC	-	Int.	[124]
Si planar	13	-	10^5	10^2	10	PZT	100	Sputtering	RTA, 620 °C, 90 s	Int.	[125]
MoS_2	57	67	10^5	10^5	0.17	Al:HfO_2	10	ALD	RTA, 850 °C, 5 min	Int.	[126]
MoS_2	8.5	161	10^6	10^4	up to 6	HZO	12, 23	ALD	RTA, 550-600 °C, 30 s	Int.	[127]
MoS_2	52.3	-	10^6	10^4	0	HZO	20	ALD	RTA, 400-600 °C	Int.	[128]

Table 2.1. An overview of experimentally demonstrated negative capacitance field effect transistors (continued).

FET type	SS w. NC, mV/dec	SS w/o NC, mV/dec	I_{On}/I_{Off} ratio w/o NC	No of decades with NC	Hysteresis, V	FE material	FE thickness, nm	FE deposition method	FE post-processing	FE integ.	Ref.
CNT	55	70	-	-	Yes	Al:HfO_2	10	ALD	RTA, 800 °C, 10 min	Int.	[129]
β-Ga_2O_3	53.1	-	10^6	-	0.1	HZO	20	ALD	RTA, 500 °C, 1 min	Int.	[130]
MoS_2	47	-	10^6	-	2	HZO	15	ALD	RTA, 500 °C, 30 s	Int.	[131]
MoS_2	44	198	10^6	10^4	6	PVDF	400	SC	-	Int.	[132]
Si planar	48	110	10^6	10^3	0	PVDF	16	SC	-	Ext.	[133]
MoS_2	42.5	-	4×10^6	10^5	< 1	PVDF	-	SC	130 °C, 30 min	Int.	[134]
Ge pFET	50	-	-	10^2	0.1	HZO	-	ALD	RTA, 450 °C	Int.	[135]
WSe_2	14.4	79.1	-	10^3	0.2	HZO	20	ALD	RTA, 500 °C, 1 min	Int.	[136]
In_2O_3	10	150	10^8	10^5	1	PVDF	120	SC	-	Int.	[137]
In_2O_3	44	-	10^7	10^4	3	PVDF	-	SC	130 °C, 30 min	Int.	[138]
Ge	45	-	10^4	-	-	Zr:Al_2O_3	Nanocryst.	ALD	450 °C	Int.	[139]

*Abbreviations: Planar - planar MOSFET. SC - spin coating. PVDF or P(VDF-TrFE) - poly[(vinylidenefluoride-co-trifluoroethylene]. W. - with; w/o - with out.

3. Engineering and integration of high-κ dielectrics into Carbon Nanotube FETs

This chapter discusses the process flow development for ALD coating of single-walled carbon nanotubes with high-κ dielectric and their integration into transistors. To promote high-κ dielectric growth on a nanotube surface, a novel TiO_2-based surface pretreatment technique was developed. To study the effect of TiO_2 on the CNT properties, on-substrate bottom-gate and top-gate transistors, as well as suspended CNT structures were fabricated. Structural and electrical characterization showed that the pretreatment strategy did not degrade the nanotube properties and enabled subsequent ALD coating with Al_2O_3 high-κ dielectric. The resulting TiO_2-Al_2O_3 all-oxide compound dielectric uniformly coated the entire length of the suspended single-walled carbon nanotubes and exhibited an improved dielectric constant.

3.1. Single-walled carbon nanotube synthesis and integration into FETs

The multi-stage process developed for the fabrication of CNT FETs, consists of six steps, four of which are lithographic. The major steps are schematically depicted in figure 3.1. Single side polished degenerately doped n-type silicon wafer (ρ = 0.001-0.005 $\Omega \times$ cm) with 50 or 100 nm thick thermal oxide (Virginia Semiconductor, Inc), or single side polished ST-cut quartz (UniversityWafer.com), were used as substrates. The former has the advantage of a ready to use back gate, whereas the latter allows graphoepitaxy. The major steps of the fabrication process flow are presented in the next few sections, whereas the full details can be found in Appendix 6.2.

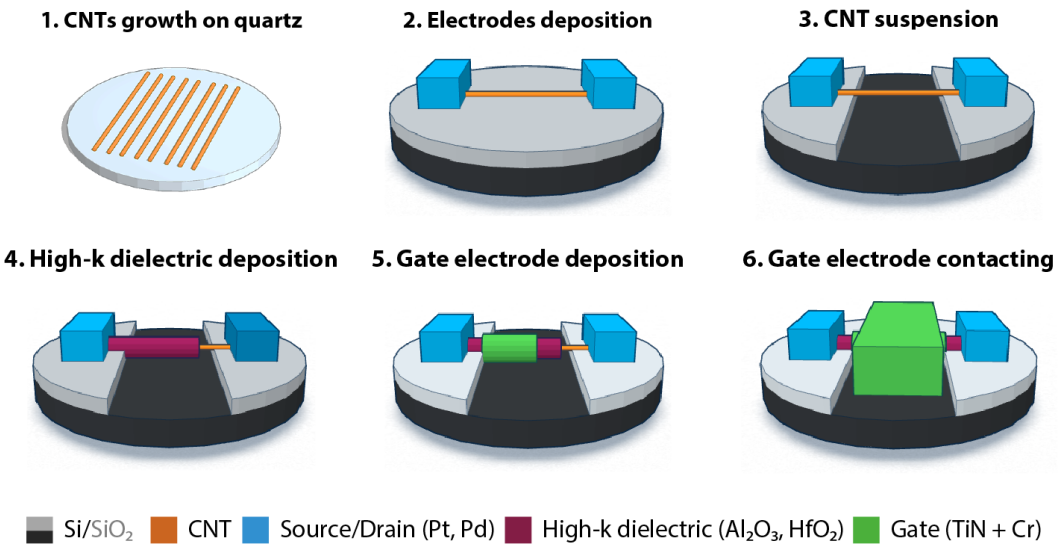


Figure 3.1. CNFET fabrication process flow.

Fabrication of alignment markers. The fabrication starts with defining alignment markers on the substrate. This is required to align all of the lithographic layers with respect to each other. Samples were first annealed in an oven at 180 °C for 5 min and cooled down to room temperature to remove moisture from their surface and improve photoresist adhesion. Next, ma-N 1420 negative-tone photoresist (Microresist technology GmbH) was added on the surface of the wafer and spun at 4000 RPM (revolutions per minute) for 45 seconds. On smaller samples (0.5×0.5 or 1×1 cm), to improve the contact between the photoresist and the photolithography mask used in the next steps, the formed edge beads were manually removed using cleanroom swabs soaked in acetone – gently wiping the edges of the chip right after spin-coating. After positioning the sample under the ABM mask aligner (ABM-USA, Inc), the sample was brought into soft contact with the mask to perform levelling, and moved down for alignment. While observing under a microscope, the sample position was adjusted using X, Y, and rotation micrometers knobs. The sample was brought into vacuum contact and exposed with a UV source having a typical energy density of 90 mJ/cm^2 (t = 6.4 s for P = 14 mW/cm^2). Next, samples were developed in a TMAH-based developer (ma-D 533/s - Microresist technology GmbH) for 50-60 seconds, and thoroughly rinsed in deionized (DI) water. The thickness of the photoresist after development was measured using a Dektak 150 profilometer (Bruker Corporation, USA) by scanning across exposed and unexposed/developed areas, and was estimated to be ~1.7 µm. This photolithography process was used to define different structures during subsequent steps and hereinafter will be referred as “the standard ma-N 1420 recipe”.

After developing the photoresist, samples were moved to a thermal or electron beam evaporator for Cr evaporation. Cr films were deposited to a thickness of 30 nm, at a rate of 1 Å/s and a pressure better (lower) than 5×10^{-6} mbar. Next, the Cr layer was lifted-off by ultrasonication in acetone for 5 minutes at room temperature, then rinsed in 2-propanol (IPA) and blow-dried with N_2. The resulting alignment markers provided sufficient optical contrast both on Si/SiO_2 and quartz (transparent) substrates. Several potential issues were considered for the marker fabrication: (1) the metal used for the marker should be stable at the CNT growth temperature (865 °C, 30 min); (2) the metal should not inhibit CNT growth; (3) markers should be thick enough to have sufficient contrast after growth, since some of material will diffuse or evaporate. Chromium markers met all of these requirements.

Catalyst island fabrication. CNTs were grown using a thermal chemical vapor deposition (CVD) technique that relies on the dissociation of a carbon containing gas phase precursor (methane - CH_4) on catalyst nanoparticles (iron - Fe). Iron catalyst islands were fabricated using standard lithography and lift off processes. After photoresist patterning using the standard ma-N 1420 recipe, samples were annealed in oxygen plasma to remove possible photoresist residues. This was achieved by processing samples in an Oxford 80+ Reactive Ion Etcher (Oxford Instruments, UK) for 2 minutes, while flowing O_2 at a flow rate of 60 sccm, plasma power of 150 W, and a chamber pressure of 60 mTorr. After oxygen plasma etching, iron with a nominal thickness of 2 Å was deposited using thermal evaporation at a deposition rate of 0.1 Å/s and a pressure better than 5×10^{-6} mbar. The subsequent lift-off process was performed by leaving samples in hot acetone at 50 °C for 30 minutes, followed by rinsing in IPA. Sonication was not used, which was observed to remove the ultra-thin Fe layer. After the lift-off step, some of the samples had photoresist residues visually observable under an optical microscope, however these residues did not seem to impact the CNT growth process, which could be due to the polymer burning during the prolonged high temperature oxidation step required during CVD.

Carbon Nanotube synthesis. The CVD synthesis of nanotubes was performed in a Lindberg/Blue M - 1" tube furnace (Thermo Scientific, USA). Before starting the growth process, an empty quartz tube was typically pumped to a pressure of 3 Torr and refilled with N_2, which was repeated 3 times to keep the tube clean. Next, substrates were transferred into the reactor and the growth process was started.

The growth process is schematically depicted in figure 3.2, and consists of 4 main

steps: calcination, reduction, growth, and cool down. Calcination is required to oxidize Fe and form discontinuous Fe_xO_y islands. The reduction forms metallic Fe, transforming the islands into catalyst nanoparticles that are located within a lithographically defined area. The growth is achieved by cracking carbon containing gas at high temperature. This results in carbon precipitating on the Fe nanoparticles and dissolving into it. When the carbon reaches the supersaturation point in the Fe particles, it precipitates out, forming nanotubes.

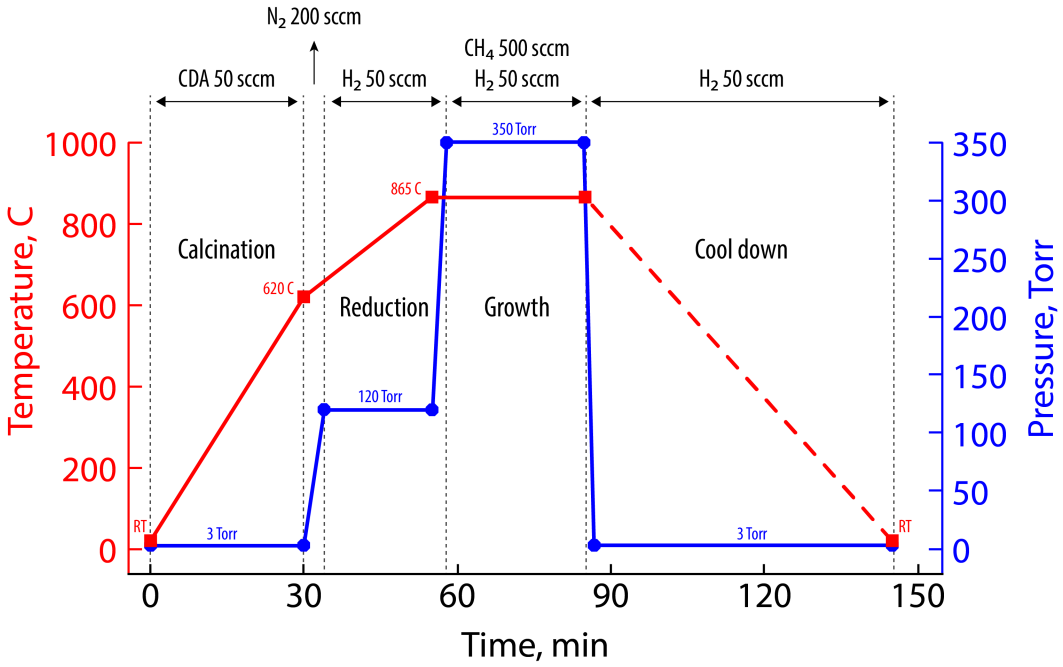


Figure 3.2. Thermal chemical vapor deposition of single-walled carbon nanotubes process diagram.

Calcination was carried out in a tube furnace flowing compressed dry air (CDA, 20% O2) at a rate of 50 sccm (standard cubic centimeter per minute), and a reaction pressure of 3 Torr. The furnace was heated to 620 °C at a rate of 20 °C/min. The total oxidation time was 30 minutes. Once a temperature of 620 °C was reached, dry air was switched to N_2 (200 sccm) to flush the tube. At the same time, the pressure controller was set to 120 Torr. When the set point was reached, N_2 was shut off and H_2 was introduced at a flow rate of 50 sccm. Flushing the reactor with inert gas is an important step that prevents a potentially dangerous oxygen and hydrogen reaction. The furnace temperature was continuously increased up to 865 °C at a ramp rate of 10 °C/min under hydrogen atmosphere. The total reduction time was 20 min. When the growth temperature of 865 °C was achieved, 500 sccm CH_4 and 50 sccm H_2 were introduced. Simultaneously, the pressure was set to 350 Torr and the reactor was kept in this condition for 30 min for CNTs to grow. After the growth

step, the furnace heating and CH_4 flow were switched off. The pressure was set to 3 Torr, and samples were allowed to cool down to room temperature under H_2 flow. Once cooled, the quartz tube was refilled with N_2, brought to atmospheric pressure, and samples were removed. The resulting nanotubes were single-walled CNTs, as confirmed by atomic force microscopy (AFM) measurements presented below.

Horizontally aligned CNT synthesis. Depending on the substrate, CNTs may grow upwards or "crawl" on the substrate, the mechanisms of which were discussed in detail in chapter 2.3.1. Two substrates were used to grow CNTs: Si wafers with a thermally grown SiO_2 layer, and ST-cut quartz. Synthesis on Si/SiO_2 resulted in randomly oriented single-walled carbon nanotubes, whereas nanotubes grown on quartz were horizontally aligned and parallel to each other.

Figure 3.3a shows SEM images of CNTs grown on an as-purchased ST-cut quartz substrate, with iron deposited everywhere on the chip, i.e. without fabricating catalyst islands. Nanotubes prepared on such substrates did not show any preferential growth direction. To improve the graphoepitaxy, quartz chips were annealed in CDA for 11 h at 900 °C. Figure 3.3b shows CNTs grown using the same CVD recipe as the previous ones. A clear preferential growth direction can be observed, although many tubes are randomly oriented. This can be attributed to iron nanoparticles on the surface of quartz that hinder aligned growth by diverting the growth trajectory. Figure 3.3c shows CNTs grown on annealed substrates using lithographically defined catalyst islands. Graphoepitaxy can be observed, with nanotubes growing parallel to each other in the quartz's [2-$\bar{1}$-$\bar{1}$0] or X direction. Randomly oriented nanotube networks can be seen within the catalyst island. Figure 3.3d shows a higher magnification image of horizontally aligned nanotubes obtained with atomic force microscopy (AFM). AFM maps were measured from 12 different regions across the sample. The misalignment was estimated to be 8.8%, i.e. the amount of tubes that did not grow in the X direction. The alignment can be further improved by optimizing the growth conditions, reaching an alignment value of 99.9% (compared to ours 91.2%) as was shown in [31]. The average CNT density was calculated to be 1.98 $\pm$ 0.43 tubes/μm. UV-lithography resolution typically allows for fabrication of 1+ μm structures, making the narrowest electrode to be in the same range. The obtained CNT density results in ~1 tube per 2 μm wide electrode, which is good enough for studying individual tube FETs. The average CNT diameter was extracted by measuring the line profiles of 20 tubes using Gwyddion software, fitting the peaks corresponding to CNTs with a Gaussian

line shape and extracting its peak value. The resulting diameter distribution was calculated to be 1.0 $\pm$ 0.4 nm, which corresponds to the expected value for single-walled nanotubes. The average diameter of our nanotubes is comparable with the data reported for nanotubes grown from similar few-angstrom-thick iron catalyst layers [140, 31].

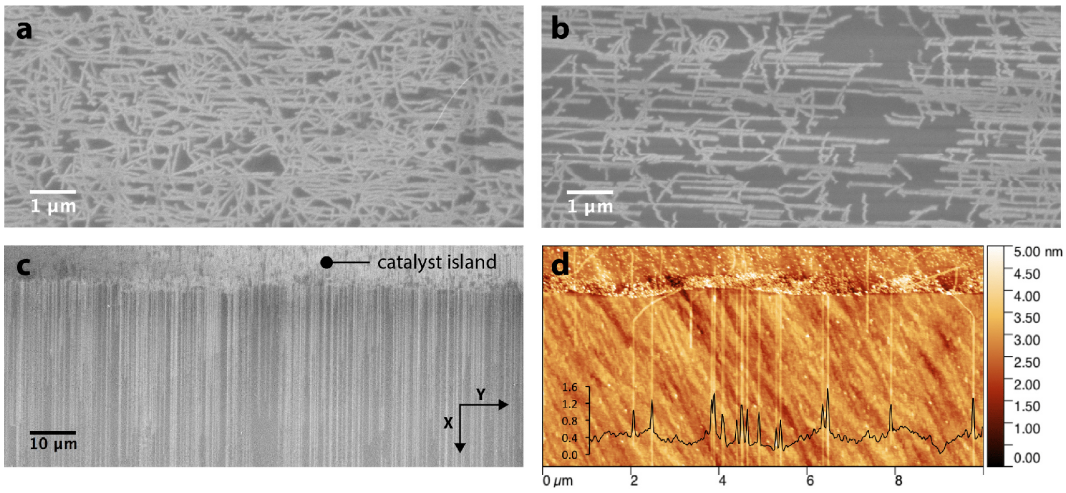


Figure 3.3. Graphoepitaxial CNTs on the surface of ST-cut quartz. CNTs grown on (a) as-purchased substrate; (b) quartz annealed at 900 °Cfor 11 h; and (c) annealed quartz with nanotubes grown from catalyst islands. (d) AFM image of horizontally aligned CNTs. Inset in (d) shows the height profile of the tubes.

3.2. Electrode integration and suspended CNT fabrication

After nanotube synthesis, source and drain electrodes were patterned. The standard ma-N 1420 lithographic recipe was used to define the electrodes. Next, Cr/Pt with a thickness of 5/60 nm were deposited at a deposition rate of 0.5/1 Å/s by e-beam evaporation. The lift off was performed in N-Methyl-2-Pyrrolidone (Remover PG, MicroChem) heated to 65 °C for 1 h. Once the metal bilayer was lifted off, samples were rinsed in IPA and dried with a N_2 gun. Figure 3.4a shows the resulting multiple devices fabricated on a single chip. The design enables fabrication of 720 source-drain electrode pairs on a 1×1 cm die. Figure 3.4b shows two FETs with a common source electrode that was fabricated on top of the catalyst island from which CNTs were grown. Figure 3.4c shows a close-up view of the source-drain region with CNTs connecting the electrodes, as well as a nanotube that did not bridge "D1" and "S" electrodes. These devices do not show preferential nanotube alignment since they were grown on a regular Si/SiO_2 substrate with an oxide thickness of 100 nm. The bottom Si can be used as a bottom gate and the transport characteristics of one of the fabricated devices are shown in figure 3.4d.

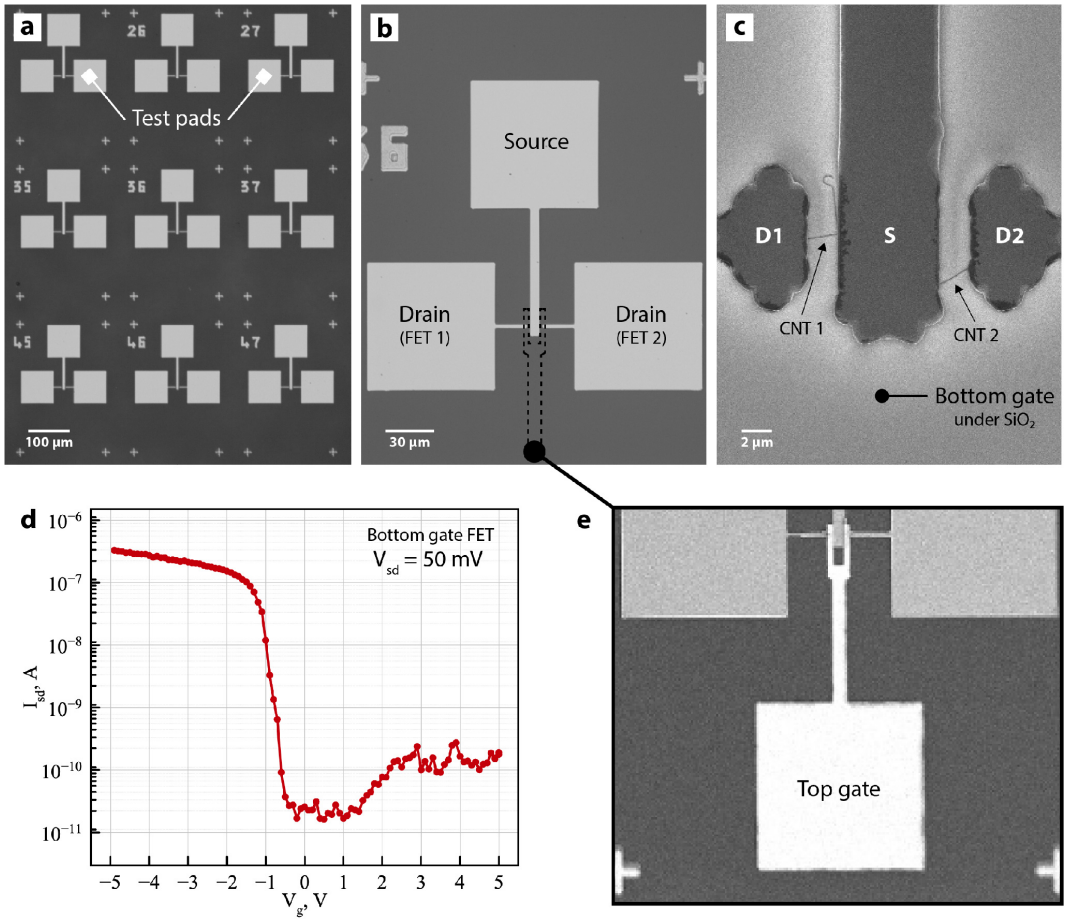


Figure 3.4. SEM images of lithographically defined electrodes. (a) Overview of multiple electrodes. (b) Close up view of two FETs with common source electrodes. Dashed line represents the future top gate electrode, SEM image of which is shown in (e). (c) Close up view of two bottom gate FETs with contacted CNTs. (d) Typical transport characteristics obtained from a bottom gate CNFET. (e) Devices after top gate deposition.

To estimate the gate modulation, the source-drain voltage was kept at V_{sd} = 50 mV, and the gate voltage V_g was swept from -5 V to 5 V while recording the change in source-drain current I_{sd}. V_{sd} was kept low to avoid burning the tube. The measurements were performed on an Agilent 4156 Precision Semiconductor Parameter Analyzer (Agilent Technologies, USA) connected to a manual probe station (Micromanipulator, USA). The resulting FET device shows p-type behavior due to the use of high work-function Pt electrodes, with a very small gate modulation within the positive V_g region. The negative branch of CNFET characteristics has an on/off ratio of 1×10^4 and a subthreshold swing of SS = 203 mV/dec. Such a relatively high SS can be attributed to the Schottky barrier between the semiconducting nanotube and the metallic electrodes as well as thick SiO_2 dielectric layer.

Figure 3.4d shows a SEM image of a top gated device that was fabricated using a standard lithography and lift off process. A dielectric layer needs to be deposited prior to the top gate formation. The details of ALD-based high-κ dielectric, as well as FET performance using it, are discussed in the next section.

Suspended carbon nanotubes. The previous section was devoted to the discussion of fabrication of on-substrate CNFETs with a bottom gate. Such a configuration does not realize the full potential of CNTs as FETs, since they suffer from unwanted interaction of the nanotubes with the substrate, which degrades device performance. To overcome this problem, suspended devices are of particular interest. Such a device is comprised of a nanotube bridging a trench, with the two sides clamped by, or lying on, electrodes (see figure 3.1, step 3). This configuration enables integration of the gate electrode around the tube to fabricate a so called "gate-all-around" (GAA) FET. This geometry provides the best electrostatics by maximizing the capacitive coupling between the gate and nanotube that are separated by a thin, high-k dielectric layer (see figure 3.1, step 5). The remaining steps of the process flow for the GAA structure fabrication is discussed below, however we were not able to measure gate modulation in GAA FET due to high leakage current in devices.

After nanotube synthesis and electrode integration, the bottom oxide layer was etched to undercut the CNT. The wet etching was performed in BOE HF (1:1 or 1:6) solution with different HF concentrations to obtain a 100 nm deep trench. After etching, samples were carefully transferred to a large beaker with DI water without drying the sample. Chips were left immersed in water for 10 minutes to dilute the HF, after which they were carefully transferred to acetone, again without allowing the liquid on the surface of the chip to dry.

The samples were dried using a critical point dryer (CPD) to avoid destruction of the structures by capillary forces. To illustrate the importance of this method, figure 3.5a shows a carbon nanotube that was dried from acetone without CPD – leaving the solution on the bench for a few hours. After the drying step, all CNTs were either broken or sagged due to the surface tension of acetone, which pulls nanotubes toward the substrate. CPD overcomes this issue by drying the delicate structure in supercritical CO_2. The suspended CNT devices were transferred into the CPD chamber filled with a solvent, after which the chamber was cooled down to temperatures below 10 °C, and the solvent was replaced with CO_2, which is liquid below 10 °C. Once the solvent is replaced with liquid CO_2, the chamber is heated to 31.5 °C or higher, increasing the pressure inside the chamber to 1072

psi (73 atm) or higher. At these conditions, liquid CO_2 becomes a supercritical fluid and has no surface tension. Once supercritical regime is achieved, CO_2 can be slowly pumped out and the chamber is brought to atmospheric pressure, allowing the delicate suspended structures to dry without collapsing. CPD is widely used for sample preparation in microscopy as well as in micro-electro-mechanical systems (MEMS).

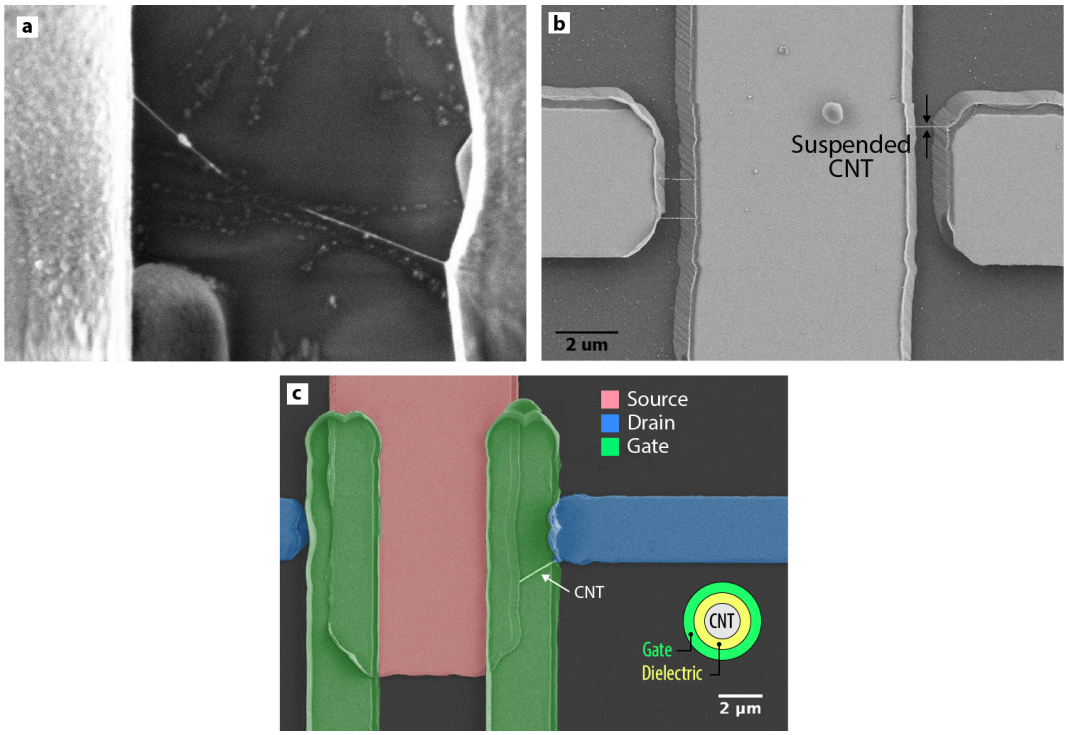


Figure 3.5. Suspended carbon nanotube fabrication. (a) CNT after etching and drying from acetone. (b) Suspended CNTs after etching and drying with CPD. (c) CNT in gate-all-around geometry.

Figure 3.5b shows CNTs etched in HF using the protocol discussed above and dried by CPD, yielding CNTs suspended across the trenches and connecting the electrodes. Suspended single-walled nanotubes are difficult to visualize under SEM. To enhance their visibility, tubes were covered with 10 nm of Al_2O_3 using ALD. As can be seen from the SEM images, the resulting ALD layer is discontinuous but serves the purpose. However, such a discontinuous film is unacceptable for GAA geometry fabrication, where high-κ dielectric has to be uniform and conformal across the entire nanotube. To achieve this a TiO_2-based pretreatment strategy was developed, which will be discussed in detail in the next section. Surface pretreatment with TiO_2 enabled the fabrication of concentric layers of Al_2O_3 (high-κ dielectric) and TiN (synthetic metal) using ALD. The alumina serves as an insulator, whereas TiN serves as gate electrode wrapped around the tube, as schematically

depicted in figure 3.1, step 5. Next, the Cr gate contact was defined using standard lithography and lifted-off in acetone (figure 3.1, step 6). This electrode was used to contact TiN underneath it, as well as a hard mask to remove TiN everywhere else on the chip. The latter was required to reduce parasitic capacitance. TiN was etched in basic piranha solution (NH_4OH:H_2O_2:H_2O) using the recipe discussed in chapter 5.2. The obtained structure was a suspended nanotube wrapped with a Al_2O_3/TiN bilayer, where the TiN layer is contacted by a Cr electrode. Figure 3.5c shows a top view SEM image of such a structure. It's important to mention that the source and drain electrodes need to be completely passivated with Al_2O_3 during ALD, so that the TiN will not be in direct contact with them or the nanotube. However, fabricated devices showed a large leakage current, the source of which still needs to be identified.

3.3. ALD thin film integration

As mentioned above, uniform ALD growth on defect-free CNTs is difficult due to a lack of growth nucleation sites. This issue is also commonly encountered during ALD growth on graphene and other pristine 2D materials. To overcome this issue, a special approach was developed for depositing uniform ALD layers on the surface of one- and two-dimensional materials.[1]

ALD was used multiple times throughout this work: to fabricate ferroelectrics, high-κ dielectrics and 2D materials. This technique is used to synthesize pinhole-free, high quality materials at relatively low temperatures, with angstrom-level control over the thickness. In addition, it is possible to uniformly and conformally coat high-aspect ratio geometries, such as deep trenches and suspended structures. During the ALD process, growth of the first few layers is a critical step. It depends not only on the chemistry of ALD precursors, but also on the surface chemistry of the substrate to be covered. The substrate surface should have reactive sites for the precursor to nucleate. If the density of nucleation sites is low, the resulting film will be discontinuous in the ultra-thin film regime. For thicker films, the islands can merge and cover the surface completely.

In this respect ALD on single-walled carbon nanotubes (SWCNTs) is a challenging process. Pristine SWCNTs are hydrophobic, inert, and typically have no defect sites (or very few), making ALD nucleation difficult. Therefore, ALD on suspended SWCNTs results in no coverage or the formation of nanospheres, originating on rare nanotube surface defects [141, 142]. Similar difficulties exist with 2D materials,

such as graphene [143, 144] and TMDs [145, 146]. These structures do not have dangling bonds or surface groups available for ALD thin film nucleation, resulting in discontinuous island grown on defects or edges of 2D materials.

CNT surface functionalization. To promote ALD growth on SWCNTs, several surface pretreatment strategies exist, also called surface functionalization. They can be classified into two groups: (1) covalent and (2) non-covalent functionalization. The first group relies on **covalent bond formation** between a functional group and the tube. This approach may create scattering centers, defects, and change the carbon hybridization from sp^2 to sp^3. The latter two effects degrade the CNT's exceptional electronic and optoelectronic properties [147, 148], so covalent functionalization is not a good choice for electronics applications of CNTs.

On the other hand, **non-covalent functionalization**, in which materials are physisorbed on the nanotube surface, is a suitable approach. It was shown that DNA [149, 150], surfactants [151] and polymers [152, 153, 154] can be used to promote ALD growth on SWCNTs. Non-covalently attached species typically do not change the carbon hybridization, but can create scattering centers and induce doping. This does not necessarily degrade the SWCNT properties, but may alter its electron transport properties. For example, gas phase NO_2 was used to functionalize the surface of suspended nanotubes [155] and graphene [156, 157]. It was shown that NO_2 can physically adsorb on these materials and react with Al_2O_3 ALD precursors to form a thin intermixed layer, followed by pure ALD material. Although, NO_2 and other materials listed above provide sufficient nucleation sites and the final ALD thin film is uniform and conformal, it is not a pure oxide material. This is important if the functionalization and ALD dielectric layers are used in FET gate stack, since the functionalization layer may reduce the overall dielectric permittivity.

In this context, CNT surface pretreatment using oxides, or materials that can be subsequently oxidized, seems promising since together with the ALD layer, they can compose an all-oxide gate dielectric. One of the few metals that form uniform layers on CNTs, and at the same time can be easily oxidized, is titanium. It was shown that Ti has good wetting to carbon nanomaterials, forming continuous layers [158].

To study the pretreatment-layer assisted nucleation on the surface of suspended SWCNTs, ALD Al_2O_3 – a widely used high-κ dielectric – was chosen. For this, suspended nanotubes were synthesized across 1 - 1.5 μm wide microfabricated trenches or silicon nitride TEM membrane holes (dia. 1 μm), using the CVD process

discussed previously. Next, some of the samples were covered with metallic Ti by thermal evaporation at a deposition rate of 0.1 Å/s and a pressure of better than 5×10^{-6} mbar. Next, the Ti layer was oxidized to TiO_2 under ambient conditions by leaving the samples in air for 24 h.

TiO_2 pretreatment: TEM and SEM studies. Figure 3.6a shows SEM images of CNTs suspended across trenches and coated with 10 nm of Al_2O_3, without (left) and with (right) a TiO_2 pretreatment layer. As expected, alumina layers on CNTs without pretreatment were discontinuous, whereas nanotubes pretreated the TiO_2 layer were covered completely and reproducibly. To study suspended nanotube coverage with oxides in further detail, transmission electron microscopy (TEM) measurements were performed on a JEOL 2100F TEM (JEOL Ltd., Japan) at an accelerating voltage of 120 or 200 kV. Figure 3.6b shows a TEM image of a nanotube covered with 10 nm of Al_2O_3 only, confirming the difficulties associated with ALD nucleation on pristine nanotubes. When Ti with a nominal thickness of 3 nm was deposited and oxidized to form TiO_2, the titania seed layer provided a sufficient amount of nucleation sites for subsequent ALD synthesis of 10 nm thick Al_2O_3, resulting in continuous but non-uniform and slightly rough coverage (figure 3.6c). To improve the uniformity, 5 nm of Ti was nominally deposited and oxidized, followed by ALD alumina deposition. Figure 3.6d shows the resulting bilayer thin film, revealing the morphology of the coating is continuous, uniform, and conformal to the nanotube. The tooling factor (i.e. what fraction of the thickness measured with quartz crystal monitor or the nominal thickness, corresponds to the actual thickness of the film) of the deposition system that was used to grow Ti was $\times0.6$. The expected Ti volume increase after oxidation is $\times1.6$, so the nominal Ti thickness translates into TiO_2 thickness as ~1:1.

Figure 3.6d and f show TEM images of nanotubes covered with TiO_2-only, formed by oxidizing 3 nm and 5 nm thick Ti, respectively. These images indicate that the alumina non-uniformity observed in figure 3.6c originates from the non-uniformity of the seed titania layer, the thickness of which varies within a few nanometers. As can be seen, slightly increasing the initial Ti thickness helps to significantly reduce the non-uniformity, which was investigated by rotating the tubes along their longitudinal axis. Figure 3.6g and h show the nanotubes from figure 3.6c and d respectively, rotated to different angles, which confirmed continuous and conformal coating of the tubes. A high magnification image of the tube in figure 3.6h is given in figure 3.6i, revealing the uniform, amorphous coverage with titania and ALD alumina.

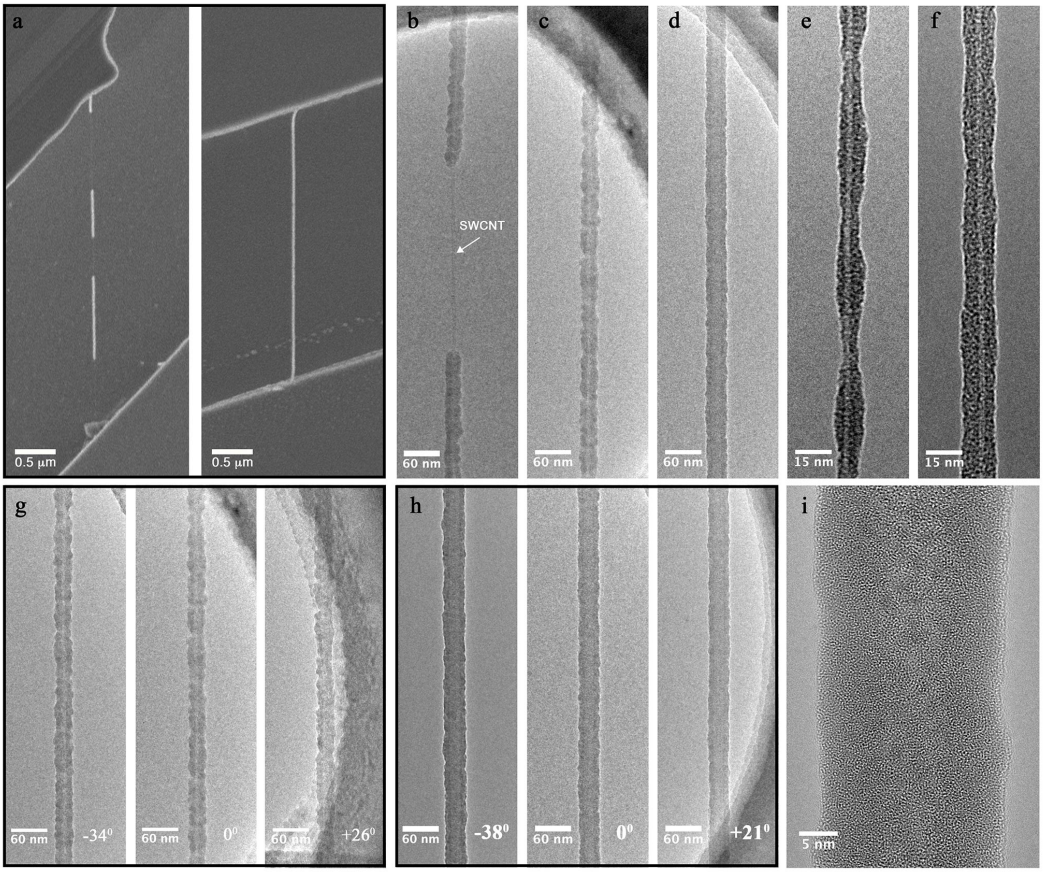


Figure 3.6. Morphology of thin films deposited on suspended SWCNTs. (a) SEM images if nanotubes covered with Al_2O_3 without (left) and with (right) TiO_2 seed layer. (b-i) TEM images of CNTs with (b) 10 nm of Al_2O_3 only; (c) 3 nm of Ti converted to TiO_2 and covered with 10 nm Al_2O_3; (d) 5 nm of Ti converted to TiO_2 and covered with 10 nm Al_2O_3; (e) 3 nm of Ti converted to TiO_2 only; (f) 3 nm of Ti converted to TiO_2 only; (g) 3 nm of Ti converted to TiO_2 and covered with 10 nm Al_2O_3 rotated along the nanotube axis; (h) 5 nm of Ti converted to TiO_2 and covered with 10 nm Al_2O_3 rotated along the nanotube axis;(i) high magnification image of the CNT in (h). This figure is reprinted from an open access article [159] based on CC BY license.

Both seed layers showed continuous coverage, providing enough nucleation sites for complete passivation by ALD Al_2O_3. Due to a high binding energy, Ti has good wetting behavior [160] on the CNT surface, forming a continuous film. Also, titanium has a large Pilling-Bedworth ratio (PBR), i.e. the ratio between the volume of metal oxide to the volume of corresponding metal, of $PBR_{Ti} = 1.6$ [161], which results in an increase in size after oxidation, further increasing the coverage. Theoretical calculations show that Ti has a very strong interaction with carbon, forming a covalent bond with CNTs and graphene [162, 163, 164], which is, as discussed previously, an undesirable effect. However, according to density functional theory (DFT) calculations, Ti favors the reaction with O_2, oxidizes

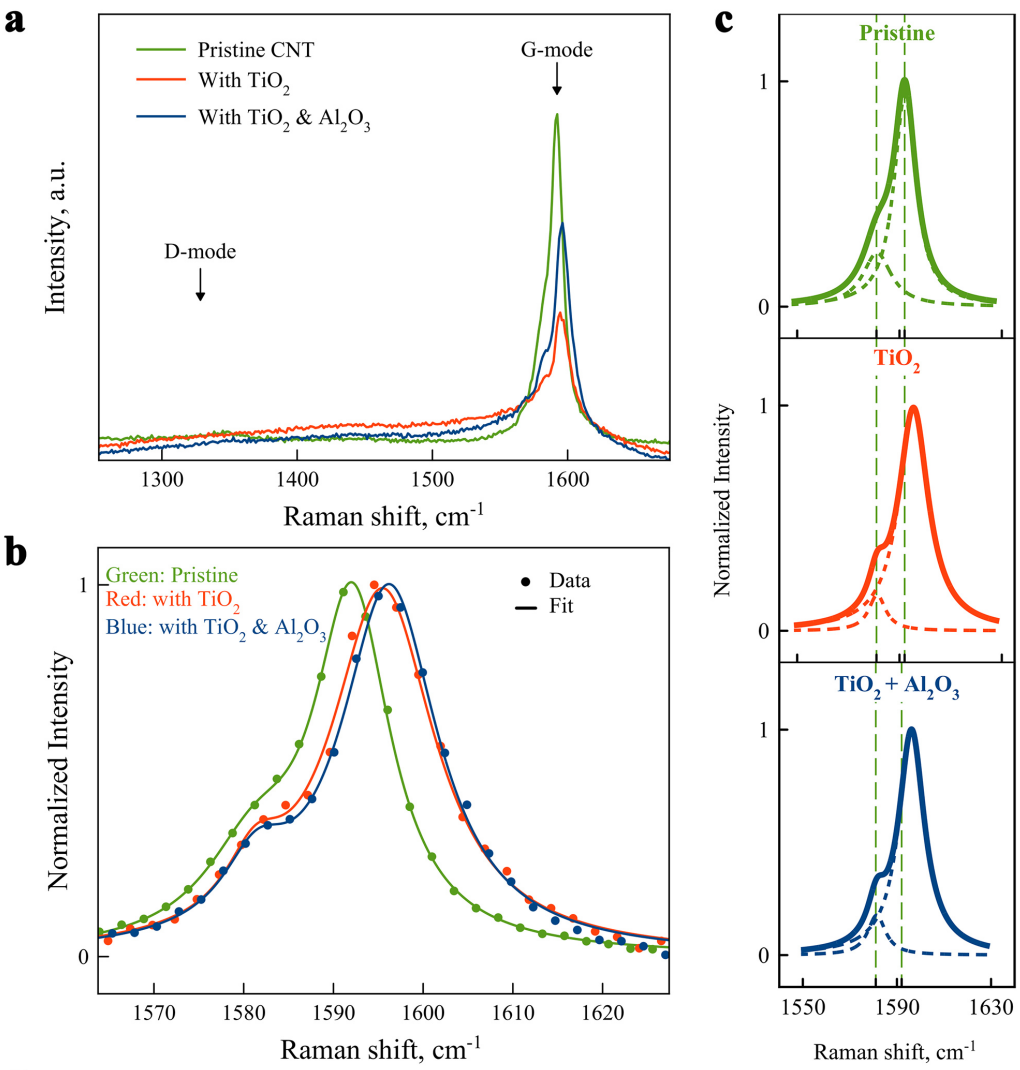
very fast, and during oxidation weakens its interaction with carbon [165, 166]. These calculations allow us to speculate that upon oxidation, the newly formed TiO_2 layer weakly interacts CNTs. This hypothesis is supported by Raman and electrical measurements presented below, and to the extent that these techniques are able to provide such information, they show no degradation of the nanotube properties.

Titania-alumina bilayer impact on the phonon properties of CNTs. Next, we studied the effect of the TiO_2 pretreatment and ALD layers on phonon properties of CNTs. For this, Raman spectroscopy was performed on coated and not-coated suspended CNTs. CNTs possess a number of Raman modes. For this study, the most interesting ones are the D- and G-modes. The D-mode allows a qualitative analysis of the degree of disorder in CNTs, providing an estimate of the amount of surface defects. The absence of the D-mode, or its low intensity compared to the G-mode ($I_G/I_D > 100$), is an indicator of a high-quality material. The G-mode consists of G^+ and G^- modes responsible for carbon atom vibrations in the longitudinal and circumferential directions, respectively. The G mode is sensitive to mechanical stress and doping.

Figure 3.7a shows Raman spectra of as obtained and coated nanotubes. The D-mode, expected to be at around 1320 cm^{-1}, is not observed (possibly at the noise level), which allows us to conclude that the initial nanotube is defect-free (or low defect), and no defects were introduced after the deposition of both TiO_2 and Al_2O_3, suggesting that the CNT surface preparation technique does not degrade the nanotube quality.

On the other hand, there were some noticeable changes to the G-mode. To study these changes the G-mode was normalized and fitted with two Lorentzian curves to extract the G^+ and G^- modes positions. Figure 3.7b shows the resulting fit, and figure 3.7c shows decoupled G^+ and G^- modes. As can be seen, after the deposition of TiO_2, the G^+ modes blueshift relative to the pristine tube. Subsequent deposition of Al_2O_3 results in further small G^+ mode shift towards higher wavenumbers. The table in figure 3.7d summarizes the extracted peak positions. We hypothesize that the observed shifts can be attributed to the mechanical stress induction and/or doping effect. Both mechanisms are well studied in carbon nanotubes. Mechanical confinement from coating results in strain, which shifts the G-mode. The extent of this shift depends on chirality, specifically C–C bond elongation [167]. CNT doping induced Raman shifts result from the charge transfer between attachments,

or between the coating and the tube [168].



d

Process step	G⁻ mode, cm^{-1}	G⁺ mode, cm^{-1}
Pristine	1581	1592
With TiO_2	1581	1595
With TiO_2 and Al_2O_3	1581	1596

Figure 3.7. Raman spectroscopy of a pristine nanotube and a nanotube coated with TiO_2 and Al_2O_3. (a) As-obtained spectra. (b) Normalized G-mode fitted with two Lorentzian functions. (c) $G^+$and G^-modes shifts. (d) Summary of coating induced G-mode changes. This figure is reprinted from an open access article [159] based on CC BY license.

3.4. Titania-alumina all-oxide high-κ dielectric

Previous measurements and discussions were made with an assumption that metallic Ti was oxidized after exposing it to ambient environment. To confirm this, X-ray

photoemission spectroscopy (XPS) was performed on a Thermo Scientific K-Alpha XPS, using a monochromatic Al Kα X-ray source ($h\nu$ = 1486.7 eV). The flood gun was used to minimize charging effects, and the C1s carbon peak was used as a reference to accommodate for charging and shift in the spectrum. To achieve good signal-to-noise ratio, a TiO_2 thin film was fabricated on Si/SiO_2 substrate by evaporating 5 nm of Ti and oxidizing it under the same conditions as the CNT samples.

Figure 3.8a shows the high resolution XPS spectrum of the Ti 2p region. Two main peaks at 458.5 and 464.3 eV correspond to Ti $2p_{3/2}$ and Ti $2p_{1/2}$ respectively, and can be attributed to Ti^{4+} with TiO_2 stoichiometry [169]. No peak was detected at 453.86 $\pm$ 0.32 eV, corresponding to metallic Ti [169], which confirms that Ti oxidation in air was successful. This is especially important for TiO_2 integration into FET gate electrode stacks, since incomplete oxidation may result in source-to-drain and/or increased gate leakage currents through a metallic conduction pathway.

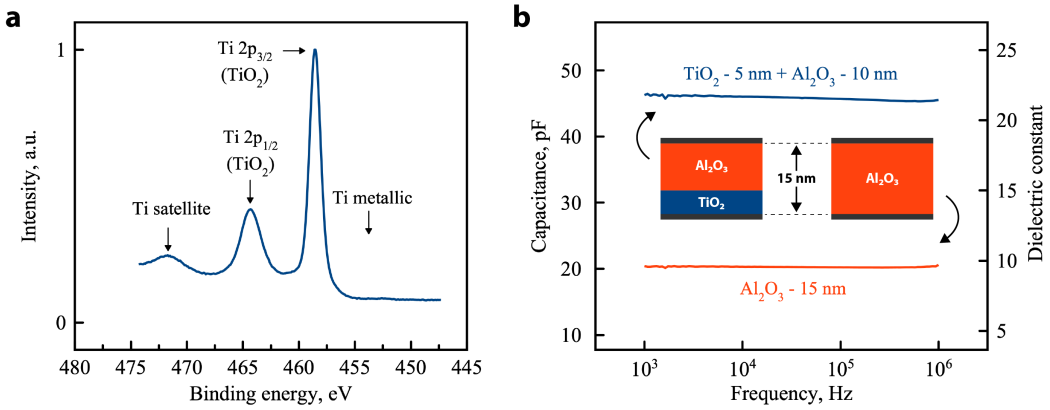


Figure 3.8. Chemical composition and dielectric properties. (a) XPS measurement of Ti thin film oxidized to TiO_2, revealing no metallic inclusions and complete oxidation. (b) Dielectric constant enhancement in compound titania-alumina gate oxide. Inset in (b) schematically represents MIM capacitor that was fabricated to measure dielectric properties. This figure is adapted from an open access article [159] based on CC BY license.

After confirming TiO_2 formation with XPS, titania was integrated into a metal-insulator-metal (MIM) capacitor structure to compare the dielectric properties of compound TiO_2-Al_2O_3 dielectric, with pure Al_2O_3 dielectric. For this, two capacitors were fabricated, as schematically shown in figure 3.8b: (1) with 15 nm ALD Al_2O_3 only; and (2) with 5 nm TiO_2 (oxidized Ti) and 10 nm ALD Al_2O_3. The total oxide thickness and area of both devices was kept the same and were equal to d = 15 nm and A = 6.4 $\times$ 10^3 μm^2, respectively. The dielectric measurements were performed on a Keysight E4990A Impedance analyzer (Keysight Technologies, USA) by obtaining capacitance-frequency characteristics in the frequency range

from 1 kHz to 1 MHz at an amplitude of 0.01 V. Figure 3.8b shows the measurement results, revealing a twofold increase in capacitance of the device with a titania-alumina stack (45.8 $\pm$ 0.3 pF), compared to a pure alumina one (20.3 $\pm$ 0.1 pF), although the oxide thickness and capacitor electrode area of both devices are the same. By using a parallel-plate capacitor geometry calculation, the compound oxide shows a dielectric constant of $\kappa_{Al_2O_3+TiO_2} = 21.7$, whereas pure alumina has a dielectric constant of $\kappa_{Al_2O_3} = 9.4$. Both κ values were extracted at 1 MHz. Such an increase in overall dielectric constant can be explained by a very high dielectric permittivity of TiO_2. In this context, one would recommend using pure TiO_2 as a high-κ dielectric, however it has a relatively small bandgap ($E_{TiO_2} = 3.5$ eV), which will result in thermionic emission and direct current tunneling leading to an increased gate leakage [170]. This is especially important for sub-10 nm thin films. Thus, for few-nanometer thick gate oxides, TiO_2 should be used together with another high-κ dielectric with sufficiently large bandgap, such as Al_2O_3 ($\kappa_{Al_2O_3} = 9$, $E_{Al_2O_3} = 8.8$ eV), HfO_2 ($\kappa_{HfO_2} = 25$, $E_{HfO_2} = 5.8$ eV), or others [170]. In order to obtain high overall dielectric permittivity, while keeping the leakage current low, an optimal thickness and combination of oxides should be found.

The (*EOT*) of the fabricated oxides was calculated using the following equation:

$$EOT = \frac{\varepsilon_0 \varepsilon_{SiO_2} A}{C_{ox}}, \tag{3.1}$$

where ε_0 and ε_{SiO_2} are vacuum permittivity and dielectric constant of SiO_2, respectively; and A and C_{ox} are area and capacitance of the capacitor with an oxide of interest, respectively. For the pure alumina device, an *EOT* of 6.2 nm was extracted, whereas for the titania-alumina-based capacitor, it was found to be 2.7 nm. Such a scale down of the *EOT* shows that titania can be used to improve the dielectric strength of a gate oxide, and can be successfully used together with ALD-based nanomaterials. Although the synthesized titania-alumina high-κ dielectric shows promising results, the ratio of oxide thicknesses, the quality of the interface between them, and other material combinations should be studied further.

To further test the titania-alumina compound dielectric, two devices were fabricated: (1) back-gated and (2) top-gated CNFETs. The former was used to study how coating with oxides impacts the transport properties of the transistor, while the latter was used to directly evaluate the TiO_2-Al_2O_3 as a gate dielectric.

The back-gate CNFET was fabricated on a degenerately doped Si substrate (ρ = 0.001-0.005 $\Omega \times$ cm) with 100 nm thick thermal oxide, using the fabrication process discussed previously. The CNFET was characterized in three configurations: in its pristine condition - directly following fabrication; after TiO_2 (oxidized Ti) coating, and after TiO_2 with ALD Al_2O_3 coating. The corresponding transport characteristics are shown in figure 3.9a, revealing an on/off ratio of ~10^4. No conductance degradation was observed after deposition of TiO_2 or Al_2O_3. The transistor in its pristine state, shows p-type conduction due to the high-work function of Au used for the electrodes and shifts towards negative gate voltages, becoming more p-type after oxide deposition. The I_{sd}-V_g curve after Al_2O_3 deposition, shows a slightly improved on/off ratio with lower I_{on} and higher I_{off}, which can be attributed to contact annealing during the prolonged ALD step, performed at 300 °C.

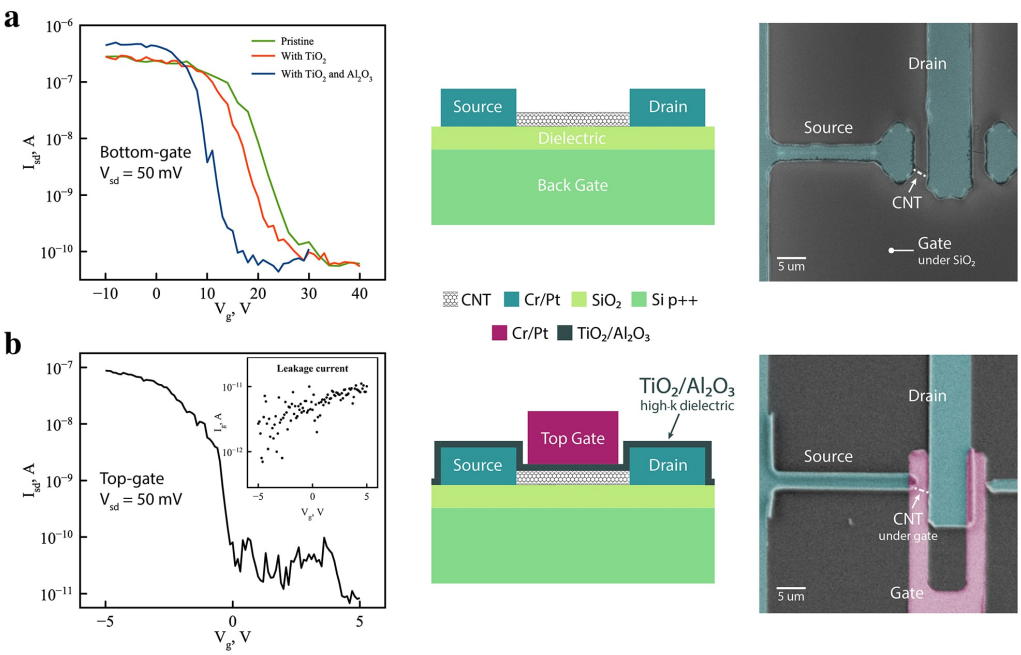


Figure 3.9. Electron transport properties of CNFETs. (a) Transport characteristics, schematic illustration and top-view SEM image of the back-gated FET measured in pristine condition (green), and after coating with TiO_2 (red) and Al_2O_3 (blue). (b) Transport characteristics, schematic illustration and top-view SEM image of the top-gated FET fabricated using TiO_2-Al_2O_3 high-κ dielectric. This figure is reprinted from an open access article [159] based on CC BY license.

Figure 3.9b shows the transport characteristics of the top-gated CNFET, which similar to the previous device, shows p-type behavior but with significantly improved threshold voltage. The on/off ratio of the device is ~10^4 and the field

effect mobility was calculated using the following equation:

$$\mu_{FE} = g_m \times \frac{L^2}{C} \times \frac{1}{V_{sd}}, \tag{3.2}$$

where g_m, L and C are the transconductance, device length, and capacitance, respectively [46]. The capacitance was calculated as follows:

$$\frac{C}{L} = \frac{2\pi\varepsilon_0\varepsilon_{ox}r}{2t_{ox}}, \tag{3.3}$$

where ε_0 is the vacuum permittivity, ε_{ox} is the dielectric constant of the oxide extracted from *C-f* measurements (figure 3.8), t_{ox} is the oxide thickness, and r is the radius of the CNT. The extracted field effect mobility μ_{FE} = 226 cm^2/Vs is comparable with those reported in literature. It is important to mention that the field effect mobility is device specific and depends on many factors, including contact resistance, surface roughness, measurement parameters, and other parameters. The inset in figure 3.9b shows the gate leakage current, which is at least one order of magnitude lower than source-drain current and was limited by the sensitivity of the measurement setup. The low leakage current, in addition to the estimated *EOT*, show that the developed titania-alumina bilayer is a promising all-oxide high-κ dielectric for use in FET gate stacks.

Notes

[1]The results presented in this and subsequent sections of this chapter have been published in [159]. Some of the ideas were are also discussed in [171].

4. Lithographically defined synthesis of transition metal dichalcogenides

In this chapter we present a novel lateral conversion technique, used to grow few-layer thick WS_2, WSe_2, MoS_2 and $MoSe_2$ van der Waals materials[2]. In this technique; first, a multilayer structure is fabricated with ALD-deposited metal-oxide (e.g. WO_x) sandwiched between two SiO_2 layers, and then the structure is dry etched to expose the edges of the oxide. Next, the metal-oxide layer is converted into TMD material through chalcogenation that starts at the exposed edges, and proceeds laterally inside the buried oxide layer, converting it into metal-sulfide (e.g. WS_2) or -selenide (e.g. WSe_2). The technique enables wafer-scale synthesis of lithographically patterned, highly-ordered layered TMD materials with few-layer precision. The sections below discuss the details of the lateral conversion technique, and present Raman, SEM, TEM, and other characterization results.

4.1. Wafer-scale WS_2 synthesis

Lithographic patterning. To realize the lateral conversion of metal-oxide to metal-sulfide, WO_x-to-WS_2 transformation was chosen as a model reaction. For this, WO_x was grown by ALD on Si substrates with 250 nm SiO_2 thermal oxide, in an Oxford FlexAl ALD at 300 °C. Bis(tert-butylimino)bis(dimethylamino)tungsten(VI) and O_2 plasma were used as the tungsten and oxygen precursors, respectively. An *in situ* ellipsometer was used to measure the deposition rate, which was calculated to be in the range between 0.45 and 0.5 Å/cyc. After WO_x growth, substrates were covered with SiO_2 in ALD without breaking the vacuum to preserve a high-quality clean interface between the materials. A ~5 nm thick film of silica was grown at a deposition rate of 0.5 Å/cyc, using tris(dimethylamino)silane and O_2 plasma as the silicon and oxygen precursors, respectively. Since it has a significantly higher growth rate compared to

ALD, samples were covered with an additional 50 nm of SiO_2, using an Oxford 80+ plasma enhanced CVD (PECVD) system. The additional SiO_2 layer was deposited to ensure the silica was thick enough to eliminate diffusion of the chalcogen containing gas through it during the conversion step. The growth was performed at 350 °C, using a 10 W plasma consisting of 1% SiH_4 in Ar and N_2O, introduced at flow rates of 1182 sccm and 710 sccm, respectively.

Once the WO_x/ALD-SiO_2/PECVD-SiO_2 multilayer stack was deposited on the Si/SiO_2 wafer, it was patterned us thing the standard ma-N 1420 lithographic recipe, and dry etched in an Oxford 80+ reactive ion etching (RIE) system with Ar + CHF_3 (25 sccm + 35 sccm, 100 W, 30 mTorr), to a depth of ~100 nm. The left image in figure 4.1a schematically illustrates the etching process and the resulting structure, which consists of a WO_x layer with exposed edges, sandwiched between two SiO_2 layers. After etching, the photoresist was removed in hot acetone at 50 °C using ultrasonication. To ensure complete removal of photoresist residues and fluoropolymer, which can form on the trench sidewalls during dry etching, samples were annealed in O_2 plasma (50 sccm, 150 W, 100 mTorr) for 10 min. To avoid chalcogen precursor reaction with the silicon substrate, the backside and exposed chip edges were covered with ~50 nm thick PECVD-SiO_2 by loading samples in the reactor upside down. More details about the fabrication can be found in Appendix A2.

Chemical conversion process. Next, WOx was chemically converted to WS_2 using a two-step process, consisting of (1) reduction and (2) chalcogenation. Both steps were performed in a MTI Crystal 1200x-RTP-4 tube furnace reactor.[3] The reduction step was performed by annealing samples in an Ar/H_2 gas mixture, flowing at a rate of 1000/50 sccm, at atmospheric pressure, and temperatures ranging from 650 to 750 °C. Depending on the experiment, reduction time was up to 2 h. After the WO_x reduction to metallic W, it was sulfidized by introducing H_2S at a flow rate of 25 sccm into the Ar/H_2 mixture. The reaction was carried out at a pressure of 100 Torr, and at temperatures ranging from 650 to 850 °C. The conversion time was varied depending on the experiment. After the chemical conversion step was finished, the reactor was pumped down to base pressure, refilled with Ar, and allowed to cool to room temperature.

Control over the TMD shape. Figure 4.1a and b show schematic illustrations and corresponding true-color, white light reflection microscopy (WLRM) images for each major fabrication step. The WLRM images were obtained on a Leica

DM2500-M microscope.[4] The difference in colors of WO_x, W and WS_2 are due to changes in thickness and refractive index of the materials. For the sample in the right image in figure 4.1b, the chalcogenation was intentionally stopped before sulfidizing the entire sample, to visualize the color difference between WS_2 and W. The observed dark blue ring, around the etched hole (appears white in the image), shows the converted region, with WS_2 buried under the SiO_2 layer. The concentric ring also confirms that the conversion took place only around the lithographically defined hole and that the silica layer was thick enough (total thickness – 55 nm) to eliminate H_2S diffusion through the top of the film. This demonstration shows that the conversion starts at the edges and proceeds laterally, forming TMD material. Figure 4.1c shows another set of WLRM images of the arbitrarily patterned samples, with the same initial WO_x thickness, but different conversion times. From these images, it can be clearly seen that the **extent of lateral conversion (ELC)** can be controlled by the reaction time, and that the resulting materials can be of any arbitrary shape. The ELC can be also controlled by the reactor temperature. The reaction kinetics (i.e. time and temperature dependence) will be discussed in detail in the next section.

Control over the TMD thickness. Because the optical and electronic properties of TMDs are highly sensitive to the number of layers present in these films, it is important to control this parameter in these materials. Practically, we were able to tune the number of layers by using the ability of ALD to precisely control the WO_x deposition thickness, which were subsequently converted to the chalcogenide. To show that the developed lateral conversion technique enables control over the number of TMD layers, cross-sectional TEM measurements were performed.[5] The cross-section samples were milled using a FEI Helios G4 UX dual beam, focused ion beam (FIB). For this, the sample surface was covered with amorphous carbon or platinum using electron beam induced deposition. After milling the region of interest, substrates were thinned to 10-50 nm cross sections.

Figure 4.1d shows cross-sectional TEM images of 5 samples with different initial WO_x thickness – converted using the same reaction parameters. The WO_x thickness was varied from 2.5 to 9.6 nm (top to bottom). The TEM images reveal that the converted films consist of distinct Van der Waals WS_2 layers with an interlayer spacing of ~6.2 Å, which matches the lattice spacing of WS_2 in the *c*-direction. To extract the number of layers for each of the 5 samples, TEM images were obtained at 30 spots along a 10 μm cross-section. The graph in figure 4.1d shows the results, revealing a linear dependence of the number of WS_2 layers on the thickness of the

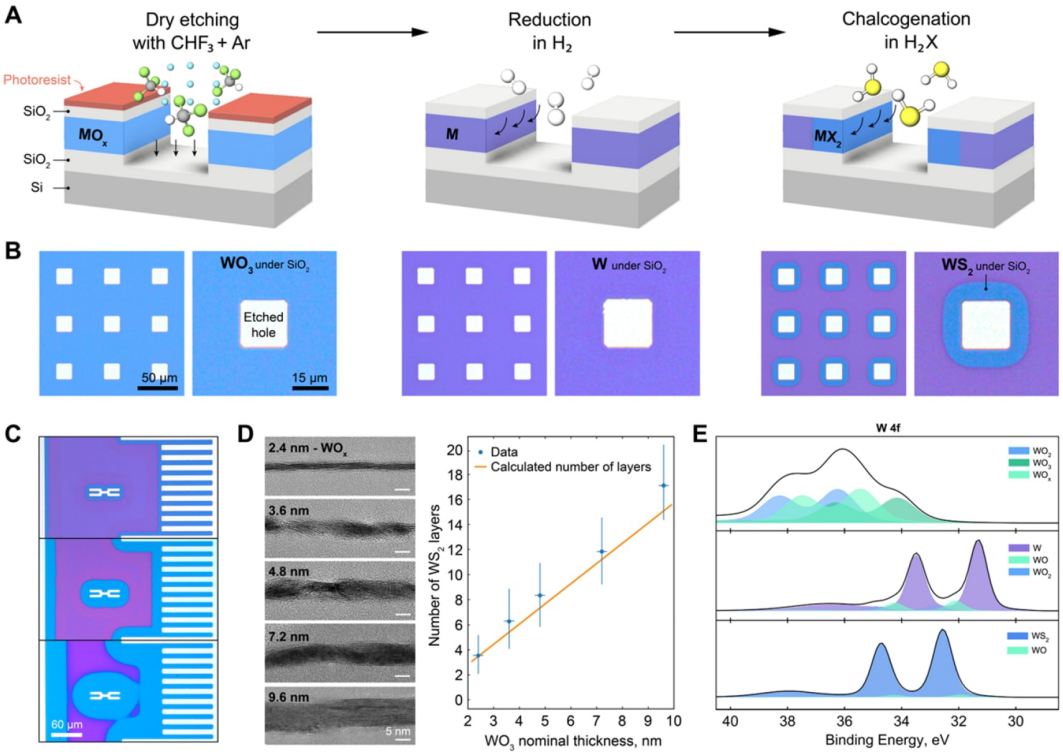


Figure 4.1. Lithographically defined WS_2 grown using lateral conversion technique. (a) Schematic illustration and (b) corresponding WLRM images at each conversion step. (c) WLRM images of WS_2 converted for different amount of time, demonstrating the control over ELC and the ability to fabricate structures of any arbitrary shape. (d) Cross-sectional TEM images of WS_2 converted from WO_x with thickness ranging from 2.4 to 9.6 nm. Graph on the right side demonstrates the ability to control the number of layers. (e) XPS measurements showing the composition of oxide synthesized using ALD and its successful reduction to W and conversion to WS_2. This figure is reprinted from an open access article [159] under the terms of the Creative Commons Attribution 3.0 license.

initial ALD-deposited WO_x. The error bars show the span of the number of layers, revealing that it can be controlled with a $\pm$ 1 layer precision for the thinnest sample. The dependence also shows excellent agreement with the predicted/calculated number of layers (orange line). The lattice spacing was measured to be ~6.2 Å that closely matches to the lattice spacing of pristine WS_2.

Elemental analysis. XPS measurements were performed to confirm the elemental composition of the samples at each step of the conversion process. Depth profiling was used to precisely remove the top SiO_2 layer and reach the layer of interest, taking care to not to sputter it or to change its chemistry. Figure 4.1e demonstrates the W 4f region for the WO_x film, as-deposited (top), after reduction (middle), and after sulfudization (bottom). The as-deposited film shows peaks corresponding to WO_2, WO_3, and an intermediate oxidation state, which indicate that the ALD-deposited WO_x is a complex oxide. After reduction, the XPS spectrum changed significantly;

the WO_x peaks mostly disappeared, and two strong peaks at 31.6 eV and 33.6 eV emerged, corresponding to metallic W. In this sample, the oxide content was estimated to be less than 8%. After the conversion step, the peaks shifted to 32.4 eV and 34.2 eV, which can be attributed to WS_2, with a small peak indicating less than 2% residual WO_x. Thus, XPS measurements confirm the composition of the buried layer at each step, showing successfful transformation of WOx to W to WS_2 using reduction and chalcogenation, respectively.

4.2. High-resolution Raman spectroscopy of WS_2

Due to the changes in color of the converted films discussed earlier, light microscopy provides a quick and easy way to estimate the ELC, and was routinely used to study the conversion results and adjust synthetic parameters for subsequent experiments. To validate this quick screening methodology, and to provide additional information, such as TMD quality, thickness and orientation, Raman spectroscopy – another optical technique – was used [172]. In this work, high resolution Raman spectroscopy maps were obtained on a custom microscope, based on a Nikon Eclipse Ti inverted microscope, equipped with a 532 nm laser that was focused to a diffraction limited spot with a Nikon 100× 0.95 NA objective.[6] Samples were scanned with a MadCityLabs Piezo scan stage, while recording the signal with an Acton 2300i spectrometer – equipped with an 1800 grooves mm^{-1} grating, and a Princeton Instruments PIXIS CCD.

Raman intensity correlation with WS_2 quality. Figure 4.2a shows WLRM (left column) and high-resolution Raman images (right column), obtained for converted samples with an initial oxide thickness ranging from 2.4 nm to 9.6 nm. The Raman maps represent integrated signal of the WS_2 spectra. As can be seen, the ELC extracted from both optical measurement techniques are in good agreement. Three distinct regions can be observed in the Raman maps of the three thickest samples, which are demarcated for the 4.8 nm sample. The Raman intensity is the highest and the most uniform in the first region (closest to the etched hole) and can be attributed to continuous WS_2 material. The second region has a slightly lower intensity with a slightly higher intensity variation, which tells us that the quality of the material is decreasing, and non-converted metallic W may be present in this region. The third region has the lowest intensity, decaying deeper inside the sample (in the lateral direction), which indicates that it mostly consists of unreacted material and small inclusion of WS_2. These observations are consistent with a diffusion driven reaction mechanism, and further confirms that the reaction proceeds laterally inside

the sandwiched layer.

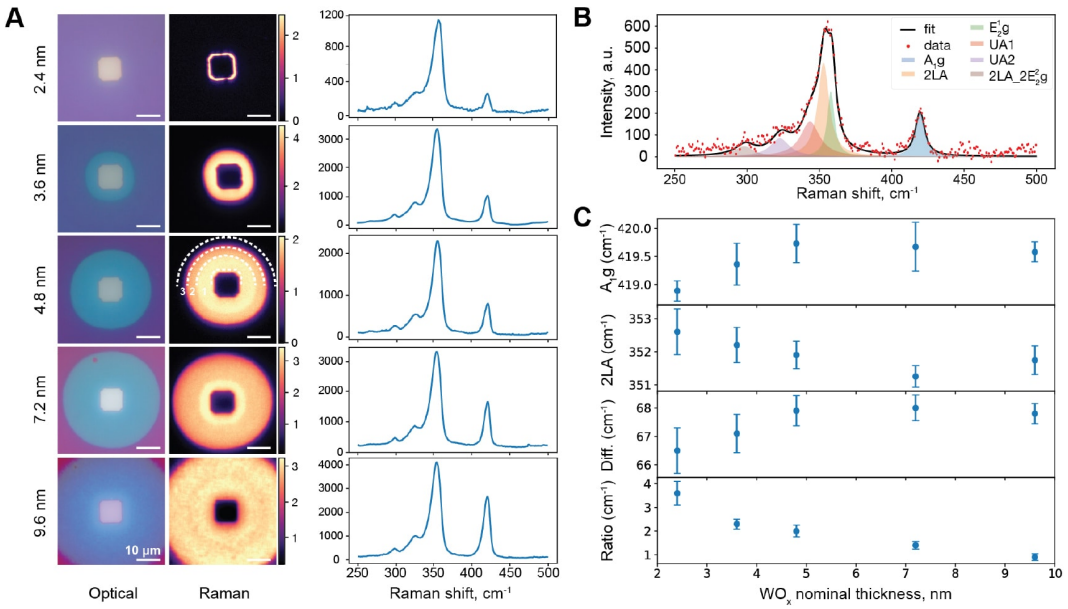


Figure 4.2. High-resolution Raman spectroscopy of WS_2. (a) WLRM images and Raman intensity maps with corresponding average Raman spectrum for WS_2 of different thickness. (b) A representative Raman spectrum, demonstrating the extracted WS_2 Raman modes. (c) A_1g and $2LA$ modes evolution as a function of the WO_x nominal thickness, revealing its direct impact on thickness of the final WS_2. This figure is reprinted from an open access article [159] under the terms of the Creative Commons Attribution 3.0 license.

Raman modes evolution. Graphs in the right column of figure 4.2a, represent an average Raman spectrum for each sample. Each spectrum consists of multiple WS_2 Raman modes, among which A_1g, E_2^1g, and $2LA$ modes have the highest contribution. They originate from out-of-plane sulfur oscillations, in-plane W and S displacement, and the longitudinal acoustic mode from the M point of the Brillouin zone, respectively. These, and other WS_2 Raman modes, overlap with each other, but their peak positions and intensities can be accurately extracted by fitting the experimental data with multiple Lorentzian line shapes. Figure 4.2b shows a representative Raman spectrum fitted using this method, which was also done for each point (pixel) in the acquired Raman maps. The values were plotted as a function of WO_x thickness and presented in figure 4.2c. A number of interesting observations can be made by studying the evolution of A_1g and $2LA$ modes. It has been shown that, as the number of layers in mechanically exfoliated WS_2 are decreased, the $2LA$ to A_1g ratio increases, while the distance between the peaks decreases [173]. Raman modes observed for our samples, show the same trend, from which it can be concluded that the number of layers in the final WS_2 film is defined by the thickness of the initial WO_x film deposited by ALD.

4.3. Structural characterization of buried WS_2

Raman spectroscopy and WLRM, are relatively rapid methods for characterizing TMD materials, which provide information about their general quality, and morphology. However, diffraction-limited optical characterization typically cannot provide information on single-grains, or structure at the atomic level. In this regard, TEM studies help to obtain information with atomic level detail; although this technique is time-consuming, especially when intricate sample preparation, such as FIB milling of lamellas, is required. Figure 4.3a shows WLRM image (left), Raman map (center) and SEM image (right) of the part of the sample that was used for cross-sectional TEM measurements. WLRM and Raman microscopy were used to identify the region of interest. The SEM image shows sites, from which two, ~14 μm long lamellas, labelled as "FIB 1" and "FIB 2" on the figure, were milled out. Next, these lamellas were thinned to 10-50 nm thickness and studied under TEM. The corresponding images are shown in figure 4.3b and c. Three regions were identified, which are labeled numerically and color coded: red, green, and blue. These regions are also shown on the SEM image in figure 4.3a (right).

Panoramic TEM images, shown in figure 4.3b and c, consist of six high-resolution TEM (HRTEM) images each. Under them, three higher-magnification images are presented, which are representative of the corresponding region in the panoramic image. The exposed edge, through which the conversion starts, is on the left side of the HRTEM image in figure 4.3b. Region 1 shows highly oriented continuous multilayer WS_2. This is correlated with the area having uniform, high Raman intensity in figure 4.2a. Region 2 consists of multilayer WS_2, showing more disorder and occasional small inclusions of metallic W than region 1. The term disorder, is used to refer to the variation of the number of layers, non-uniform alignment of these layers, and gaps between the grains. These are consistent with the variations observed in Raman intensity maps. Region 3 mostly consists of metallic W. This correlates with the end of the region, laterally converted to TMD, observed optically. The occasional layered WS_2 can be found between the metallic grains. The material evolution across these regions, suggests a diffusion-driven mechanism, by which the chalcogenide progresses between the layers from the exposed interface. The presence of WS_2 in region 3, beyond the still-metallic regions, suggests grain boundary diffusion plays a role in this process.

Figure 4.3d shows a cross-sectional HRTEM image of the thinnest sample obtained. With an initial WO_x thickness of 2.4 nm, the converted WS_2 is a highly crystalline

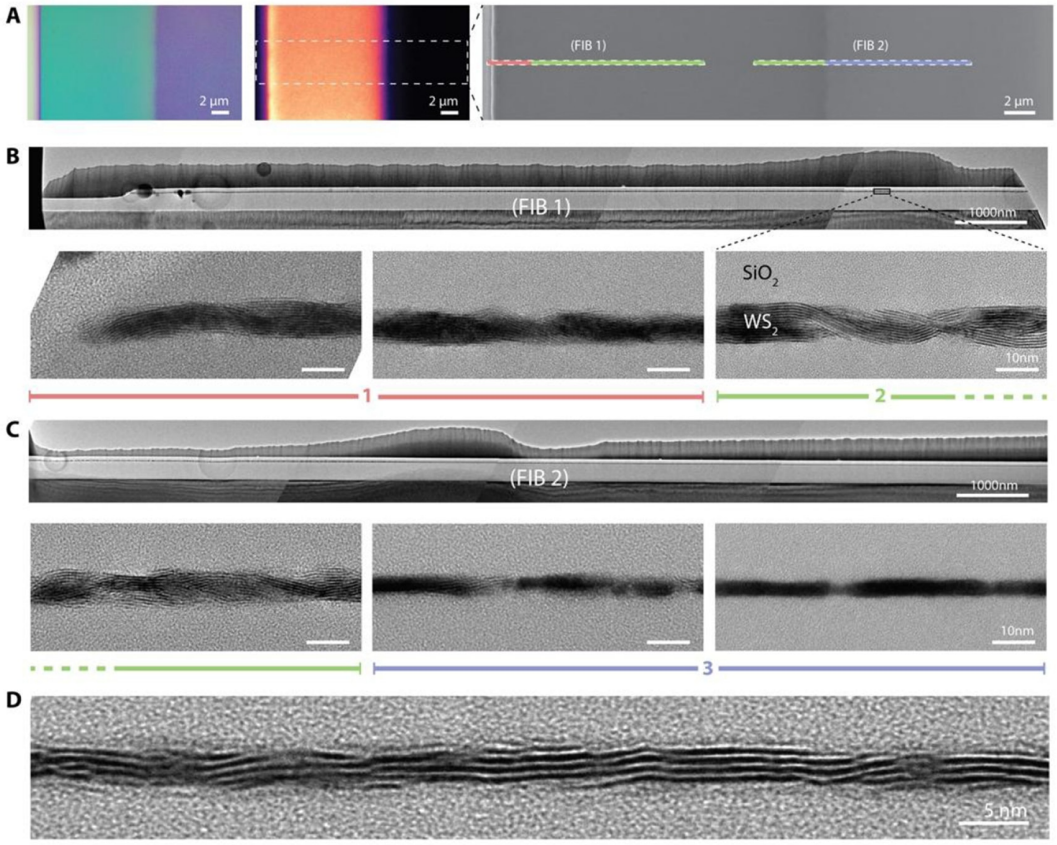


Figure 4.3. Structural characterization of WS_2 synthesized using lateral conversion. (a) WLRM, Raman and SEM images (from left to right) of the region on the converted that was used for cross-sectional TEM analysis. The dashed boxes indicated the areas from which lamellas were FIB milled. (b) and (c) Panoramic TEM image (top) and HRTEM images (bottom) of WS_2 sandwiched between amorphous silica layers. (d) Cross-sectional HRTEM image of a few-layer WS_2 synthesized using lateral conversion technique and demonstrating highly aligned TMD material. This figure is reprinted from an open access article [159] under the terms of the Creative Commons Attribution 3.0 license.

film composed of 4 ± 1 Van der Waals layers, having a high degree of alignment within the plane of the confined area.

The precise control over the thickness of the WS_2 layers, wafer-scale lithographic alignment, and pre-existing capping layer, make this a promising method for the fabrication and wafer-scale integration of TMDs in electronic devices. The pre-existing protective layer should enable clean and contamination-free integration of these highly surface-sensitive materials. Moreover, the top layer (composed of silica or other suitable material) can serve as a seed layer for subsequent ALD deposition of thin films. This is especially important for ideal, large-domain TMDs, since they do not have nucleation sites on the basal plane for ALD reactions, similar to CNTs (detailed discussion can be found in chapter 3.3). Thus, the capping layer

can help to deposit high-κ dielectric and ferroelectric materials to engineer the gate oxide stack of future TMD-based FETs.

4.4. Lateral conversion kinetics

To further study the origins of the lateral conversion, the dependence of ELC on the sample thickness, reaction temperature, and time was studied. All other parameters, such as temperature ramp-rates, gas flow-rates, and pressure were kept constant. The ELC was extracted from the measurements obtained using Raman spectroscopy and WLRM. To obtain Raman line scans and point spectra, a Horiba Jobin Yvon LabRAM ARAMIS confocal microscope, equipped with 532 nm laser and focused by a 100$\times$ 0.9 NA objective, was used. Figure 4.4a shows the integrated intensities of the $E_2^1g + 2LA$ and A_1g Raman modes as a function of distance (top). The corresponding true-color WLRM image is at the bottom, showing that the color contrast corresponds to the WS_2 Raman signal, and can be used to extract the ELC with a comparable precision. Such correlation was observed for all studied samples. Therefore, WLRM was used to simplify the characterization process and to quickly extract the ELC in all further measurements. From WLRM images, the ELC was programmatically extracted in ImageJ by measuring intensity profiles, based on color differences between the converted and not-converted regions of the samples.

Time dependence. Samples with a WO_x thickness ranging from 2.4 to 9.6 nm, were used to study the conversion kinetics. The WO_x films in these samples were first reduced to metallic W by annealing in Ar/H_2 at 750 °C for 120 - 180 min. A sufficient time and temperature were used to ensure reduction of the entire WO_x layer. Next, they were sulfidized for times ranging from 15 to 120 min. The resulting ELC is shown in figure 4.4b. Two main conclusions can be made: the ELC increases with the increasing (a) oxide thickness and (b) sulfidation time. The 3.6 and 4.8 nm samples show a smoothly increasing thickness with time, whereas thicker films show a steep increase after 60 min of sulfidation.

Temperature dependence. To study the temperature dependence of sulfidation, samples were reduced, as described for the time-dependent studies, and chalcogenated at temperatures varying between 650 °C and 800 °C, while keeping the sulfidation time constant at 30 min. The resulting ELC is shown in figure 4.4c, showing that it increases with increasing reaction temperature. However, the temperature-dependent curve does not follow a simple Arrhenius equitation,

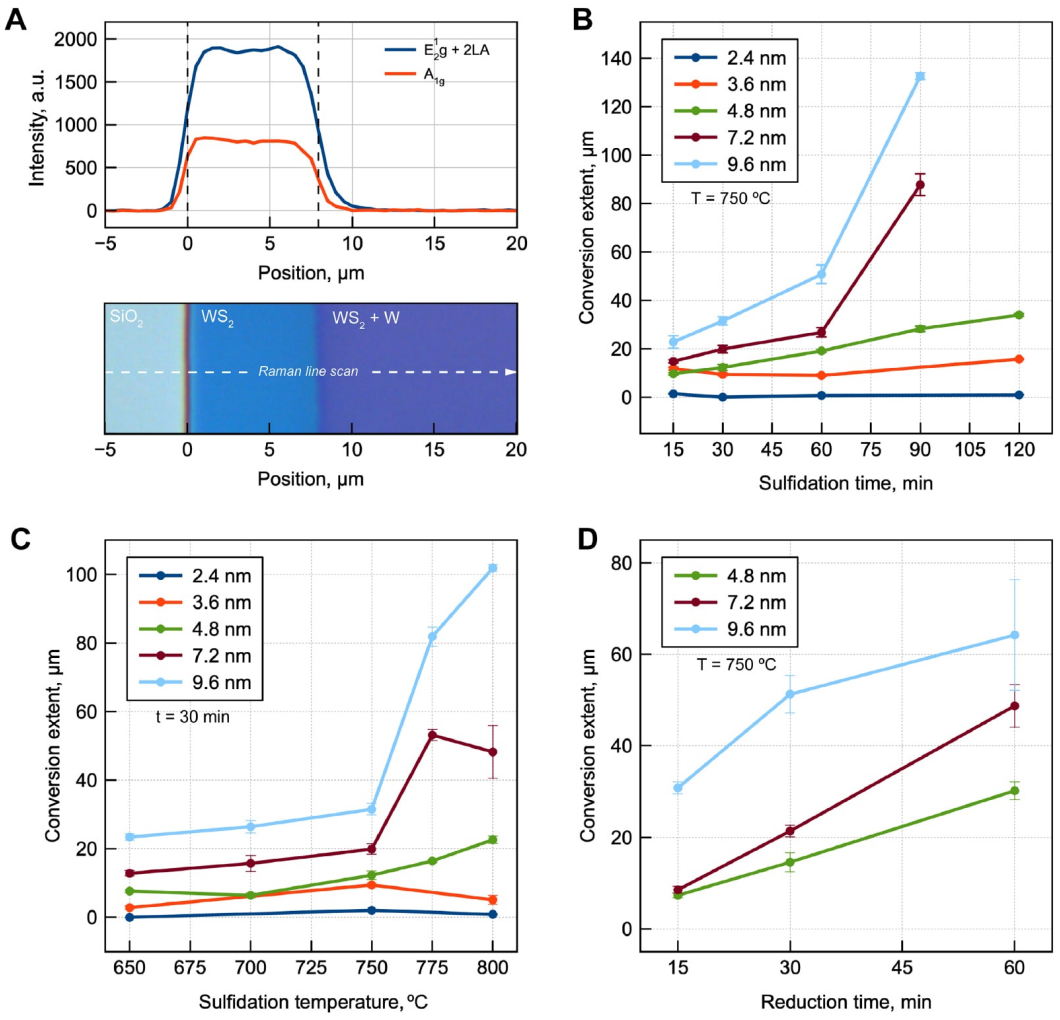


Figure 4.4. Lateral conversion kinetics. (a) Raman intensity line profiles of $E_2^1g + 2LA$ and A_1g modes of the laterally converted WS_2 and WLRM image from the same area, demonstrating that both techniques provide similar ELC information. (b) ELC dependence on the sulfidation time. (c) ELC dependence on the temperature. (d) Extent of lateral reduction as a function of WO_x reduction time. This figure is reprinted from an open access article [159] under the terms of the Creative Commons Attribution 3.0 license.

which is an indicator that diffusion driven process cannot be explained by simple random-walk diffusion, and has a more complex nature. At temperatures higher than 800 °C, the trends break down, which we attribute to the formation Si_xS_y, observed on the edges of the sample – where the SiO_2 layer is thinnest. We believe silicon sulfide forms a reactive species that negatively impacts the conversion, hence the trend breakdown and significantly larger error bars. Similar series of time and temperature experiments were performed on quartz substrates (not presented here) as opposed to Si substrates, and showed that quartz is able to withstand higher temperature conversions, supporting the hypothesis that silicon plays a role.

The obtained time- and temperature-dependent conversion rates do not follow those expected for a simple diffusion-driven process. One of the explanations for this may be the existence of multiple diffusion mechanism that take place concurrently and have different rates. The microfabricated geometry may permit three pathways for the diffusion of sulfur or H_2S: (1) through weekly attached Van der Waals WS_2 layers; (2) through grain boundary diffusion; and (3) diffusion through thin film discontinuities, originating as a result of the oxide volume shrinkage during the reduction step. Further study is needed to better understand this process.

The impact of the reduction step. The ELC was also studied as a function of reduction step duration. For this, samples were reduced for 15 - 60 min, while the subsequent sulfidation step was performed for 120 min. The direct observation of reduction is challenging due to the very small color contrast between WO_x and W, and because no Raman peaks could be observed for either material. Therefore, the extent of reduction was indirectly inferred from the extent of conversion to TMD when the duration of the reduction step was kept small (varied), followed by an excess sulfidation step. Importantly, in the absence of a reduction step, little to no conversion was observed. The obtained results are shown in figure 4.4d. The general trends show that thicker films and longer reduction times result in a larger extend of reduction/conversion. This behavior strongly suggests that the reduction of WO_x to metallic W proceeds laterally as well.

The previous discussion may lead to the idea of using a metal seed layer by depositing W metal and converting from it directly. While this might be an interesting approach for a thicker WS_2 synthesis, for a few- or mono-layer material, an ultra-thin seed layer is required. The synthesis of uniform sub-5 nm thick metals is challenging, since they typically used sputtering or electron beam/thermal evaporation approaches. These typically result in thin films that are discontinuous and consist of separate islands, which would produce non-uniform TMD layers. On the other hand, ALD of metal-oxides enables the synthesis of ultra-thin films at wafer scale, and can coat high-aspect ratio structures, which could further enable 3D integration of TMDs into various advanced architectures using this method.

4.5. Extensibility of the lateral conversion technique

In the previous sections we introduced the idea of TMD synthesis using lateral conversion, showing that it is not only possible to synthesize highly crystalline WS_2, but also to lithographically define its location, shape, and thickness down

to a few layers. Next, we were able to extend this technique to fabricate WSe_2, MoS_2, $MoSe_2$ and a multilayer structure consisting of alternating WS_2 and SiO_2 layers. Figure 4.5a-c show true-color WLRM images of the obtained materials and the corresponding Raman spectra. The Raman modes of each TMD material were fitted with Lorentzian functions to obtain their position, and are consistent with those reported in literature – confirming the assigned composition. The obtained $MoSe_2$ and WSe_2 show non-uniform conversion around the etched hole, unlike WS_2 and MoS_2. We believe that the optimization of the micro-fabrication, conversion or both processes can improve the uniformity.

Figure 4.5d shows WLRM and cross-sectional HRTEM images of a vertically stacked sample with alternating layers of WS_2/SiO_2. The WS_2 was synthesized by converting WO_x with a thickness ranging from 9.6 nm to 3.6 nm from bottom to top. Due to different ELC of each layer, the top-view WLRM image reveals concentric layers around the etched holes. Only three rings are observed (out of expected four) since the conversion of the topmost layer was not successful. This is also evidenced by the HRTEM image, which shows that the top layer consists of metallic W. We suspect that the opening was clogged with redeposited SiO_2 during the dry etching step, inhibiting chalcogen diffusion. The thicker layers show highly aligned WS_2 layers. This demonstration shows that the lateral conversion method provides a unique capability of synthesizing vertically stacked layers, and together with the demonstrated range of synthesized TMD materials, shows the flexibility of the technique.

To summarize, the developed lateral conversion technique was used to synthesize a number of TMD materials from metal-oxides. A combination of ALD-enabled angstrom level precision of the seed layer thickness and lithographic patterning, allows control of the thickness, shape, and location of the TMD material on a wafer scale. In addition, the resulting structure has a pre-existing capping layer that can protect delicate TMDs from damage during the subsequent fabrication steps and integration into devices. Moreover, the capping layer (SiO_2 in this work) enables subsequent ALD deposition, which is known to be challenging on pristine TMDs, since TMDs (similar to CNTs) do not have dangling bonds on their basal plane. Thus, the capping layer not only protects TMDs, but can also serve as a buffer layer for subsequent coating with, for instance, high-κ dielectric or ferroelectric materials, which is an important aspect of this work.

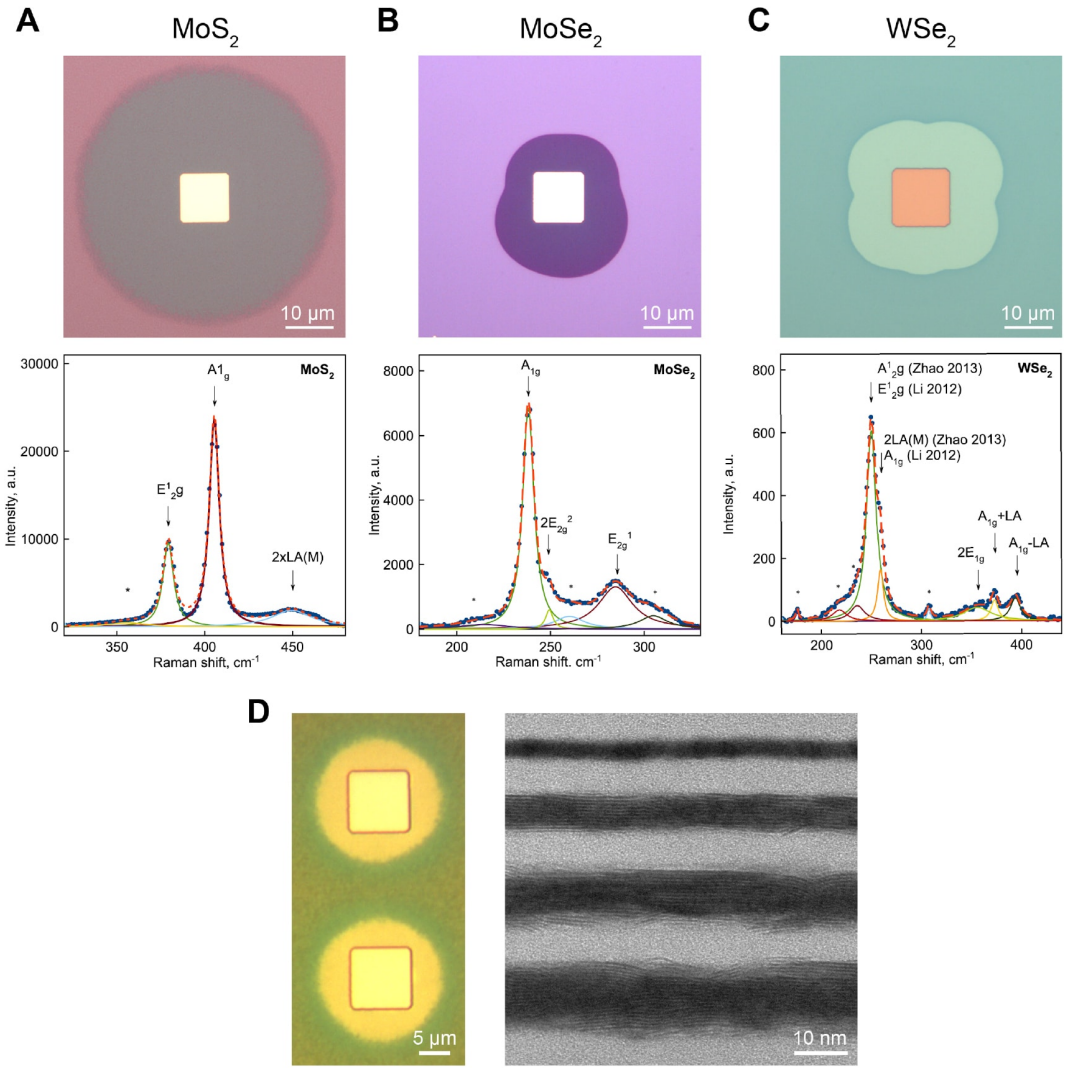


Figure 4.5. The extensibility of the lateral conversion technique. Optical image (top) and corresponding Raman spectrum (bottom) of (a) MoS_2, (b) $MoSe_2$ and (c) WSe_2, synthesized using lateral conversion process. (d) WLRM image (left) and cross-sectional HRTEM image (right) of the vertically stacked WS_2/SiO_2 multilayer structure. This figure is reprinted from an open access article [159] under the terms of the Creative Commons Attribution 3.0 license.

Notes

[2]The results of this chapter have been published in [174].

[3]Chemical conversion on the furnace reactor were performed by visiting students Aldiyar Kuntubek (NU, Kazakhstan), Nicholas Chang (University of Nevada, USA) and Bekassyl Battalgazy (NU, Kazakhstan) under the supervision of Dr. Tevye Kuykendall (Berkeley Lab, USA).

[4]WLRM images were obtained by Dr. Tevye Kuykendall, Berkeley Lab (USA).

[5]TEM measurements and the corresponding sample preparation using FIB were performed by Dr. Shaul Aloni, Berkeley Lab (USA).

[6]High resolution Raman spectroscopy and the corresponding data fitting were performed by Dr. Shaul Aloni, Berkeley Lab.

5. Synthesis and characterization of ferroelectric hafnium zirconium oxide

This chapter discusses the process flow development for the synthesis of hafnium zirconium oxide, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films, their integration into capacitors, and post-synthesis annealing techniques required to induce ferroelectricity in hafnia. HZO integration into metal-insulator-metal (MIM) stacks was achieved by sandwiching it between two titanium nitride (TiN) layers. This was necessary for two reasons: (1) to use the TiN as electrodes during the testing of ferroelectric properties; and (2) to provide mechanical confinement for the HZO layer, required to induce ferroelectricity in the material.

In terms of post-synthesis annealing of amorphous HZO, with the aim to crystallize it, two routes were explored: (1) rapid thermal annealing (RTA); and (2) irradiation with intense pulsed ions beams (IPIBs). The latter approach is especially interesting to explore since it can be used to precisely control the temperature ramp rate, and, more importantly, cooling rate, as will be discussed later in the text. In addition, IPIBs enable ultra-low thermal budge annealing, since it is possible to achieve temperatures as high as 2000 °C within nanoseconds. Although we have not studied ferroelectricity in HZO obtained with IPIB-based annealing yet, the crystallization of hafnia, zirconia and HZO using this technique was shown for the first time. On the other hand, the RTA approach was successful, resulting in ferroelectric HZO and will be used as a benchmark to improve the irradiation process.

5.1. Metal-insulator-metal stack fabrication

MIM stacks were fabricated at the Nanofabrication facility of The Molecular Foundry (Berkeley Lab, US). The recipe for each ALD layer (bottom TiN, HZO, top TiN) was developed separately and later used to grow the multilayer structure, schematically depicted in figure 5.1a. ALD and the corresponding recipe development was performed on an Oxford Instruments FlexAL PEALD system (Oxford Instruments, UK). Using an *in situ* Woolam M-2000 ellipsometer, the growth rate was monitored to optimize the synthesis parameters (e.g. precursor temperature, pulse width, purge duration, etc.) and obtain linear growth behaviour. Silicon wafers with 250 nm thermal oxide, or prime Si wafers (both moderately doped, ρ = 1 - 60 Ω × cm) were used as substrates for process development and final devices. Before starting the synthesis, full wafers or wafer pieces were loaded into the reactor, preheated to 250 or 300 °C, and evacuated to reach a base pressure of 5×10^{-6} mbar or better. A recipe was then started and the chamber was filled with Ar to reach the growth pressure (typically in the 10-80 mTorr range). ALD precursors were alternately pulsed into the chamber to grow one of the materials (eg. TiN). Between deposition of each type of material, the ALD chamber was pumped down to 5×10^{-6} mbar (= 3.8×10^{-6} Torr) or better before growing the next layer, to minimize/remove unreacted precursors and eliminate the formation of intermixed layers. The final MIM stack, consisting of TiN/HZO/TiN layers were grown in one ALD reactor without breaking the vacuum, to ensure high-quality interfaces between the materials. However, the recipe for each layer was developed separately, as discussed below.

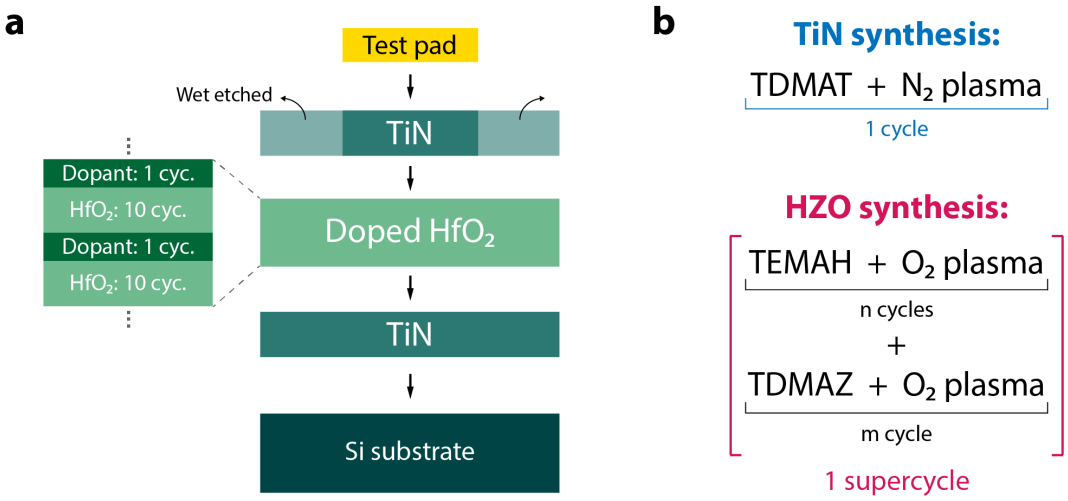


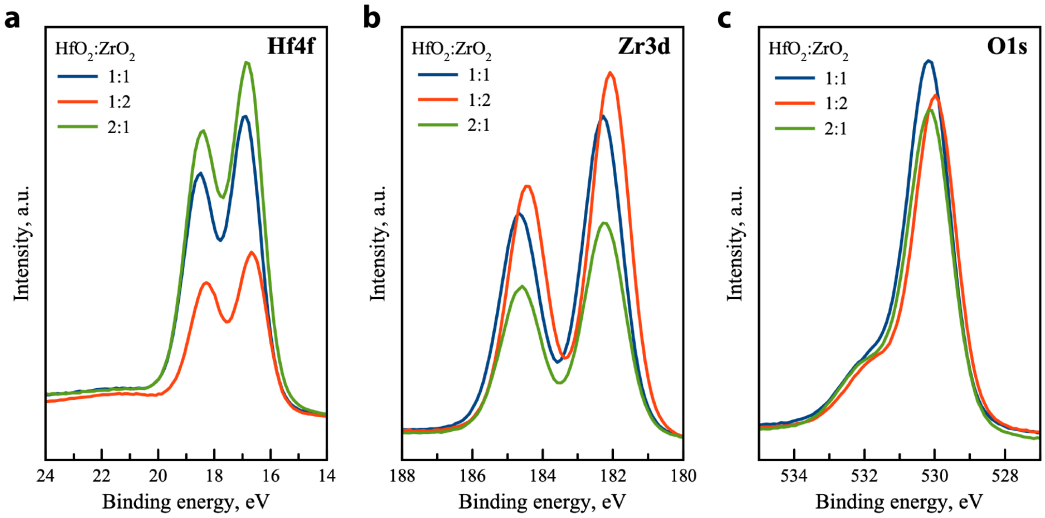
Figure 5.1. MIM capacitor geometry. (a) Fabrication process flow schematics. (b) ALD precursors and cycles used to synthesize HZO films.

Titanium nitride (TiN) was grown via ALD using tetrakis(dimethylamino)titanium (TDMAT) and N_2 as the titanium and nitrogen precursors, respectively. TDMAT was first pulsed into the chamber with a duration of 0.8 s to react with the substrate, followed by purging with Ar for 5 s to remove byproducts and unreacted TDMAT. Next, N_2 plasma was introduced into the reactor for 30 s to complete a reaction cycle, forming TiN. The cycle was finished by purging byproducts and unreacted TDMAT with Ar for 5 s. The *in situ* ellipsometer measurements revealed TiN growth of 0.5 Å/cycle with a linear rate, except for the first 2-3 cycles. The final TiN thickness was controlled by repeating ALD cycles: (TDMAT pulse) + (N_2 plasma pulse) = 1 cycle (see figure 5.1b). The number of cycles was set to 200 cycles to obtain 10 nm thin films. Electrical properties of TiN were measured using Van der Pauw (four point) technique on an Ecopia HMS-5000 series Hall effect measurement system. For this $\sim 1 \times 1$ cm samples were mechanically cleaved and loaded into the thermal evaporator to deposit a Cr/Au bilayer with a nominal thickness of 10/50 nm, respectively. Electrode deposition was performed using a shadow mask to form $\sim 2 \times 2$ mm test pads at the four corners of the square sample. To ensure good contact between the test pads and probes, small slices of indium metal were manually placed on the test pads. The resistivity of 10 nm thick TiN films, deposited at 300 °C, was measured to be $\rho = 1.35\ 10^{-4}\ \Omega \times cm$ (at room temperature), which is comparable with the data reported for PEALD TiN in the literature [175, 176]. This is, small enough for TiN to serve as an electrode in a MIM capacitor, but higher than that of traditional metals by ~2 orders of magnitude. Compared to resistivities on the order of $10^{-6}\ \Omega \times cm$ [177] for TiN with very few impurities, our relatively higher resistivity can be explained by carbon and oxygen inclusions that originates from the precursor chemistry and cross-contamination from other metal oxides previously deposited by users in the same ALD reactor. The oxygen content in TiN (or more precisely TiO_xN_y) thin films was studied by another group of scientist from the Molecular Foundry, with Auger electron spectroscopy, confirming O_2 presence when deposited using a similar recipe in the same system [178].

Hafnium zirconium oxide was grown by depositing alternating layers of HfO_2 and ZrO_2 of different thickness to control the stoichiometry of the final $Hf_xZr_{1-x}O_2$. HfO_2 was grown using tetrakis(ethylmethylamido)hafnium(IV) (TEMAH) preheated to 100 °C. TEMAH was pulsed into the chamber with a duration of 0.1 s, followed by a 6 s Ar purge step. Oxygen plasma was used as the second precursor. *In situ* ellipsometer measurements revealed a HfO_2 growth rate of 1.12 Å/cycle. ZrO_2 was grown using tetrakis(dimethylamido)zirconium(IV) (TDMAZ) preheated to 70 °C. TDMAZ was pulsed into the system with a duration

of 0.1 s, followed by a 6 s Ar purge step. Oxygen plasma was used as the second precursor. In situ ellipsometer measurements revealed a ZrO_2 growth rate of 1.13 Å/cycle.

Other works on ferroelectric HZO [104] have shown that the optimal Hf-to-Zr ratio is 1:1 and that the thickness of the thin film should be ~10 nm (see figure 2.9d) to achieve the best ferroelectric performance. To reproduce these results, three samples were prepared with HfO_2-to-ZrO_2 ALD cycle ratios of n:m = 1:1, 1:2 and 2:1 (Figure 5.1b), composing a super-cycle that was repeated the required number of times to obtain 10 nm thick HZO thin films. It is important not to confuse the ALD cycle ratios with the Hf-to-Zr concentrations (i.e. stoichiometry of the final film), which do not translate one-to-one, since the density and deposition rates of HfO_2 and ZrO_2 can be different.



d

HfO_2:ZrO_2	Hf, at%	Zr, at%	O, at%	Hf:Zr	Stoichiometry		
					Hf	Zr	O
1:1	12.6	20.7	66.7	0.6	0.4	0.6	2.0
1:2	7.1	26.1	66.8	0.3	0.2	0.8	2.0
2:1	**16.5**	**15.8**	**67.8**	**1.0**	**0.5**	**0.5**	**2.0**

Figure 5.2. XPS measurements1 of HZO samples with different HfO_2-to-ZrO_2 ALD cycles ratio. High resolution XPS spectra of (a) Hf4f, (b) Zr3d and (c) O1s energy levels. (d) Extracted stoichiometry of HZO samples.

Figure 5.2 shows **XPS measurement** results obtained using a Thermo Scientific K-Alpha x-ray photoelectron spectrometer,[7] with a monochromatic Al Kα X-ray ($h\nu$ = 1486.7 eV). The Hf4f, Zr3d and O1s peaks were fitted and analyzed using the Thermo Scientific Avantage software to obtain atomic percentage of the elements and extract the resulting stoichiometry (figure 5.2d). The sample with a HfO_2:ZrO_2

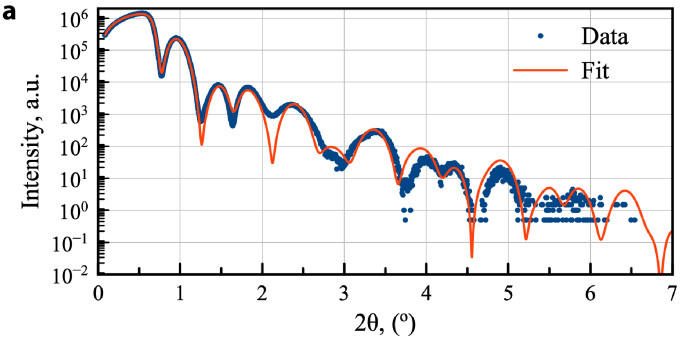
ratio of 2:1 showed $Hf_{0.5}Zr_{0.5}O_2$ stoichiometry, and its recipe was used to fabricate all HZO-based MIM capacitors.

The deposition rates extracted from ellipsometry, were used to nominally obtain 10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ layer, sandwiched between 10 nm thick TiN layers, by performing 30 ALD super-cycles (with HfO_2:ZrO_2 = 2:1) and 200 ALD cycles, respectively. It is important to mention that ellipsometry was used to estimate the growth rate of HfO_2 and ZrO_2 thin films, separately; to avoid complications with fitting a compound ALD layer, it was not used to directly measure the thickness of the resulting HZO layer.

X-ray reflectometry (XRR) measurements were performed to measure the thickness of TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN multilayer stack deposited on prime Si substrate. XRR was done at Nazarbayev University on a Rigaku SmartLab XRD/XRR system and equipped with a Cu Kα (1.54 Å) source.[8] The measurements were performed at an angle of incidence ranging from 0° to 7° with 0.01° step in a parallel beam, parallel slit geometry with an incident slit width of 0.05 mm, and receiving slit width of 0.25 mm.

Figure 5.3a shows the obtained XRR spectrum (blue dots). The oscillations in the spectrum result from interference fringes, originating from X-ray reflections from each layer of the stack as the X-rays penetrate deeper inside the sample, with increasing angle of incidence. The oscillation periodicity was used to extract the thickness of each layer, whereas the roughness was calculated from the dampening of the reflected signal. For this, the XRR spectrum was fitted using GenX 2.4.10 software [179], freely available at https://genx.sourceforge.io/. The following stack was used for simulation (from bottom to top): Si substrate/SiO_2/TiN/$HfZrO_4$/TiN/ambient. The SiO_2 layer was used to represent the thin native oxide layer formed on the surface of a prime Si wafer. Thickness and density of the top and bottom TiN layers were coupled (set to be equal) to reduce the computation time. Si and SiO_2 densities were set to constant values of 2.33 and 2.6 g/cm^3 respectively. The density, thickness of ALD layers and roughness of all layers were fitted. Beam footprint correction and normalization factors were fitted as well. GenX software uses the unit [formula unit/Å^3] as a unit to input and output material density, which can be converted to/from the more familiar [g/cm^3] by using the instructions available at https://genx.sourceforge.io/doc/faq.html, or the "SimpleLayer" plugin natively available in the software. The crystallographic R-factor or R1-factor was used as a figure of merit [180].

a



b

Parameter	Value
Top TiN roughness, A	4
HZO thickness, A	63
HZO roughness, A	3
HZO density, g/cm^3	7.9
TiN thickness (coupled), A	109
TiN density (coupled), g/cm^3	4.1
Bottom TiN roughness, A	3.8
Native oxide thickness, A	14.29
Native oxide roughness, A	6
Si substrate roughness, A	0.1
Beam footprint corrections, a.u.	1.19E-02
Normalization factor, a.u.	2.50E+06

Figure 5.3. X-ray reflectivity from a TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN multilayer stack. (a) XRR measurement results. (b) Parameters extracted from the fit.

The extracted parameters are presented in figure 5.3b. The roughness of all simulated layers was extracted to be in the sub-1 nm range, revealing a high-quality interface between them. As expected, the TiN thickness was calculated to be ~11 nm with a density of 4.1 g/cm^3. The thickness of the HZO layer was ~6 nm, which is surprisingly low, compared to expected 10 nm. In the recipe used, two HfO_2 cycles were followed by one ZrO_2 cycle, and the process was repeated. Lower nucleation of ALD layers on the surface of another material during the first few cycles is a well-known problem, and in this situation, all cycles can be considered as "the first few cycles". Thus, we hypothesize that such a discrepancy can be explained by the low initial ALD nucleation of HfO_2 on ZrO_2 and vice versa. This means that the deposition rate of a thicker oxide (which is an average deposition rate across all ALD cycles) cannot always be used to reliably estimate the thickness of a super-thin (sub-) monolayer of the same material.

5.2. Ferroelectricity stabilization in HZO using RTA

As discussed in chapter 2.4.2 for a material to be ferroelectric, it should have a particular crystalline structure. For hafnia-based ferroelectric materials, the ferroelectricity is influenced by the relative amount of orthorhombic phase. Using recipes discussed in the previous section, the as-deposited ALD thin films are amorphous. To crystallize the HZO films, rapid thermal annealing (RTA) was used. RTA relies on fast heating of samples using an IR lamp. With temperature ramp rates up to 250 °C/sec for some commercially available systems, samples can reach crystallization temperature within seconds. This allows annealing of the substrates at high temperatures to induce crystallization with a low thermal budget. In addition to high ramp rates, RTA offers a higher cool down rate, compared to conventional ovens, since heating is typically localized around the sample and the

oven/chamber walls do not have time to become as hot, unless a prolonged annealing was performed.

Annealing. To anneal HZO integrated into MIM stack, an ULVAC MILA-5000 RTA system was used. Several TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN on Si samples were annealed for 60 sec at 550, 600, and 650 °C, under N_2 flow with a rate of 1 slm (standard litre per minute), and a pressure of 1 atm. The maximum temperature ramp rate of the RTA is 50 °C/sec, but results in large overshoot (sometimes more than 30 °C), so the ramp rate was kept constant at 20 °C/sec for all samples, resulting in 1-2 °C overshoot. To speed up the cooling down process, N_2 flow rate was increased to a maximum value of 3 slm right after the annealing. The resulting cool down rate was ~10 °C/sec for the temperature range between 650-300 °C.

Crystallinity of HZO thin films. After annealing, the degree of crystallinity was measured by grazing incidence x-ray diffraction (GIXRD) technique at Nazarbayev University[9] using a Rigaku SmartLab XRD system equipped with a CuKα (1.54 Å) source. The measurements were performed at an incidence angle of 0.5° (which is close to critical angle of total reflection) in a parallel beam, parallel slit geometry, with a collimator slit width of 0.02 mm, and detector slit width of 10 mm using the "1D" detector mode. Such a low angle of incidence was used to reduce the penetration depth of X-rays and to obtain information from the near-surface layer, enhancing the signal from the top ~30 nm, where the thin films of interest were grown.

The GIXRD measurements were obtained from TiN (10 nm)/$Hf_{0.5}Zr_{0.5}O_2$ (6 nm)/TiN (10 nm) deposited on a Si substrate after annealing at 500 – 650 °C. These particular samples were measured after Cr/Au contact deposition and top TiN removal (fabrication details are discussed in the next section). Black curves in figure 5.4a represent the raw data. The XRD pattern of the sample annealed at 500 °C does not have any peaks that can be attributed to HfO_2, which means that the annealing was not sufficient, and little to no crystallization of hafnia was achieved. After annealing at higher temperatures, multiple peaks emerge that correspond to different HfO_2 polymorphs. For example, the peak at 30° is a mix of the signals from orthorhombic and tetragonal phases. Precise identification of each hafnia phase contributing to the diffraction pattern is challenging due to overlapping peaks (see reference peaks at the bottom of figure 5.4a). However, it is still possible to extract phase fractions by preforming Rietveld refinement, which is a fitting procedure that uses the least squares method to refine a theoretical profile and match it to

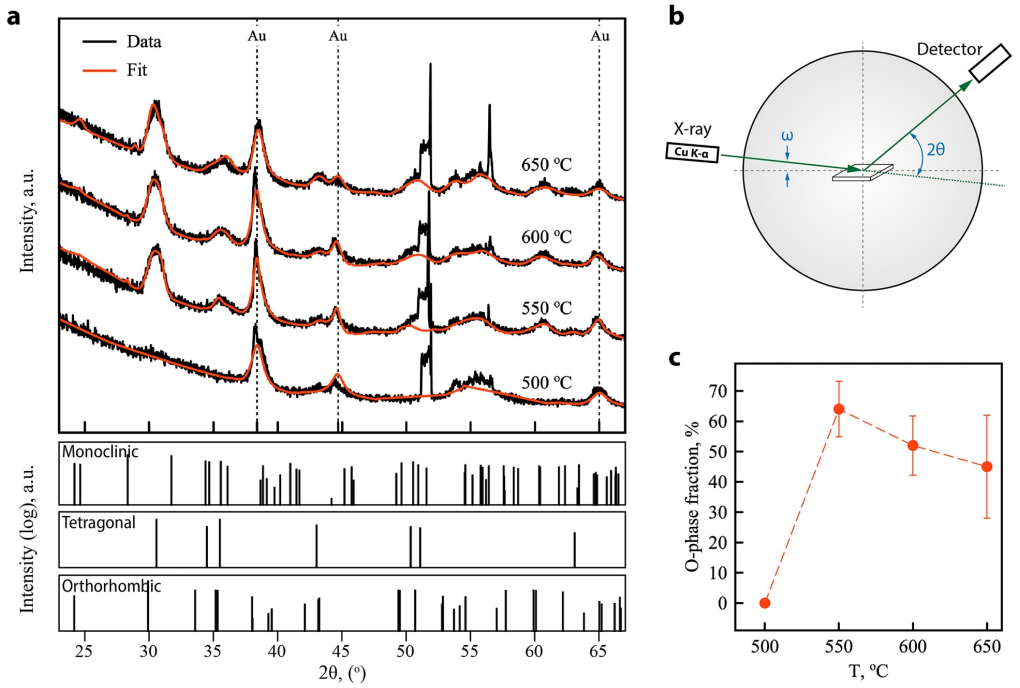


Figure 5.4. GIXRD measurement of annealed HZO. (a) GIXRD patterns (black curves) with Rietveld refinement results (red curve) for samples annealed at 500 - 650 °C. (b) Schematic illustration of GIXRD technique. (c) Orthorhombic phase fraction extracted from Rietveld refinement for HZO annealed at 500 - 650 °C.

the experimentally obtained data by adjusting peak position, intensity, and shape. This is done by varying (1) crystal structure parameters of each phase, such as unit cell parameters a, b, c, α, β, γ and atomic coordinates; (2) specimen properties, e.g. texture and stress; and (3) instrument settings, such as wavelength, geometry, slits, angular calibration and broadening.

The following reference patterns were used for simulations: Au *Fm3m* phase (COD[10] 1100138), monoclinic-HfO_2 ([181] or PDF[11] 00-034-0104), orthorhombic-HfO_2 (PDF 04-005-5597), and tetragonal-HfO_2 (PDF 04-011-8820). The cubic phase was not used for the analysis since its diffraction peaks heavily overlap with tetragonal phase. Consequently, the tetragonal phase fraction might be overestimated, which is reasonable for our studies since we are mostly interested in the orthorhombic phase. Only HfO_2 reference patterns were used for fitting, despite having ZrO_2 in thin films in the same amount. This is an acceptable approach in the community due to the similarity of crystal structures of these oxides [182]. The Rietveld refinement was performed using Maud 2.39 software, freely available at http://maud.radiographema.eu/. The "theta_offset" parameter that accommodates for 2θ shift due to the offset of the diffractometer, was disabled/removed, to improve

the reproducibility. The sharp peak at around 51°, which belongs to the Si substrate [183], was excluded from the fitting process.

Figure 5.4c shows the extracted orthorhombic phase fraction for each sample. No orthorhombic phase was identified in the sample annealed at 500 °C. The highest o-phase concentration was found in HZO annealed at 550 °C, which decreases with increasing temperature. The refined profiles in figure 5.4a and error bars in figure 5.4c, are far from perfect since it is difficult to distinguish between different hafnia phases, although some estimation is still possible.

Metal-ferroelectric-metal capacitor (MFM) fabrication. After growth and annealing of the all-ALD grown MFM stack, capacitors with predefined shape and size were fabricated. For this, wafers were diced or mechanically cleaved into 1x1 cm chips, exposing the edges of all three layers. To establish contacts with the top and bottom TiN layers without short-circuiting them, Cr/Au test pads were lithographically defined on the surface of the top TiN layer. The purpose of the test pads is twofold: (1) to be used as test pads for electrical characterization; and (2) to serve as a hard mask for selective etching of top TiN layer, schematically depicted in figure 5.1a. The process details are provided in Appendix A3. Briefly, after photoresist patterning, a Cr/Au bilayer stack with a nominal thickness of 10/60 nm was deposited by thermal evaporation. Next, unwanted metal was removed using the lift-off technique – sonicating samples in acetone for 5 min. After the chips were rinsed in IPA for 1 min and blow-dried with N_2, they were ready for wet etching. The resulting Cr/Au test pads had a size of 80×80 μm.

The parts of top TiN film, that were not covered with Cr/Au electrodes, were etched at 50 °C for 5 min in diluted basic piranha solution consisting of NH_4OH:H_2O_2:H_2O, with the ratio of 1:2:40. For this, NH_4OH was first added into H_2O and the mixture was heated to 50 °C. Once the process temperature was reached, H_2O_2 was poured very slowly, and the etching was performed by immersing samples in the prepared solution. Basic piranha does not attack Cr/Au, nor the HZO layer, so the etching stops once the unprotected top TiN is fully removed. Some TiN under-etching can be expected under the Cr/Au bilayer, the extent of which is negligible compared to the electrode size. After etching, the samples are thoroughly rinsed in DI water and blow-dried with N_2. Each resulting 1×1 cm chip consisted of 80 square shaped MIM capacitors with an area of $A = 6.4 \times 10^3$ μm^2, having individual top electrodes and common bottom electrodes. To access the buried bottom electrode, a small droplet of silver paste was put on one

of the edges of the chip and dried, establishing a contact with the open edge of the bottom TiN layer. Figure 5.5a shows a top-view light-microscopy image from one of the regions with three fabricated capacitors, two of which were used for electrical characterization. The third one was not used due to irregular shape.

Ferroelectric measurements were performed at UC Berkeley on a Radiant Precision Multiferroic ferroelectric test system.[12] This system uses the so called "virtual ground method" to extract the polarization value [115]. The circuit implemented in the tester is schematically depicted in figure 5.5b, and relies on indirect current measurement using an inverting operation amplifier and a feedback resistor. In this configuration, the signal from the MFM capacitor (sample) is going to the inverting terminal of the op-amp, and the output voltage is adjusted to keep the voltage at both inputs equal, which is proportional to the current flowing through the feedback resistor.

All ferroelectric samples fabricated in this work, showed pinched hysteresis loops in pristine condition. The origin of such loops was discussed in detail in chapter 2.4.3 and was attributed to the "wake up" effect. After measuring their pristine ferroelectric properties, MIM capacitors were subjected to electric field cycling to open the polarization loop and study the remnant polarization improvement as a function of number of cycles. Figure 5.5c shows the cycling-measurement sequence that consisted of *P-E* hysteresis loop measurement, followed by electric field cycling and then repeated. All measurements on the ferroelectric tester were performed at a frequency of 1 kHz. The cycling was done using a square wave with a frequency of 10 kHz and an amplitude of peak to peak voltage of V_{pp} = 2 V using a Keysight 33500B Waveform Generator (UC Berkeley) in the burst mode, where the number of cycles can be specified.

Figure 5.5 shows ferroelectric polarization switching measurements of TiN samples (10 nm)/$Hf_{0.5}Zr_{0.5}O_2$ (10 nm)/TiN (10 nm) with a capacitor area of 6.4×10^3 μm^2, annealed at different temperatures. The MIM capacitor processed at 500 °C (figure 5.5d) shows a very small hysteresis window, which may suggest partial crystallization with mostly paraelectric behavior. Samples annealed at 550 °C showed pinched ferroelectric polarization loop in pristine condition (cycle #1 in figure 5.5e). With an increasing number of cycles, the hysteresis loop shape improves, reaching a maximum value after cycling 10'000 times with a remnant polarization of $2P_r = |P_r| + |\text{-}P_r| = 32$ $\mu C/cm^2$, which is higher than average reported HZO remnant polarization values in literature. The coercive filed was

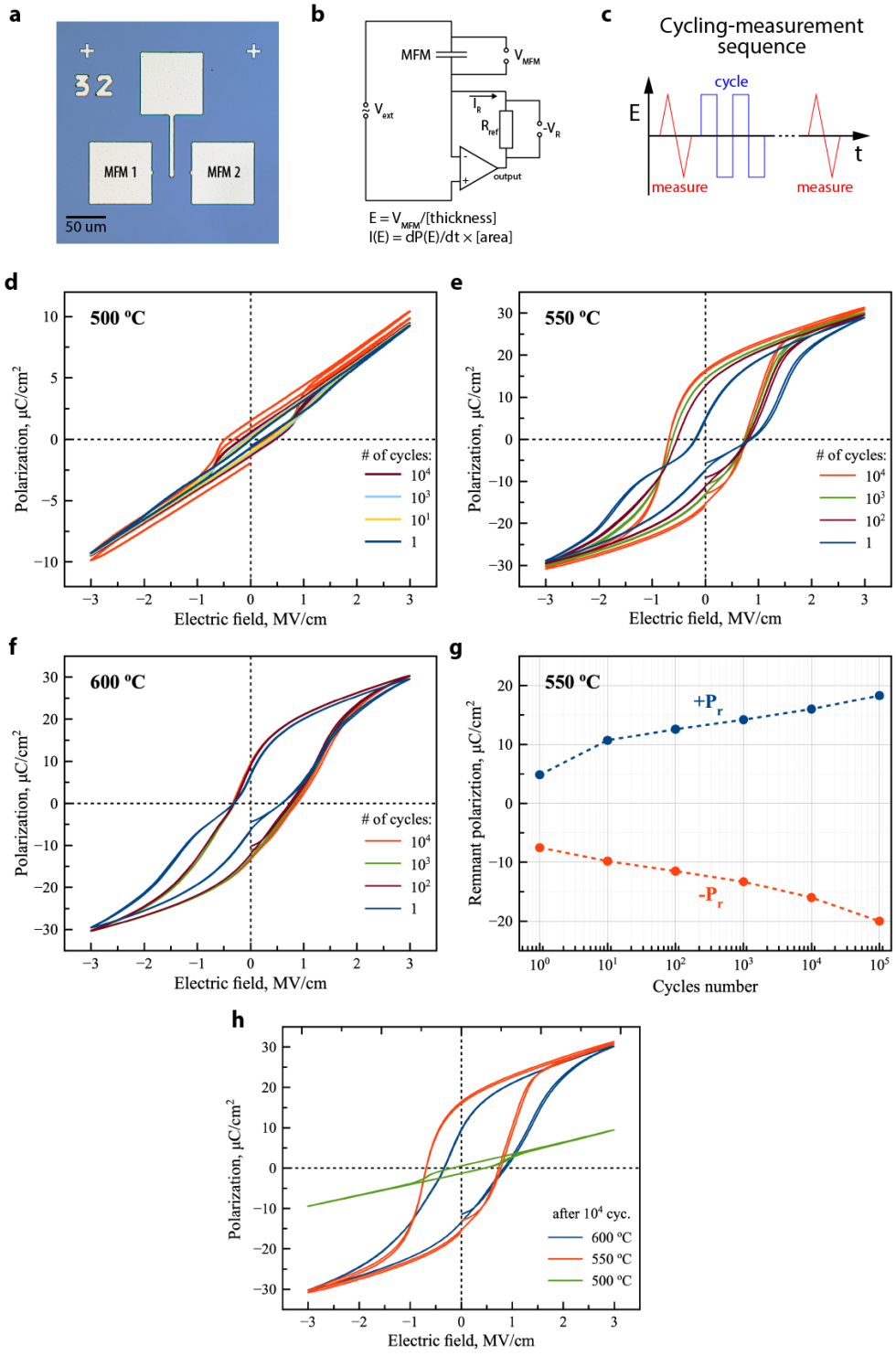


Figure 5.5. Ferroelectric hysteresis measurements of $Hf_{0.5}Zr_{0.5}O_2$. (a) Top-view light microscopy image of a typical sample region with MFM capacitors. (b) Virtual ground method circuit realized in the tester used to perform ferroelectric measurements. (c) HZO electric field cycling-measurement sequence to study wake up effect in HZO annealed for 1 min at (d) 500 °C, (e) 550 °C, (f) 600 °C. (g) Remnant polarization evolution after field cycling. (h) Comparison between woken up HZO annealed at different temperatures.

estimated to be $2E_c = |E_c| + |-E_c| = 1.4$ MV/cm. Figure 5.5g shows the remnant polarization evolution as a function of number of cycles. As can be seen, P_r continuously improves. However, after cycling the MFM capacitor 10^5 times the electric breakdown occurred (also observed for other samples), which was evidenced by a hysteresis loop shape of a leaky dielectric, so its higher P_r value can be neglected. Samples annealed at 600 °C also showed ferroelectric behavior with remnant polarization improving after the electric field cycling, reaching a maximum value of $2P_r = 23$ μC/cm^2. The lower P_r, compared to the sample annealed at 550 °C, suggests that less orthorhombic phase was stabilized. Figure 5.5h compares the hysteresis loops of all samples after waking up (conditioning), showing that the optimal annealing temperature is 550 °C.

5.3. HZO crystallization using Intense Pulsed Ion Beams

Rapid thermal annealing has proven to be a quick and reliable approach to stabilize ferroelectric properties in HZO. It has been routinely used for other ferroelectrics as well. Although RTA allows sample processing with low thermal budget, it is still challenging to perform annealing of functional layers deposited on temperature-sensitive substrates, such as polymers. In this context, annealing using nanoseconds-long intense pulsed ion beams is a promising approach since IPIBs deliver the energy within tens to hundreds of nanoseconds proving ultra-high heating and cooling rates. The latter is especially important to control since the ferroelectricity stabilization in hafnia occurs when the thin film is cooling down. By using substrates with different thermal conductivity, it is possible to increase or decrease the cool down rate of an irradiated sample, whereas by varying the ion beam intensity and pulse width, one can adjust the annealing temperature and duration. In the next sections, IPIB basics and applications in materials science are reviewed, and the first experiments towards IPIB-induced HZO crystallization are demonstrated.

5.3.1 IPIB basics and application in materials science

When solid materials are irradiated with high intensity pulsed beams, with pulse length of up to 100 ns, the following processes can take place [184]: (1) thermal effects; (2) thermal effects + mass deposition; and (3) shock wave generation. The first scenario takes place when the energy and density of ions penetrating into the solid material is not high enough to directly induce structural changes and most of the energy is converted into heat. Typically, purely thermal effects are expected

from relatively low doses ~10^{12} ions/cm^2, with energies up to several hundreds of eV. In the second case the ion density should be, in the range from 10^{14} to 10^{18} ions/cm^2 with energies up to several hundreds of eV. The ion dose is high enough to induce structural changes through doping, alloying, material intermixing and significant defect creation. The third effect – shock wave generation – can be understood as pressure pulses propagating inside the sample and on its surface. One of the mechanisms behind this effect is the rapid expansion caused by heating [184]. In addition to the previously mentioned effects, defects creation and annealing is another consequence of IPIBs interaction with matter [185].

Tuning materials properties using ion beams has a long-standing history [186]. Most of the early works were focused on studying the impact of ion beam treatment of bulk materials, such as metals and ceramics. Many species (ions) from the periodic table have been used for acceleration and their interaction with materials has been studied. Recently this technology has shown promising applications using hydrogen ions - or protons, among other ions, to study the interaction with thin films, nano- and microscale materials. Small diameter proton ions, compared to heavier ones, have a higher penetration depth (typically microns), and less destructive for thin films. Proton beams have been used to non-destructively induce phase transformation of paramagnetic materials, converting them into ferromagnetics [187] or to study radiation hardness and self-healing in perovskites [188] Proton beams are also extensively used for defect engineering, which has been used to controllably alter structural and electrical properties of oxides, such as ZrO_2 nanorods [189], TiO_2 thin films [190] and β-Ga_2O_3 [191]. Two-dimensional materials, such as graphene [192] and MoS_2 [193] were also investigated under the impact of proton beams, and the studies revealed a direct dependence between an increase in radiation dose and the introduction of defects. This technique has also proven to be efficient in interacting with biological materials, and proton therapy has become a common practice in medicine [194].

The above-mentioned applications of proton beams have generally employed continuous irradiation, where hydrogen ions are continuously pumped into a material until the desired changes are observed. This typically requires a long-term irradiation procedure (several hours and more) in order to reach the required fluences of ions supplied to sample. However, another special type of ion beam irradiation employs intense pulsed beams. This technique typically utilizes high current ion beams with densities above 10 A/cm^2, obtained using a magnetically insulated ion diode in a pulsed power architecture-based accelerator [195], in contrast to

continuous ion beams with currents in the range of nano- to micro-amps. At such relatively high current densities, 10^{10} - 10^{13} ions per cm^2 are supplied to the target per single shot with a typical duration of hundreds of nanoseconds. The ions are accelerated towards targets and delivered to them within hundreds of nanoseconds. Among other applications, this approach has been utilized for smoothing of surfaces [196], amorphization of materials [197], annealing of thin films [198] and to improve radiation hardness [199]. IPIBs allow super-fast heating in the tens-to-hundreds of nanoseconds regime, followed by super-fast cooling, leading to (re-) crystallization and phase transitions in materials. This opens new perspectives for ultra-low thermal budget annealing of materials, as well as may enable more precise control over the crystallization.

5.3.2 Interaction volume of proton beam generated on the INURA accelerator

In this work, IPIB was used to crystallize initially amorphous ALD deposited on top of Si substrate. In this configuration the structure of the surface layer can be changed, while the chemical composition is unaltered The irradiation experiments were performed on INURA high current pulsed ion accelerator [195]. The system uses a magnetically insulated ion diode with focusing geometry, an active anode plasma source, an accelerating voltage of 400 kV, an ion beam (pulse) duration of 80 ns, and a total beam current of 10 kA. The composition of the ion beam is determined by the material used as the electrode and can range from light ions, such as H^+, to heavy ions such as W^+.

To evaluate the ion penetration depth and energy loss, Monte Carlo simulations of hydrogen ions traveling inside a TiN (10 nm)/HZO (10 nm)/TiN (10 nm) on Si (500 μm) structure, were performed using the Stopping and Range of Ions In Matter (SRIM) software package [200]. For simulations, a non-monochromatic proton beam with a peak energy of 350 eV and a full width at half maximum (FWHM) of 10 eV was used, which resembles the irradiation parameters used in this study. The SRIM software package does not directly support simulation of non-monochromatic beams, however a list of ions with individual parameters, including ion energy, can be fed to the software. For this MATLAB was used to generate random energy values with normal distribution, given peak value and FWHM for 2,000 protons.

Figure 5.6a shows proton penetration depth distribution. According to the simulation results, most of the protons travel to a depth of around 4 μm, which

is much higher than the 30 nm thick ALD thin film stack on the surface of the sample. Since the ion stopping range is at least two orders of magnitude larger, it is possible to treat the interaction of the beam with thin films without considering doping and compositional changes. Inset of figure 5.6a shows simulated trajectories of ions.

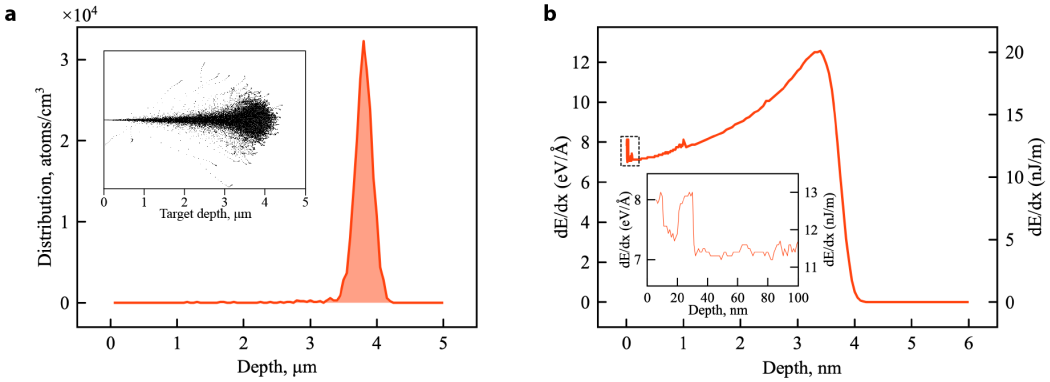


Figure 5.6. SRIM simulations of protons traveling inside HfO_2/Si target. (a) Hydrogen ions distribution and as a function of penetration depth. Inset in (a) shows the simulated trajectories of 2000 protons. (b) Energy loss within the full interaction volume. Inset in (b) shows the energy loss for the first 100 nm.

The energy loss plots in figures 5.6b, associated with proton beam interaction with the sample, show that the energy loss in the ALD thin films stack (see inset of figure 5.6b for more details) is only a fraction of the total energy transferred to the sample. Based on this result, we speculate that most of the heating should originate in the bulk of the Si substrate.

When using IPIBs, the heating effect can be varied by changing the intensity of ion beam. Increasing the intensity (current density) results in an increase of the number of ions interacting with the sample per pulse, transferring their energy, and higher annealing temperature can be reached as a result. On the other hand, a proton beam that is too intense may result in sputtering and ablation of materials, which was observed for all oxide samples irradiated with a current density of J = 90 A/cm^2 and higher. Thus, optimal irradiation parameters need to be found to controllably irradiate and anneal samples.

5.3.3 Hafnia and zirconia crystallization using proton beam irradiation

Two types of samples with pure, amorphous 10 nm thick (a)HfO_2 and (b)ZrO_2 thin films were deposited on silicon substrates using the ALD recipes discussed in

chapter 5.1. These films were subjected to irradiation with proton ions (H^+) with an accelerating voltage of 400 kV and a beam pulse duration of 80 ns.[13] Beam current density was varied between 30 and 100 A/cm^2, while keeping the acceleration voltage the same. The exact irradiation parameters are presented in Appendix A3. The degree of crystallinity of samples was studied using GIXRD.[14]

Figure 5.7 shows GIXRD spectra of pristine (non-irradiated) hafnia and hafnia irradiated with different beam current densities (top), as well as the reference diffraction peaks (bottom). Pristine material shows no clear HfO_2 peaks and one strong silicon substrate peak at around 51°, confirming the amorphous nature of ALD-deposited hafnia. After irradiation of samples with different proton beam current densities, multiple peaks emerge. It is typically difficult to differentiate between HfO_2 polymorphs, since their XRD peaks either completely overlap or are located very close to each other. Crystallographic information extraction using Rietveld refinement or other fitting procedures was not successful due to low signal-to-noise ratio, associated with the XRD system condition during the measurements. Nevertheless, analysis of a region between 27° and 37° allows a qualitative assessment of the HfO_2 crystalline composition.

The minimum required current density to induce crystallization was found to be around 60 A/cm^2. Below this value, no crystallization was observed. For samples irradiated with a current density of J = 63 A/cm^2, two peaks can be observed. The peak at around 30° can be attributed to a mix of orthorhombic (o-), tetragonal (t-) and monoclinic (m-) phases, whereas the peak at around 35° can be from m- and/or t-phase. At higher irradiation intensities, an additional peak emerges at around 28°, which can be attributed to the m-phase. The main peak at 30° slightly changes its shape with the increasing current density, so that the left shoulder of this peak, responsible for o/t-phases, becomes less pronounced. Together with the appearance of a monoclinic peak at 28°, it can be concluded that orthorhombic/tetragonal-to-monoclinic content ratio has decreased after irradiation with proton beams of higher current densities - 75 A/cm^2 and 81 A/cm^2. Current densities lower than ~60 A/cm^2 did not result in any observable hafnia crystallization, whereas beams with 90 A/cm^2 and higher started to damage the surface of the sample.

Figure 5.8 shows the irradiation results of ZrO_2 thin films. Similar to hafnia, as-deposited zirconia is amorphous and has no XRD peaks, and the only observable peak is from the Si substrate. Zirconia irradiated with J = 63 A/cm^2 shows clear

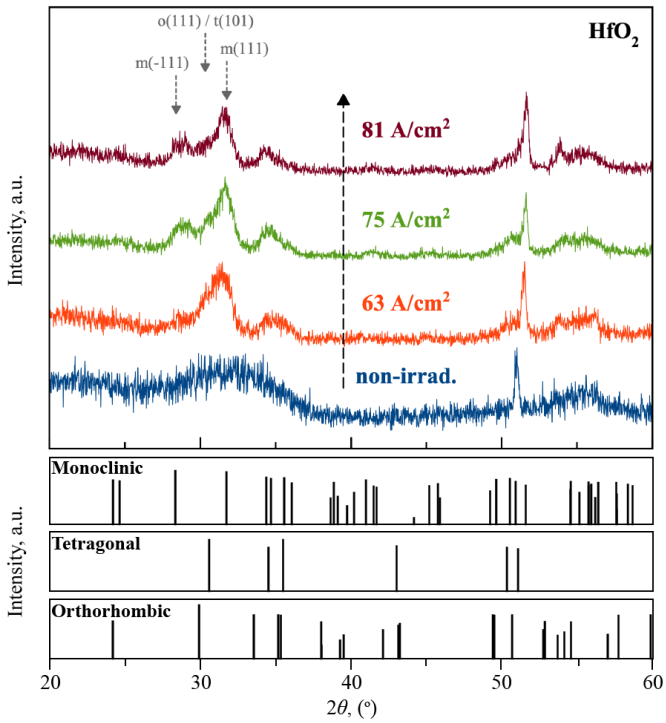


Figure 5.7. GIXRD measurements showing crystallization of HfO_2 after irradiation with pulsed high intensity proton beam of different current density (top), and XRD patterns for the monoclinic, tetragonal and orthorhombic phases (bottom) obtained from powder diffraction files (PDF).

diffraction peaks, all attributed to the t-phase. The main peak at 30.5° is quite symmetric, with no observable contribution from the cubic (c-) phase, indicating that the resulting thin film mostly consists of tetragonal zirconia. With an increase of proton beam intensity, the c-phase is formed, which is evidenced by a peak emerging at 31.5° in both the 73 A/cm^2 and 81 A/cm^2 samples.

To study the IPIB induced crystallization of HZO, the corresponding samples were grown using Fiji G2 ALD system at Nazarbayev University due to temporary unavailability of the previously used Oxford FlexAl PEALD system. The main difference between the two ALD systems is that the Fiji G2 uses a thermal ALD process, in which H_2O precursor is used, unlike O_2 plasma in the FlexAl. The Hf- and Zr-containing precursors were the same as those used in all previous experiments.

Figure 5.9 shows the GIXRD measurement results obtained for $Hf_xZr_{1-x}O_2$ grown on a silicon substrate and irradiated with current densities of 63 A/cm^2 and 75 A/cm^2. The two spectra look visually similar, but two observations can be still made. (1)

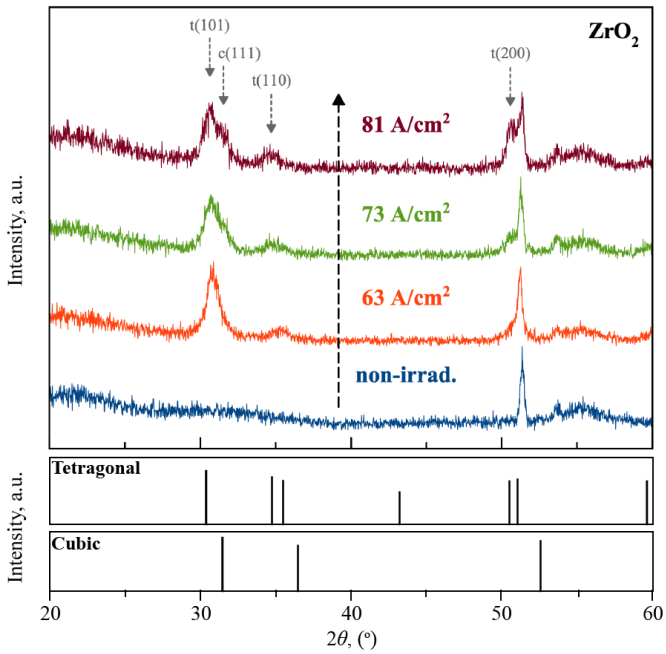


Figure 5.8. GIXRD measurements showing crystallization of ZrO_2 after irradiation with pulsed high intensity proton beam of different current density (top), and XRD patterns for the tetragonal and cubic phases (bottom) obtained from powder diffraction files (PDF).

The monoclinic peak at 28° appears in the sample with higher irradiation intensity. (2) A shoulder on the right side of the main peak at 30° becomes more pronounced for the sample irradiated with J = 75 A/cm^2. Both changes can be attributed to an increasing fraction of the monoclinic phase. Samples irradiated with J = 81 A/cm^2 and higher were visually damaged. This is in contrast to HfO_2 and ZrO_2 samples that were able to withstand current densities up to 90 A/cm^2. A possible explanation for the changed behaviour can be that HZO is more susceptible to high temperature annealing. This also results in a significantly lower HZO crystallization temperature (400 - 600 °C) compared to doped HfO_2 (can be as high as 1000 °C) [201].

In addition to HfO_2, ZrO_2, and HZO, we also studied the IPIB-induced crystallization of the samples used for RTA, namely TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN multilayer stacks with HZO thickness of 6 nm. Surprisingly, no crystallization was observed for this class of samples, when irradiated with current densities up to 250 A/cm^2.

Based on the results obtained so far, we believe that materials modification using IPIBs is a promising technique, providing unique capabilities, such as super-fast heating and super-fast cooling. The latter can be used to study the ferroelectric phase formation during the cool down step, which we think is an understudied topic in the

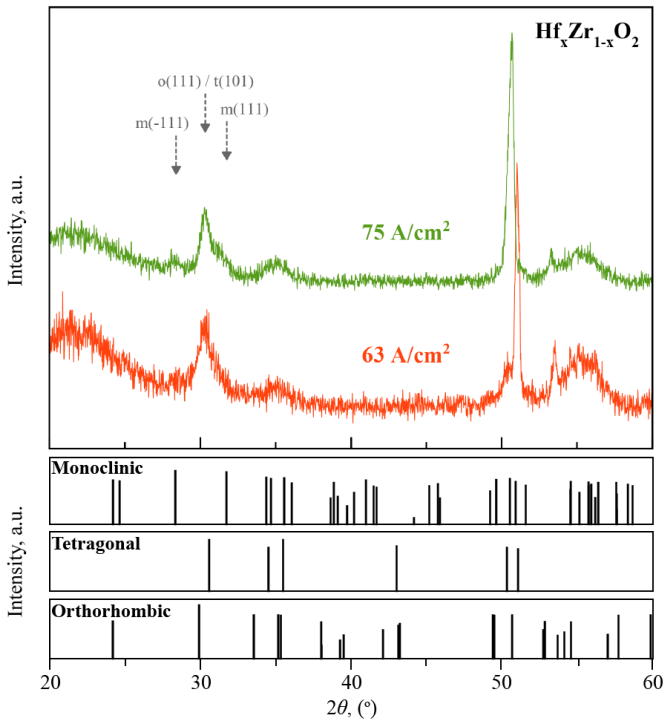


Figure 5.9. GIXRD measurements showing crystallization of $Hf_xZr_{1-x}O_2$ after irradiation with pulsed high intensity proton beam of different current density (top), and XRD patterns for the monoclinic, tetragonal and orthorhombic phases (bottom) obtained from powder diffraction files (PDF).

literature. It is also interesting to point out that the IPIB-based annealing process has an ultra-low thermal budget, since the heating takes place within only 80 ns (proton beam pulse width), while the cooling happens in the next hundreds to thousands of nanoseconds after irradiation. Conventional RTA cannot provide such high ramp and cool down rates, making it impossible to anneal materials deposited on, for example, flexible polymer substrates. Somewhat similar results were obtained by using millisecond flash lamp pulses [111], where similar changes in GIXRD pattern of $Hf_xZr_{1-x}O_2$ were observed, but the thermal budget of this technique is still higher, so the IPIB-based annealing might be another technique to treat temperature sensitive, low melting point materials. In addition, using IPIB together with shadow masks could pave the way to the formation of crystallized regions of any arbitrary shape and anywhere on the wafer by irradiating and annealing only specific regions not covered with the shadow mask. However, the irradiation parameters would need to be tuned so that the heating occurs closer to the surface of the substrate, e.g. by using heavier ions.

Notes

[7]XPS measurements were performed with the help of Michael Elowson (Berkeley Lab).

[8]XRR measurements were performed with the help of Arman Tuigynbek (Nazarbayev University).

[9]GIXRD measurements were performed with the help of Arman Tuigynbek (Nazarbayev University) and Gulnur Akhtanova (Nazarbayev University).

[10]Crystallography Open Database available at http://www.crystallography.net/.

[11]Powder Diffraction File card from the International Center for Diffraction Data (ICDD).

[12]Thanks to Prof. Lane Martin (UC Berkeley) for the provided access to the ferroelectric tester and Dr. Shishir Pandya and Gabriel Velarde for the equipment training and helpful discussions.

[13]The irradidation on INURA accelerator was performed by Dr. Marat Kaikanov (Nazarbayev University).

[14]GIXRD measurements presented in this section are partially based on the research activities of and obtained by Arman Tuigynbek (Nazarbayev University).

6. Conclusions and Outlook

The overarching theme of the work presented here, is to develop materials and methods for the realization of next-generation, energy-efficient, low-power electronic devices as Moore's law and Dennard scaling are pushed to their limits. Many possible solutions exist that can be divided into two groups: (a) synthesis and integration of novel nanomaterials into electronics; and (b) development of novel advanced device architectures. The latter approach also requires the synthesis of novel materials and their co-integration. In this work a number of novel materials were synthesized, which includes semiconductors, such as 1D single-walled carbon nanotubes and 2D transition metal dichalcogenides, as well as ferroelectrics, such as $Hf_{0.5}Zr_{0.5}O_2$. These low-dimensional semiconductors can help to overcome short-channel effects seen when scaling traditional semiconductor FET devices, while their integration with ferroelectrics can help to achieve more efficient switching by taking advantage of the negative capacitance effect. Although, we were not able to experimentally demonstrate the negative capacitance transistor yet, a number of novel and useful processes were developed. Two sections below will summarize the obtained results, and provide a roadmap towards realization of the ultimate goal.

6.1. Summary and conclusions

Carbon nanotubes. A thermal CVD-based process was used to grow single-walled carbon nanotubes on regular Si/SiO_2 and quartz substrates. The former can be used when a bottom gate is required, whereas the latter is advantageous for graphoepitaxial growth. Synthesized nanotubes were integrated into top-gated and bottom gated FETs. In addition, a structure with suspended CNTs, and the corresponding nanofabrication process flow were demonstrated. The novelty of this work is in the TiO_2-based nanotube surface pretreatment technique that enables subsequent uniform and conformal coating with various ALD oxides. We

show that CNTs can be easily coated with TiO_2 by depositing metallic Ti and oxidizing it in ambient atmosphere. TiO_2 did not degrade the nanotube properties, as was evidenced with Raman and electron transport studies. The demonstrated pretreatment strategy not only serves as a buffer layer for ALD coating, but also increases the overall dielectric permittivity of an all-oxide higher-κ dielectric, improving its EOT. Processes developed for CNT synthesis, their integration into devices and surface preparation for subsequent coating with high-κ dielectrics and ferroelectrics are VLSI compatible, and based on equipment readily available in typical nanofabrication facilities.

Transition metal dichalcogenides. A novel technique that we termed "lateral conversion" was developed. The process was used to synhtesize few-layer WS_2 and further extended to grow MoS_2, $MoSe_2$, WSe_2, and vertically stacked WS_2/SiO_2 multilayers, showing its flexibility. It relies on chalcogenation of ALD metal-oxide, sandwiched between inert silica layers. Lithographic patterning ensures that the conversion proceeds only laterally, starting along the predefined exposed edge and propagating between the silica layers. ALD allowed precise control of the metal oxide thickness, which translated into a controlled number of TMD layers, and lithographic-compatibility enabled wafer-scale fabrication using this method. The thinnest achieved material was a highly crystalline film composed of 4 ± 1 Van der Waals layers, having a high degree of alignment within the plane of the confined area. The capping layer protects the delicate nanomaterial from oxidation and contamination from the subsequent microfabrication steps, and can also be used as a buffer layer for subsequent ALD coating of other materials. This overcomes the well-known difficulty of growing ALD thin films on pristine TMD surfaces.

Ferroelectrics. Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ was synthesized using ALD. The thin film stoichiometry was controlled by changing the HfO_2-to-ZrO_2 ALD cycle ratio, and was optimized to obtain a Hf-to-Zr ratio of 1:1. Next, an optimal RTA annealing temperature was found to maximize the orthorhombic phase fraction. The latter was measured using GIXRD and extracted from Rietveld refinement. Ferroelectric measurements confirmed that the samples annealed at 550 °C possess the highest remnant polarization value of $2P_r = 32\ \mu C/cm^2$ (after conditioning). The developed process is ready for integration of the ferroelectric into CNFET devices to realize the negative capacitance effect.

IPIBs were used as an alternative to RTA, to crystallize initially amorphous ALD $Hf_{0.5}Zr_{0.5}O_2$. This application of IPIBs was shown for the first time and, we believe,

will inspire other ideas where super-fast heating and cooling are required. Materials treatment with IPIBs provides ultra-low thermal budget annealing due to the very low pulse width, which for our system is 80 ns. The annealing temperature is reached within the same period of time. Our first experiments on irradiation with protons showed that it is possible to crystallize HfO_2, ZrO_2, and $Hf_{0.5}Zr_{0.5}O_2$ thin films. GIXRD measurements indicate that it is possible to stabilize different phases in these materials by varying the beam current density, which means that the process is controllable, but still requires fine tuning of the irradiation parameters and/or the materials synthesis processes, to stabilize/maximize orthorhombic phase, giving rise to ferroelectricity in HfO_2-based ferroelectrics.

6.2. Outlook

Carbon nanotubes. The ultimate goal is to demonstrate gate-all-around CNTs FET with negative capacitance. This will be the first demonstration of such device. The most effective gate geometry will meet one of the most efficient device architectures. Firstly, to achieve this goal, the developed processes for CNT synthesis, suspended CNT fabrication and CNT surface pretreatment should be used to fabricate a device with gate-all-around (GAA) geometry. This geometry will maximize the electrostatic coupling between the gate (ALD TiN) and the channel (CNT). In addition, the wrap-around gate will passivate the CNT surface, protecting it from the environment and improving the device-to-device variability. Next, ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ needs to be integrated into the gate stack to demonstrate a negative capacitance CNFET. All device components should be optimized to achieve capacitive matching and to stabilize the ferroelectric capacitor [9], which will ensure the absence of hysteretic behavior in the transistor transport characteristics.

Transition metal dichalcogenides. Two major goals are set: (1) synthesis of a monolayer TMD materials using lateral conversion; and (2) the demonstration of TMD-based negative capacitance transistor with an improved performance. To achieve the first goal the reactions governing lateral conversion should be further studied, for instance, the fate of the reaction byproducts or their impact on the grain size. Next, electrodes should be integrated to demonstrate a working transistor. The structure resulting from the lateral conversion (capped TMD with exposed edges) are particularly interesting for establishing edge contacts that were shown to have a lower contact resistance to 2D materials [202, 203]. To achieve the second goal, ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ should be integrated and a top-gated

device should be fabricated. Thanks to pre-existing capping layer, the ALD nucleation of $Hf_{0.5}Zr_{0.5}O_2$ or other ALD oxides, required for negative capacitance stabilization, should not be a problem. The FET can be fabricated using the photolithography for microscale devices or e-beam lithography to demonstrate a single-grain transistor.

Ferroelectrics. The main goal of future studies of ferroelectrics, in the context of this project, should be their properties optimization and integration into negative capacitance transistors. The process for ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ fabrication using RTA is developed and ready to be used for the thin film integration into CNT or TMD based FETs. However, the impact of RTA annealing on other materials, comprising the FET, should be studied, as interdiffusion, dopant redistribution (e.g. in Si), contact resistance degradation can be one of the possible drawbacks of the technique.

IPIB-induced crystallization of $Hf_{0.5}Zr_{0.5}O_2$ needs to be characterized on a ferroelectric tester and optimized accordingly. Different irradiation parameters, such beam current density, ion species, number of pulses, etc. need to be fine-tuned to stabilize and maximize the orthorhombic phase fraction and finally hit the ferroelectric window. In addition, $Hf_{0.5}Zr_{0.5}O_2$ thickness or substrate type should be tuned as well. The latter seems interesting to study and control the cool down rate that should depend on the thermal conductivity of the substrate. The simulation of the heating effects induced by IPIB interaction with thin films should help to advance the understanding of the underlying phenomena and to find the optimal irradiation settings. Next, $Hf_{0.5}Zr_{0.5}O_2$ should be integrated into CNT and TMD based FETs and the impact of IPIB treatment should be studied. In particular, the impact of the irradiation on the semiconducting channel (e.g. defects creation) and its radiation hardness should be studied. To realize the full potential of the IPIBs and their ultra-low thermal budget annealing capability, a device on flexible substrate can be demonstrated.

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Appendix A. Nanofabrication process flows

The developed lithographic recipe, which was used multiple times for the fabrication of different structures and was referred as “Standard ma-N 1420 recipe”:

Standard ma-N 1420 recipe		
A	Spin-coat	Small samples: Photoresist: ma-N 1420; 4000 RPM, 45 sec
		Wafers: Photoresist: ma-N 1420; (1) 2000 RPM, acceleration - 500 RPM/s, 10 sec; (2) 4000 RPM, acceleration - 1500 RPM/sec, 45 sec
B	Bake	100^{o}C, 2 min
C	Expose	90 mJ/cm^2 (e.g. 14 mW/cm^2 × 6.4 s)
D	Outgas	15 min, in air
E	Develop	ma-D 533/s: RT, 50 sec for small samples // 65-70 sec for 4’’ wafers, only last 10 sec with agitation Rinse in H_2O: RT, 1+ min, with agitation

A1. Carbon nanotube field effect transistor fabrication

1. Preparation		
1.1	Dicing	4’’ wafer saw dicing into 10.5 × 10.5 mm dies. Each substrate was half-diced into four 5.25 × 5.25 mm chips to a depth of 0.265 μm
1.2	Cleaning	Acetone – 5 min, RT, US3 IPA – 2 min
2. Markers Fabrication		
2.1	Lithography	Standard ma-N 1420 recipe
2.2	Thermal evaporation	Cr: nom. 60 nm (= 30 nm)* 0.6 Å /s, 5 × 10^{-6} mbar, without rotation. *tooling factor = 0.5-0.6
2.3	Lift-off	Acetone: 3 min, RT, US2 IPA: 2 min

3. Catalyst Islands Fabrication		
3.1	Lithography	Standard ma-N 1420 recipe
3.2	RIE	RIE: O_2 (2 sccm) + Ar (10 sccm), 100 W, 20 sec
3.3	Thermal evaporation	Fe: nom. 2 Å (~1 Å)* 0.1 Å /s, 5×10^{-6} mbar, w/o rot. *tooling factor = 0.5-0.6
3.4	Lift-off	Acetone: 30 min, 50°C, no US IPA: 2 min
4. CNTs synthesis		
4.1	Calcination	Air, 50 sccm, 20-620°C, 3 Torr
4.2	Purge	N_2, 200 sccm, ~620-650°C, 3-120 Torr
4.3	Reduction	H_2, 50 sccm, ~650C-865°C, ~20 min, 120 Torr
4.4	Growth	H_2, 50 sccm, CH_4 - 500 sccm, 865°C, 30 min, 350 Torr
4.5	Cool down	H_2, 50 sccm, 865°C to RT, ~60 min, 3 Torr
5. Source and Drain electrodes fabrication		
5.1	Lithography	Standard ma-N 1420 recipe
5.2	Thermal evaporation	Cr: nom 10 nm (=5 nm),* 0.6 Å /s, 5×10^{-6} mbar, w/o rot.; Au: nom 80 nm (=40 nm),* 2-2.5 Å /s, 5×10^{-6} mbar, w/o rot. *tooling factor = 0.5-0.6
5.3	Lift-off	Acetone: 1 h, 50°C, no US Acetone: 10 min, 50°C, no US IPA: 2 min
6. CNTs suspending		
6.1	SiO2 etching	Wetting: no Etching: BOE HF 1:6, 70 sec Rinsing: H_2O: 10 min, RT Transfer: Acetone: 5 min, RT
6.1	Quartz etching*	Wetting: IPA:H_2O - 1:5, 1 min; H_2O, 1 min Etching: BOE HF 1:1, 5 min Rinsing: H_2O: 8 min Transfer: Acetone: 5 min *not very reproducible
6.2	Critical Point Drying	Exchange Acetone with liq. CO_2 8-10 times at 6-10°C CPD at 31°C+, 75.4 mbar+

Abbreviations: w/ – with; w/o – without; rot. – rotation; RT – room temperature; BOE – buffered oxide etch; US – ultra-sonication (number is the relative power, out of 9).

A2. Transition metal dichalcogenides synthesis

1. Deposition of oxides stack			
1.1	Conditioning:	Do 100 cycles of WO_x or MoO_x on test wafer	Check the deposition rate with ellipsometer
1.2	A. ALD of WO_x	Precursors: bis(tert-butylimido)-bis-(dimethylamido) tungsten) and O_2 plasma Temperature: 300°C	Deposition rate ~ 0.5 Å/s. Wait for base pressure to reach 5×10^{-6} mbar before the deposition.
	B. ALD of MO_x	Precursors: molybdenum hexacarbonyl and O_2 plasma Temperature: 300°C	Deposition rate ~ 0.7 Å/s. Wait for base pressure to reach 5×10^{-6} mbar before the deposition.
1.3	ALD of SiO_2	Precursors: 3DMAT and O_2 plasma Temperature: 300°C	100 cycles ~5 nm Wait for base pressure to reach 5×10^{-6} mbar before the deposition.
1.4	PECVD of SiO_2	Precursors: 1% SiH_4 in Ar (1182 sccm) and N_2O (710 sccm) Temperature: 350°C, Plasma: 20 W	54 sec = 50 nm
2. Patterning			
2.1	Lithography	Standard ma-N 1420 recipe	
2.2	Descum	RIE descum O_2 plasma: 2 min, 150 W, O_2: 50 sccm, 100 mTorr	
2.3	Etch	Etch: 100 W, CHF_3: 35 sccm, Ar: 25 sccm, 30 mTorr Etch time: 5 min (etch rate 19 nm/min)	Check depth with profilometer
2.4	Photoresist removal	Acetone, RT, 10 min, US4 IPA 1 min and blow dry with N_2	
2.5	Polymer removal	RIE O_2 plasma: 10 min, 150 W, O_2: 50 sccm, 100 mTorr	
2.6	Dicing	Cleave into smaller dies or dice	
2.7	PECVD of SiO_2 (backside, only for Si/SiO_2 samples)	Precursors: 1% SiH_4 in Ar (1182 sccm) and N_2O (710 sccm) Temperature: 350°C, Plasma: 20 W	Batch 1: 45 sec = 52.5 nm Batch 2: 50 sec = 52.5 nm Deposition rates: B1 - 70 nm/min, B2 - 63 nm/min

A3. Ferroelectric hafnium zirconium oxide fabrication

1. Deposition of MIM stack			
1.1	ALD of TiN	Precursors: TDMAT and N_2 plasma Temperature: 250°C	Deposition rate ~ 0.5 Å/s. 200 cyc. = 10 nm Wait for base pressure to reach 5×10^{-6} mbar before the deposition.
1.2	ALD of $Hf_xZr_{1-x}O_2$	HfO_2 precursors: TEMAH and O_2 plasma ZrO_2 precursors: TDMAZ and O_2 plasma Temperature: 250°C	Deposition rate depends on super-cycle composition. Wait for base pressure to reach 5×10^{-6} mbar before the deposition.
1.3	ALD of TiN	Precursors: TDMAT and N_2 plasma Temperature: 250°C	Deposition rate ~ 0.5 Å/s 200 cyc. = 10 nm
2A. Rapid Thermal Annealing			
2A	RTA at 450-650°C under N_2 flow (1 slm) at 1 atm for 1 min with an average temperature ramp rate of 20°C/min. Cool down under N_2 flow (3 slm). Remove samples at 120°C (or lower) to avoid TiN oxidation.		
2B. IPIB irradiation			
2B	Irradiation on INURA accelerator. Details in Appendix B.		
3. Patterning			
3.1	Lithography	Standard ma-N 1420 recipe	
3.2	Etch	Etch in $NH_4OH:H_2O_2:H_2O$ = 1:2:40 at 50°C for 5 min	Add NH_4OH into H_2O and heat to 50°C. At 50°C add SLOWLY H_2O_2. Attention! The order in which to add chemicals is important, since the reaction is very dangerous and requires additional training.
3.3	Photoresist removal	Acetone, RT, 10 min, ultrasonication - power 4 IPA 1 min and blow dry with N_2	

Appendix B. IPIB irradiation parameters

Sample	ID	U_{diode}, V	J, A/cm^2	P, MW/cm^2
HfO_2	H1	427.6	63.0	26.9
	H2	453.7	75.2	34.1
	H3	525.4	81.4	42.8
ZrO_2	Z1	428.3	63.1	27.0
	Z2	458.7	73.4	33.7
	Z3	500.4	84.5	42.3
$Hf_{0.5}Zr_{0.5}O_2$	HZ1-1	429.1	62.0	26.6
	HZ1-2	454.5	74.3	33.8
	HZ2-1	431.2	62.0	26.7
	HZ2-2	461.4	73.4	33.8
	HZ4-1	432.4	62.0	26.8
	HZ4-2	454.5	74.3	33.8

Publications and projects

Publications

1. Kemelbay, A.; Kuntubek, A.; Chang, N.; Chen, C.; Kastl, C.; Inglezakis, V.; Tikhonov, A.; Schwartzberg, A.; Aloni, S.; Kuykendall, T. **Lithographically Defined Synthesis of Transition Metal Dichalcogenides.** 2D Mater. 2019, 6 (4), 045055. DOI:10.1088/2053-1583/ab402a;
2. Kemelbay, A.; Tikhonov, A.; Aloni, S.; Kuykendall, T. R. **Conformal High-κ Dielectric Coating of Suspended Single-Walled Carbon Nanotubes by Atomic Layer Deposition.** Nanomaterials 2019, 9 (8), 1085. DOI:10.3390/nano9081085.

Authored research proposals (peer-reviewed)

1. **Controlled synthesis of TMD materials by lateral conversion** – Primary researcher and co-author. The Molecular Foundry user proposal, 2019. Funding agency: United States Department of Energy. PI – Dr. Tevye Kuykendall.
2. **Ferroelectric hafnia formation assisted by intense pulsed beams** – Primary researcher and co-author. The Molecular Foundry user proposal, 2018. Funding agency: United States Department of Energy. PI – Dr. Alexander Tikhonov.
3. **Fabrication and characterization of high-performance single-walled carbon nanotubes field effect transistors** – Primary researcher and co-author. The Molecular Foundry user proposal, 2016. Funding agency: United States Department of Energy. PI – Dr. Tevye Kuykendall.
4. **Energy efficient carbon nanotubes based nanoelectronics** – Co-Principle investigator and co-author. Research grant, 2015. Funding agency: Ministry of Educations and Science of the Republic of Kazakhstan. PI – Dr. Raymond Whitby.

Seminars and presentations

1. **Lithographically defined synthesis of transition metal dichalcogenides.** Poster presentation (accepted), 7th Thermal Probe Workshop (Zürich,

Switzerland) – March 17-18, 2020.

2. **Fabrication and integration of engineered nanomaterials for advanced device architectures.** Nanofabrication Facility seminar, Molecular Foundry (Berkeley, CA) – October 7, 2019.
3. **Negative capacitance field effect transistors.** Nanofabrication Facility seminar, Molecular Foundry (Berkeley, CA) – November 5, 2018.
4. **Carbon nanotube field effect transistors.** Inorganic Facility seminar, Molecular Foundry (Berkeley, CA) – July 7, 2016.
5. **1D and 2D materials-based electronics.** A series of talks. Accelerator group and Nazarbayev University doctoral seminars, Nazarbayev University (Astana, Kazakhstan) – 2016-2019.

Co-supervised undergraduate students

1. Aldiyar Kuntubek (Nazarbayev University School of Engineering). **Controlled synthesis of tungsten disulfide by lateral conversion.** The Molecular Foundry summer internships, 2018 and 2019. Supervisor and host: Dr. Tevye Kuykendal.
2. Bekassyl Battalgazy (Nazarbayev University School of Engineering). **Synthetic process for conversion of transition metal dichalcogenides.** The Molecular Foundry summer internship, 2019. Supervisor and host: Dr. Tevye Kuykendal.

Curriculum vitae

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Education

- **MSc. ETH in Micro- and Nanosystems** **2012 – 2013**

ETH Zurich - Swiss Federal Institute of Technology Zurich (Switzerland)
Recipient of the "Bolashak" International Scholarship

- **B. Tech. (Hons.) in Applied Physics** **2007 – 2011**

Eurasian National University, Kazakhstan

Work Experience

- **Graduate student research assistant**, Berkeley Lab (USA) **2018 – 2019**
- **Researcher**, Nazarbayev University (NU, Kazakhstan) **since Feb 2014**

Laboratory and Equipment Experience

Nanofabrication & synthesis:

- Thin films deposition: ALD, ALD on 1D and 2D materials, PVD (thermal, e-beam, sputtering), PECVD;
- Etching: Dry – cryogenic-ICP, RIE; and Wet – HF, TiN etching, Al_2O_3 etching, and other;
- Nanomaterials synthesis: graphoepitaxial CVD growth of CNTs; TMD materials – WS_2/Se_2, MoS_2/Se_2 and other;
- Other processes: UV lithography and mask design, CPD, back-end processes.

Characterization:

- Structural: SEM, AFM, (GI-)XRD, XPS, EDS, Raman spectroscopy, ellipsometry;
- Electrical characterization of nanoscale devices: FETs, thin film, ferroelectric and Hall measurements.

Experience in working in Nanofabrication facilities:

- **Nanofabrication Facility, Molecular Foundry, Berkeley Lab (USA)**

Designed recipes for ALD system; trained users on SEM, profilometer; assisted with the maintenance of PECVD, RIE, CPD, lithography and other equipment; worked in multidisciplinary and multinational teams.

- **Nazarbayev University cleanroom (under construction)**

Designed cleanroom and helped to create policies; configured and developed recipes for ALD system; configured and assisted with technical part of the procurement of ALD, XPS, ellipsometer, profilometer, multiple tools for electronic characterization.

- **FIRST Center for Micro- and Nanoscience user, ETH Zurich (Switzerland)**