In situ doping of silicon carbide semiconductor via epitaxy

Maksym Myronov

Physics Department, University of Warwick, Coventry, CV4 7AL, UK

E-mail: *M.Myronov@warwikc.ac.uk*

Silicon carbide (SiC) is a wide bandgap semiconductor which can operate at high temperatures and resist chemicals and radiation, making it ideal for applications in a range of harsh environments [1]. Among over 200 polytypes of SiC, only cubic silicon carbide (3C-SiC) can be heteroepitaxially grown on Si. However, there are still no commercial 3C-SiC devices available due to its cost and issues with growth and leakage currents [2]. While leakage into the underlying Si can be managed by transferring the 3C-SiC layer to an insulating substrate, this process is difficult to scale and integrate into current technologies [3].

Achieving high levels of electrically active dopants in 3C-SiC epilayers is crucial for the formation of low resistance Ohmic contacts, controlling material conductivity and forming more intricate structures such as field effect transistors or PiN diodes. High energy ion implantation at elevated temperatures is typically employed for SiC polytypes, however, this can be an issue with heteroepitaxially grown 3C-SiC/Si material as the upper annealing temperature is limited by the melting point of the Si wafer. The maximum achievable impurity levels through ion implantation of n- or p-type dopants within 3C-SiC are around 6×10^{20} cm^{-3}, however, electrical activation at this level of implantation can be around 12%, saturating the free donors at ~7×10^{19} cm^{-3} [4] and leaving a high number of interstitial impurities, clusters and defects in the crystal.

Recently invented, the low temperature growth of 3C-SiC offers a commercially viable, high volume production method for 3C-SiC epitaxial growth [5]. The process enables the accurate control of the epilayer electrical properties through in-situ doping with standard Si based dopants and also offers the opportunity to grow 3C-SiC on non-standard for SiC substrates such as silicon-on-insulator (SOI) or patterned with SiO_2 Si wafers. As a consequence, extremely high levels of electrically active phosphorus (P) dopants have been introduced into 3C-SiC during epitaxial growth with 100% electrical activation up to unprecedently high level of ~2×10^{20} cm^{-3}. It results in the highest electrical conductivity of SiC material obtained so far. The process offers extreme control over the 3C-SiC electrical properties without relying on post-growth ion implantation and very high temperature annealing. Low temperature epitaxy enables the growth of doped 3C-SiC on silicon-on-insulator (SOI) substrates for device applications at high temperatures, avoiding the issue of leakage current into the Si substrate.

[1] N. G. Wright and A. B. Horsfall, Journal of Physics D: Applied Physics 40, 6345 (2007)
[2] F. La Via, Silicon Carbide Epitaxy (Research Signpost, Kerala, 2012)
[3] A. R. Md Foisal, H.-P. Phan, T. Kozeki, T. Dinh, K. N. Tuan, A. Qamar, M. Lobino, T. Namazu, and D. V. Dao, RSC Advances 6, 87124 (2016)
[4] F. Li, Y. Sharma, V. Shah, M. Jennings, A. Perez-Tomas, M. Myronov, C. Fisher, D. Leadley, and P. Mawby, Appl. Surf. Sci. 353, 958 (2015)
[5] M. Myronov, G. Colston et al., GB1513014.9 (2015).