

# Feature extraction without learning in an analog Spatial Pooler memristive-CMOS circuit design of Hierarchical Temporal Memory

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Received: date / Accepted: date

**Abstract** Hierarchical Temporal Memory (HTM) is a neuromorphic algorithm that emulates sparsity, hierarchy and modularity resembling the working principles of neocortex. Feature encoding is an important step to create sparse binary patterns. This sparsity is introduced by the binary weights and random weight assignment in the initialization stage of the HTM. We propose the alternative deterministic method for the HTM initialization stage, which connects the HTM weights to the input data and preserves natural sparsity of the input information. Further, we introduce the hardware implementation of the deterministic approach and compare it to the traditional HTM and existing hardware implementation. We test the proposed approach on the face recognition problem and show that it outperforms the conventional HTM approach.

**Keywords** Hierarchical Temporal Memory · Memristors · Spatial Pooler · Rule based approach · Analog circuits

## 1 Introduction

Hierarchical Temporal Memory (HTM) is a neuromorphic algorithm that emulates the structure and functionality of the cortical neural networks [11]. HTM can serve as a tool for intelligent data processing in edge computing devices. The increase in the number of edge computing devices and Internet of things (IoT) applications in the recent years lead to the demand to introduce on sensor processing using analog hardware.

Therefore, the translation of the HTM algorithm into analog hardware can produce the promising solution to the computational speed problems [2, 7, 12].

HTM is divided into two parts: HTM Spatial Pooler (HTM SP) and HTM Temporal Memory (HTM TM). The HTM SP has been proven to be useful for visual data processing and classification problems, whereas the HTM TM is used as a prediction and learning algorithm. In this work, we focus on the SP part of HTM. The main functionality of the HTM SP is to form the sparse distributed pattern from the input data and perform the feature encoding. The recent works show that it is useful for feature extraction and pattern recognition problems [12].

In this work, we investigate the initialization stage of the HTM SP and proposed the rule-based deterministic approach instead of the random weight approach for the initial weight assignment. The main purpose of the rule-based approach is to connect the input to the HTM weights, which allows to preserve natural sparsity and structural information from the inputs. Moreover, we propose the hardware implementation for the rule-based approach and compare it with the conventional random weight approach in terms of power dissipation and on-chip area requirements. Also, we test the system level implementation of the proposed approach on the face recognition problem and show the improvements in the recognition accuracy [10, 12].

This paper is organized into 8 sections. Section 2 provides the overview of the HTM algorithm and introduces the mathematical framework of HTM. Section 3 illustrates the difference between the conventional approach and the proposed rule-based approach. Section 4 discussed the hardware implementation of the HTM SP and illustrates the proposed hardware architecture. Section 5 shows how system level HTM SP algorithm

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can be used for the face recognition problem. Section 6 shows the results of the system-level and analog hardware implementations. Section 7 provided the discussion of the proposed rule-based method and corresponding analog hardware. Section 8 concludes the paper.

## 2 Background

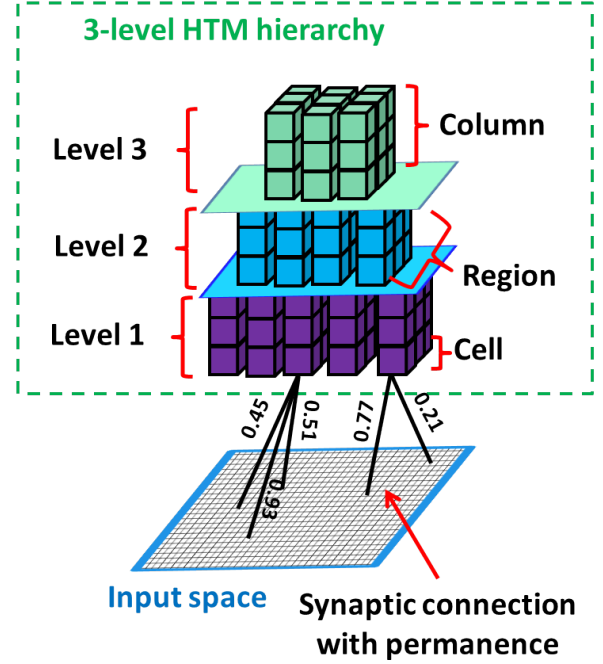
### 2.1 HTM overview

HTM is a neuromorphic machine learning algorithm that emulates the architecture and biological functionality of the neocortex in a human brain [6]. HTM algorithm focuses on the sparse distributed representation of the information, encoding of the input sensory data, learning and prediction making based on the temporal changes in the input data and previous inputs [5].

As discussed in the introduction section, the original HTM algorithm is divided into two main parts: Spatial Pooler (SP) and Temporal Memory (TM). The main purpose of the HTM SP is the encoding and producing sparse distributed representation (SDR) of the input data. This is useful for the feature extraction and visual data classification purposes [15]. The applications of the HTM SP include handwritten digits recognition [4], face recognition [12], speech recognition [11], gender classification [10], object categorization [2] and natural language processing [9]. The HTM TM is responsible for the learning and processing of temporal patterns and can be used for the prediction taking into account previous experiences [12].

HTM has a hierarchical structure, and an example 3-level HTM structure is shown in Fig. 1. Each level of HTM consists of certain regions with columns, and each column is comprised of cells. The columns in HTM is equivalent to neurons. The columns are connected to the input space with the connections through the dendrite segment with several synapses. Each synapse has a certain weight called synaptic permanence.

The HTM SP consists of four main phases: initialization, calculation of overlap value, inhibition and learning process [6]. In the initialization phase, the potential inputs in the HTM regions are identified and certain number of columns within the HTM regions are selected [3]. The potential input columns are those columns, which are considered to receive the input data. The inputs are connected to the potential input columns through the dendrite containing with potential synapses with certain permanence value (weight). In the initialization phase, the weights are assigned randomly following the uniform random distribution approach. If this weight (permanence value) is greater than the threshold, the potential synapse is considered to be connected.



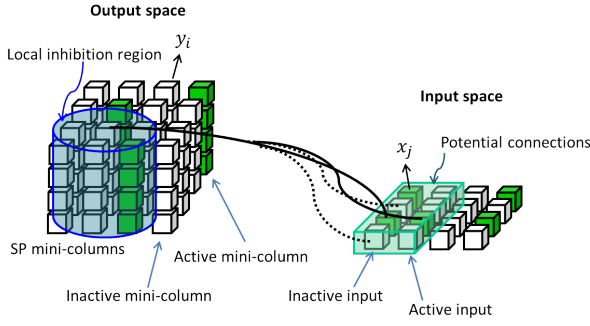
**Fig. 1** The hierarchical structure of HTM. The example shows 3-level HTM, where each level consists of the regions with columns, and columns are created from the cells. HTM is connected to the input space by the synapses.

If the connected synapse is connected to the active input it is considered to be active connected. In the overlap phase the number of active connected synapses is computed. In the inhibition stage, the  $k$  columns with highest overlap values become active (assigned as high, 1), and the other columns are inhibited (assigned as low, 0). In the learning phase, the HTM SP weights of the synapses are updated based on the Hebb's learning rules. After the update process, all phases, except initialization phase, are repeated.

### 2.2 Mathematical framework of the HTM SP

The arrangement of the input of the HTM SP and output space that is arranged into mini-columns is shown in Fig.2. The parameter  $x_j$  denotes the  $j$ -th input neuron in the input space, and the  $y_i$  refers to the  $i$ th output SP mini-column in the output space, which is connected to the region of the input space with the potential connections.

The synapse of the  $i$ -th SP mini-column is located in a hypercube of the input space centered at  $x_i^c$  with the edge length of  $\gamma$ . The potential connections are defined in Eq.1, where  $\mathcal{U}(x_j; x_i^c, \gamma) = 1, \forall x_j \in (x_i^c, \gamma)$ , and  $z_{ij} \sim U(0, 1)$ ,  $z$  is selected randomly and follows the uniform distribution rule ( $U$  has a range:  $[0, 1]$ ) [8, 12]. The parameter  $\rho$  denotes the assigned percentage of



**Fig. 2** The arrangement of the HTM SP input space and the output space, containing the mini-columns.

inputs that are considered to be potential connections within the hypercube of the input space.

$$PI(i) = \{j | \iota(x_j; x_i^c, \gamma) \text{ and } (z_{ij} < \rho)\} \quad (1)$$

For all synapses the synaptic permanence value (weight) is assigned. The synaptic permanence from the  $j$ -th input to the  $i$ -th SP mini-column is represented by the matrix  $\mathbf{S}_{ij} \in [0, 1]$  shown in Eq.2. If the synapse is located within the potential the region of potential inputs, the synaptic permanence value  $\mathbf{S}_{ij}$  is assigned as the uniform random distribution between 0 and 1; otherwise, the synaptic permanence is 0, so the synapse is not connected.

$$\mathbf{S}_{ij} = \begin{cases} U(0, 1) & \text{if } j \in PI(i) \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

All the connected synapses are represented by the binary matrix  $\mathbf{B}$  shown in Eq.3. Based on the synaptic permanence value, the synapse is either connected or not connected. If their value is greater the threshold value  $\theta_c$ , the synapse is connected and  $\mathbf{B} = 1$ , and vice versa. The threshold  $\theta_c$  shows the percentage of the connected synapses.

$$\mathbf{B}_{ij} = \begin{cases} 1 & \text{if } \mathbf{S}_{ij} \geq \theta_c \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

Equation 4 refers to the process, where the local inhibition neighborhood region  $\mathbf{N}_i$  of the HTM SP of the  $i$ -th SP mini-column is determined. The parameter  $\|y_i - y_j\|$  refers to the the Euclidean distance between the mini-columns  $i$  and  $j$ , and the parameter  $\phi$  controls the inhibition radius.

$$\mathbf{N}_i = \{j | \|y_i - y_j\| < \phi, i \neq j\} \quad (4)$$

In the overlap phase of the HTM SP, the activation of the SP mini-columns for a particular input pattern  $\mathbf{Z}$

is determined. The input overlap calculation is shown in Eq.5, where  $\beta_i$  is a boosting factor that refers to the excitability of the SP mini-column.

$$o_i = \beta_i \sum_j \mathbf{B}_{ij} \mathbf{Z}_j \quad (5)$$

In the inhibition phase, the activation of the SP mini-columns occurs. The activation depends of two conditions: the value of the input overlap of the SP mini-column should be above the threshold  $\theta_s$  and within the top  $s$  percent considering the other SP mini-columns in the inhibition neighborhood. The selection of the active column is shown in Eq.6, where the parameter  $\alpha_i$  is the activity of the SP mini-columns, *prctile* is a percentile function, and  $\mathbf{NO}(i) = \{o_j | j \in \mathbf{N}(i)\}$  with the target activation density  $s$ . The activation of the columns is implemented according to the  $k$ -winners-take-all rule considering all mini-columns in the particular neighborhood.

$$\alpha_i = 1, \text{ if } (o_i \geq \text{prctile}(\mathbf{NO}(i), 1 - s)) \text{ and } (o_i \geq \theta_s) \quad (6)$$

In the original HTM algorithm, the parameter  $k$ , can be changed based on the desired number of winning columns for a particular application [8]. However, in most of the existing hardware implementations of the HTM SP,  $k = 1$  due to the limitations of the Winner-Takes-All(WTA) circuits [7].

In the learning phase of the HTM SP, feed-forward connections are learned using Hebb's learning rule and the boosting factor is updated. The Hebb's rule for the connection learning implies that the permanence value of the connections is either increased or decreased by the value  $\rho$ . The update process of the boosting factor is performed considering time-average activity the SP mini-columns  $\bar{\alpha}_i(t)$  and recent activity of the SP mini-columns  $\alpha_i(t) > \bar{\alpha}_i(t)$  [8]. Eq.7 shows the calculation of the time-average activity of the SP mini-columns in time  $t$ , where  $T$  is the number of considered previous inputs, and  $\alpha_i(t)$  is a current activity the  $i$ -th mini-column.

$$\bar{\alpha}_i(t) = \frac{(T - 1) \times \bar{\alpha}_i(t - 1) + \alpha_i(t)}{T} \quad (7)$$

Equation 8 shows the calculation of the recent activity.

$$< \bar{\alpha}_i(t) > = \frac{1}{|\mathbf{N}(i)|} \sum_{j \in \mathbf{N}(i)} \bar{\alpha}_i(t) \quad (8)$$

Equation 9 refers to the update process of the boosting factor, where  $\eta$  controls the adaptation of the HTM SP.

$$\beta_i(t) = e^{-\eta(\bar{\alpha}_i(t) - \langle \bar{\alpha}_i(t) \rangle)} \quad (9)$$

### 3 Rule-based approach

To improve the initialization phase of the HTM SP, we proposed the rule-based approach for the weights assignment instead of the uniform weight distribution. In the rule-based approach, we establish the connection between the input space and the synaptic permanence values (weights of the synapses). The Eq. 10 shows how synaptic permanence weights are assigned in the rule based approach. Eq. 10 is used instead of Eq. 2 and Eq. 3.

$$\mathbf{S}_{ij} = \begin{cases} 1 & \text{if } j \in PI(i) \text{ and } PI(i) > \text{mean}(PI) \\ 0 & \text{otherwise} \end{cases} \quad (10)$$

In the rule-based approach, the synaptic permanence value is assigned based on the mean value of the inputs within the input space region with the potential connections. If the input is greater than the mean of the the inputs within this neighborhood, the synaptic permanence  $\mathbf{S}_{ij}$  is 1, otherwise  $\mathbf{S}_{ij} = 0$ .

In this work, we focus on the first three phases of the HTM SP: initialization, overlap and inhibition. The Algorithm 1 summaries the proposed approach. Lines 2-18 represent the HTM SP initialization stage, lines 20-22 refer to the overlap stage, and lines 24-27 correspond to the inhibition stage of the HTM SP.

## 4 Hardware implementation

### 4.1 Modified HTM SP

In this work, we investigate the modified HTM approach proposed in [12]. The difference between the original algorithm and the modified version of HTM is in the activation of the columns in the inhibition stage. The inhibition stage of the original algorithm is based on the WTA approach of  $k$  largest overlap values. In the modified version of the HTM SP, the selection of the winning columns occurs based on the mean value of the overlap in the inhibition region. If the overlap value of the column is greater than the mean value of the overlaps in the inhibition region, the columns is

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#### Algorithm 1 The HTM SP algorithm

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1:  $\triangleright$  HTM SP initialization
2: Define the size of input neighborhood with potential connections,  $x_i^c, \gamma, \rho, \eta, \theta_c$ , size of the local inhibition region,  $\theta_s$ 
3: Determine  $\phi$  by multiplying the average number of connected input spans of all the SP mini-columns by the number of mini-columns per inputs.
4:  $z_{ij} \sim U(0, 1)$ 
5: if  $\forall x_j \in (x_i^c, \gamma)$  then
6:    $\iota(x_j; x_i^c, \gamma) = 1$ 
7: for  $\iota(x_j; x_i^c, \gamma)$  and  $(z_{ij} < \rho)$  do
8:    $PI(i) = j$ 
9: if  $j \in PI(i)$  and  $PI(i) > \text{mean}(PI)$  then
10:   $\mathbf{S}_{ij} = 1$ 
11: else
12:   $\mathbf{S}_{ij} = 0$ 
13:  $\mathbf{B}_{ij} = \mathbf{S}_{ij}$ 
14: for  $|y_i - y_j| < \phi, i \neq j$  do
15:   $\mathbf{N}_i = j$ 
16:  $\triangleright$  HTM SP overlap
17:  $o_i = \beta_i \mathbf{B}_{ij} \mathbf{Z}_j$ 
18: for  $j \in \mathbf{N}(i)$  do
19:   $\mathbf{NO}(i) = o_j$ 
20:  $\triangleright$  HTM SP inhibition
21: if  $(o_i \geq \text{prctile}(\mathbf{NO}(i), 1 - s))$  and  $(o_i \geq \theta_s)$  then
22:   $\alpha_i = 1$ 
23: else
24:   $\alpha_i = 0$ 

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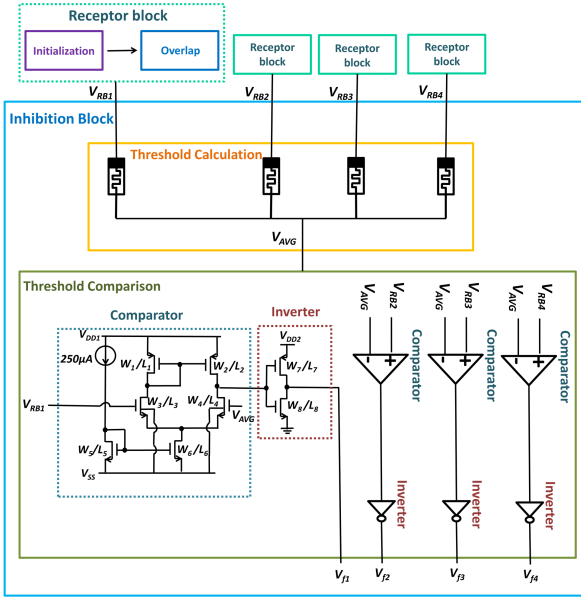
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activated, otherwise, it is inhibited. The modified approach for the inhibition region is represented in Eq. 11, which is used instead of the Eq. 6.

$$\alpha_i = 1, \text{ if } (o_i \geq \text{mean}(o_j) | j \in \mathbf{N}(i)) \quad (11)$$

As it is proven in [12] that the modified HTM approach results in higher accuracy and reduced on-chip area and power consumption, in this work, we focus on the modified HTM algorithm and check the effect of the rule-based initialization approach for the modified HTM hardware implementation. The overall architecture of the modified HTM illustrated in Fig.3. The receptor blocks correspond to the initialization and overlap calculation phases of the HTM SP and the inhibition block refers to the HTM SP inhibition phase.

The inhibition phase consists of the memristive threshold calculation block and threshold comparison block. In the threshold calculation block, the threshold value is determined as a mean of all input overlap values, which corresponds to the modified HTM SP approach. The value of the memristors in the threshold calculation block are the same. The threshold comparison block consists of the set of comparators and inverters. Each overlap voltage, corresponding to a particular connection in the inhibition block, is followed by a single comparator and inverter. The comparator is based on the



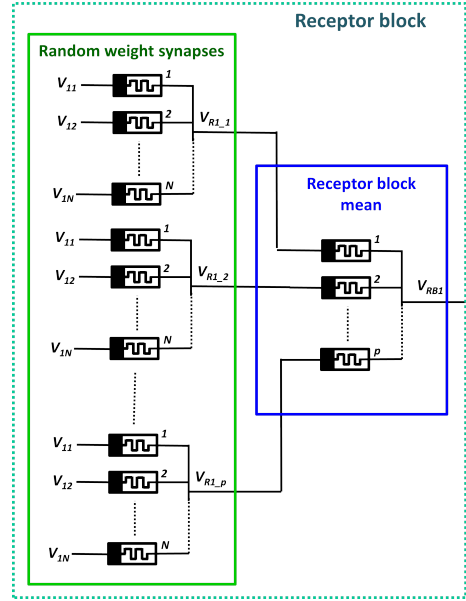
**Fig. 3** The HTM SP structure containing receptor block and inhibition block [12].

low voltage amplifier with 6 transistors and the current source. If the value of the overlap of a single column  $V_{RBj}$  is greater than the overall mean of all overlaps  $V_{AVG}$ , the output of the comparator is low, and vice versa. To invert the output of the comparator and normalize it to a certain level, the CMOS inverter is applied. The output of the inverter in the output of the inhibition block for the particular columns, which show whether the columns are activated or exhibited.

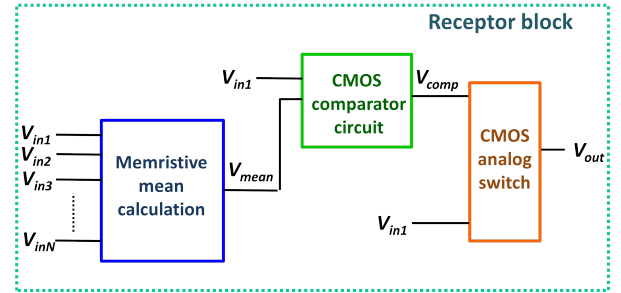
#### 4.2 Random weight approach implementation

The difference between the traditional random weight approach and rule-based approach occurs in the receptor block of the hardware implementation of the HTM SP. The implementation of the traditional approach is illustrated in Fig. 4.

The receptor block structure for the conventional HTM SP approach consists of the randomization of the weight synapses and the receptor block mean calculator. The randomization of the weights of the synapses refer to the initialization stage, where the weights are completely randomized. This is implemented with the memristive the set of the memristive mean circuits, where the resistances of the memristors are assigned randomly. Separate sets of the memristors in the block of random weight synapses refer to several random iterations to ensure that the weights are completely randomized. The receptor mean block performs the summation of all the columns for the overlap calculation.



**Fig. 4** The HTM SP receptor block structure for the random weight approach [12].



**Fig. 5** The HTM SP receptor block structure for the rule-based approach.

The parameter  $V_{RBj}$  corresponds to the final overlap of the particular column. The tradition summation of the overlap values in the HTM SP algorithm is replaced with the mean calculation on hardware, which does not have any impact on the performance of the modified HTM SP. The resistances of the memristors in the receptor block mean are the same.

#### 4.3 Rule-based approach implementation

In this work, we proposed the analog hardware implementation of the rule-based approach for the HTM SP. If the tradition hardware implementation of the HTM SP is based on the memristive circuits, the rule based approach is based on the CMOS circuits. The proposed receptor block is shown in Fig.5.

In the proposed architecture, the memristive mean calculation block and CMOS comparator circuit correspond to the initialization phase on the rule-based HTM

SP approach. The memristive mean calculation block calculates the average of the inputs in the mean of the inputs from the set of the potential inputs. The voltage  $V_{mean}$  refers to the threshold for assigning the potential inputs as connected or disconnected. The CMOS comparator circuit compares the input of the particular column with the mean of all columns from the potential inputs. If the input is greater than the threshold, the output of the comparator  $V_{comp}$  is low and vice versa. The CMOS analog switch block refers to the implementation of the overlap stage of the HTM SP. The voltage  $V_{out} = V_{in1}$ , if the comparator output  $V_{comp}$  is low, which corresponds to the case when the column is connected. The voltage  $V_{out} = 0$ , when  $V_{comp}$  is high, which means that the columns is disconnected. The voltage  $V_{out}$  refers to the overlap value of the column.

## 5 System level implementation

In this work, we apply the HTM SP with two different initialization stage approach for the face recognition problem. The overall system implementation of the face recognition module with the HTM SP is illustrated in Fig.6. The input RGB images are read by the image sensor and applied to the input data controller. In this stage, the sampling process occurs if it is required and the sampled images are preprocessed. In this method, we use only RGB to gray-scale conversion as a preprocessing step. In the existed HTM SP face and speech recognition systems [12], the standard deviation filter is applied in the preprocessing stage to improve the recognition process. However, in this work, we show the effect of the different approaches for the initialization stage; therefore, we remove the filtering stage to obtain the actual results from the HTM SP.

After the controller, the image is applied to the HTM SP stage, which performs the encoding of the image and outputs the sparse binary image with the preserved important image features. The output data controller controls, where the images are directed in the training and testing stages. In the training stage, the output from the HTM SP is preserved in the training template storage. The training continues until all image class templates are preserved. In the testing stage, the output data controller directs the images into the comparison circuit. The comparison circuit can be implemented as a memristive pattern matcher, which compares all templates from the training template storage with the current input image. Finally, the image class is determined.

The algorithmic implementation of the face recognition system approach is shown in Algorithm 2 in Appendix.

**Table 1** The average and maximum recognition accuracies for different databases for traditional random weight and proposed rule based approaches.

Dataset	Random weight approach		Rule based approach	
	mean accuracy	maximum accuracy	mean accuracy	maximum accuracy
AR	47.992 %	59.231 %	82.855%	83.231%
YALE	91.852 %	98.667 %	85.538 %	86.308 %
ORL	49.056 %	69.000 %	85.5389 %	86.308 %

## 6 Results

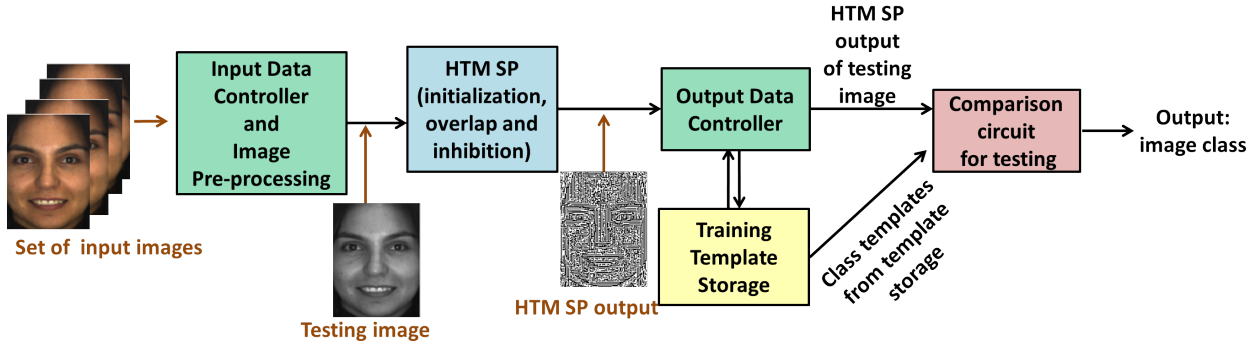
### 6.1 System level simulation

The experiments for the system level simulation were performed in MATLAB for 3 different databases: AR, ORL and YALE. The AR database contains 100 classes of faces with 26 face images per class with various natural variation and occlusions [13]. The ORL database includes 40 classes with 10 image per class with occlusions, scale variations and rotations [1]. The YALE database contains 15 classes with 11 images per class including different facial expressions and natural variabilities [14]. For the experiments in this work, 50% of the images with used for training and the other 50% for testing. The exemplar images for the random weight approach are shown in Fig.7, and for the rule-based approach in Fig.8.

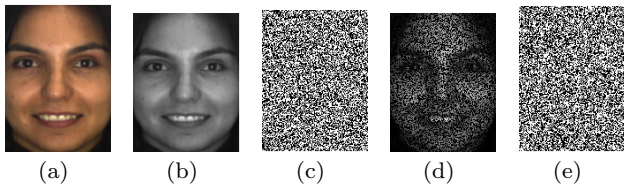
The recognition accuracy of the random weight and rule base approaches with the variation of the size of the inhibition region is shown in Fig.9. Fig.9(a) illustrates the simulation results for AR database, Fig.9(b) for ORL database and Fig.9(c) for YALE database. The rule-base approach improves face recognition accuracy for AR and ORL databases. However, for the YALE database, the recognition accuracy is decreased. This can be explained by the small number of classes and face samples in the YALE database. The average and maximum recognition accuracies for two approaches are compared in Table 1.

### 6.2 Analog hardware simulation

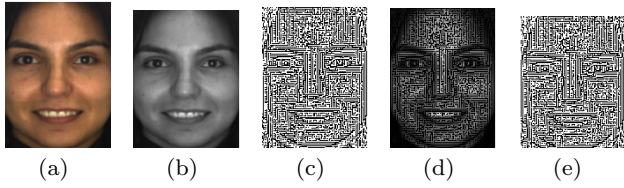
The simulation of the proposed rule-based approach was performed in SPICE for TSMC 180nm CMOS technology. Fig.10 illustrates the timing diagram for the proposed rule-based receptor block, shown in Fig.5. Fig.10(a) shows the inputs in the receptor block. Fig.10(b) illustrates the main input and the total mean of all the inputs. This main input is compared with the mean in the following stages. Fig.10(c) shows the comparator



**Fig. 6** The overall system implementation of the face recognition module with the HTM SP.



**Fig. 7** Simulation results for the random weight approach: (a) input image, (b) grayscale image, (c) binary weights, (d) HTM SP overlap output and (e) HTM SP inhibition output.



**Fig. 8** Simulation results for the rule-based approach with 2 inputs in the receptor region: (a) input image, (b) grayscale image, (c) binary weights, (d) HTM SP overlap output and (e) HTM SP inhibition output.

**Table 2** Comparison of the random weight and rule base approaches in terms of the on-chip area and maximum power consumption of a single receptor block.

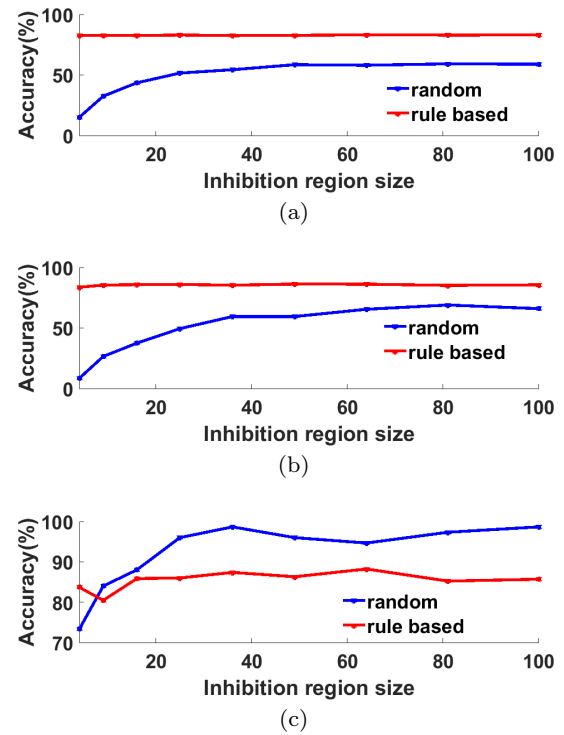
Approach	On-chip area	Power dissipation
Random weight approach	$0.125\mu m^2$	$42.92pW$
Rule-based approach	$13.31\mu m^2$	$135\mu W$

circuit output and Fig.10(d) illustrates the final output of a single receptor block.

Table 2 compares the on-chip area and power dissipation for random weight and rule-based approaches.

## 7 Discussion

As it was illustrated in Section 6, the proposed rule-based approach outperforms the traditional HTM random weight approach. This can be explained by the fact

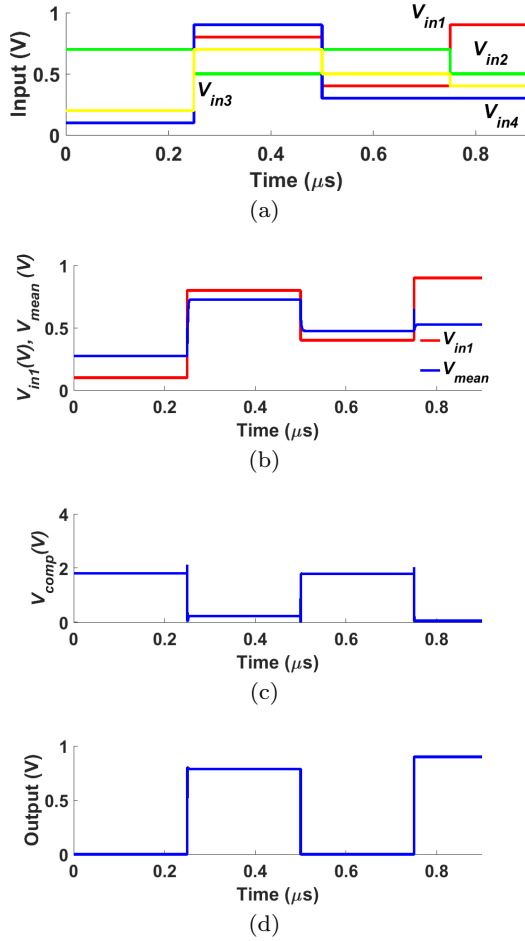


**Fig. 9** Simulation results for the face recognition for two methods for different databases: (a) AR, (b) ORL and (c) YALE.

that the rule-based approach that draws the correlation between the HTM SP weights to the input space. The main goal of the HTM SP is to create the SDR from the input. However, the facial images contain the natural sparseness. The rule based approach ensures the preservation of this natural sparseness of the images, which results in the increase of the recognition accuracy. In addition, this allows to preserve the structural information from the images, such as edges.

The hardware implementation of the rule-based approach required larger on-chip area and power consumption, comparing to the traditional random weight method.





**Fig. 10** Timing diagram for the proposed receptor block for the rule-based HTM approach: (a) inputs from the neighborhood, (b) main input and mean of the inputs, (c) comparator output and (d) receptor block output.

However, to achieve high recognition accuracy in the rule-based approach, the image filtering stage is not required, which is performed on the separate software. Moreover, the rule-based approach does not require the programming of the memristors to the random weights, which can be achieved combining either software-based or mixed-signal random number generation approach. The programming of the memristors requires additional time and reduces the processing speed. Also, the high accuracy of the rule-based approach result allows to remove the learning phase from the HTM SP, which can be implemented using digital or analog circuits and requires a significant amount of extra power and on-chip area [12].

## 8 Conclusion

In this paper, the hardware implementation of a rule-based approach for the initialization phase of the HTM

SP has been proposed. The proposed rule-based approach allows to achieve significant increase in recognition accuracy. The maximum accuracy is approximately 86%, which is equivalent to the processing of the HTM SP with the learning phase. The on-chip area and power requirements to implement the rule-based initialization phase of the HTM SP are  $13.31\mu m^2$  and  $135\mu W$  for a single receptor block, respectively.

## Appendix

In Algorithm 2, line 2 refers to the preprocessing stage, lines 3-17 refer to the HTM SP processing, lines 18-19 correspond to the training phase and lines 20-22 shows the testing (recognition) phase.

### Algorithm 2 System level implementation of HTM

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1: Define neighborhood  $N$ 
2:  $x = \text{grayscale}(x)$  ▷ PRE-PROCESSING
3: for  $p$  inhibition regions do ▷ HTM SP
4:   for  $k$  image blocks do
5:     for all  $i \in W$  do
6:       if  $x(i) \geq \text{mean}(x(i) \in N)$  then
7:          $W(i) = 1$ 
8:       else
9:          $W(i) = 0$ 
10:       $\text{image.block}(j) = W(j) \times \text{image.block}(j)$ 
11:       $\text{threshold.block} = \text{mean}(y.\text{image.blocks})$ 
12:      for  $y$  image blocks do
13:        if  $\text{image.block}(y) > \text{threshold.block}$  then
14:           $\text{inhibition.region}(y) = 1$ 
15:        else
16:           $\text{inhibition.region}(y) = 0$ 
17:       $x(p) = \text{inhibition.region}(p)$ 
18: if training phase then
19:   Store image to the training template
20: else if testing phase then
21:   Compare image to all stored templates
22:   Determine image class

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