NEUROMORPHIC MEMWEIGHT NETWORK

A.P. James*

School of Engineering, Nazarbayev University, Astana, Kazakhstan; *apj@ieee.org; alex.james@nu.edu.kz

INTRODUCTION.

The proposed processing unit called a memory cell [1] possesses remarkable properties such scalability, and small footprint on chip. We demonstrate the hardware architectures based on memory cells for character recognition, edge detection, medical image analysis, object detection, and object tracking applications.

METHODOLOGY AND RESULTS.

A hierarchical modular architecture [2] of the memory cells is utilized to recognize characters deformed by random noise, rotation, scaling and shifting. Edge detection [3] makes use of memory cells that act as kernels that process the image. Memory cell based architecture can be used in film mammograms [4] to detect lesions and in real-time cardiac x-rays for diagnostic purposes. The high speed and scalable architecture also gives the advantage of processing huge volume data making it useful for real-time high-speed object tracking applications. The memory cells can further be used for developing neuromorphic computing, and future computing architectures. Threshold logic circuits developed based on the proposed concepts [5] provide an alternative approach to CMOS VLSI chip design. This topic is one of the forefront challenges in the development of a learning enabled on-chip computing, and would require us to investigate not just new circuit design logic, but also new devices and systems.

CONCLUSIONS.

Small area and low power dissipation are the main advantages of the proposed methods using memory cell when compared to other conventional technologies. Advancements in device technologies such as memristors, resistive switching devices is essential in achieving these architectural goals.

ACKNOWLEDGMENTS.

The work reported in the poster were partly carried out under the seed grant project titled *Neuromorphic Biometric Security Memweight Networks Chip*.

REFERENCES.

- 1. James A.P., Dimitrijev S. (2010). Cognitive memory network, Electronics Letters, 46(10): 677-678.
- 2. James A.P. (2012). Machine intelligence using hierarchical memory networks, in: Handbook of Research on Computational Intelligence for Engineering, Science, and Business, p. 62.
- 3. Sherin S., James A.P. (2013). Directional edge detection using parallel cognitive cells, International Conference on Advances in Computing Communications and Informatics (ICACCI).
- 4. Sherin S., James A.P. (2013). Parallel realization of cognitive cells on film mammography, in: Proceedings of The 11th IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA-13), Melbourne, Australia, 16-18 July, 2013.
- 5. James A.P., Francis L.R.V.J, Kumar D.S. (2013). Resistive Threshold Logic. IEEE Trans. on VLSI.