Received: 1 December 2020 | Revised: 10 February 2021 | Accepted: 25 February 2021

DOI: 10.1049/tje2.12034

The Journal of Engineering

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH PAPER

Ultra-low power TIA with variable bandwidth in 0.13 μm CMOS for short-range optical interconnects

Nga T. H. Nguyen[1] | Ikechi A. Ukaegbu[2,4] | Jamshid Sangirov[3] | Mohammad Hashmi[4]

[1] LS Mtron, Anyang, Republic of Korea

[2] Integrated Device Solutions and Nanophotonics Laboratory, Electrical and Computer Engineering Department, School of Engineering and Digital Sciences, Nazarbayev University, Nur-Sultan, Kazakhstan

[3] Quantum5x Systems Inc., Ontario, Canada

[4] Electrical and Computer Engineering Department, School of Engineering and Digital Sciences, Nazarbayev University, Nur-Sultan, Kazakhstan

Correspondence
Ikechi A. Ukaegbu, Integrated Device Solutions and Nanophotonics Laboratory, Electrical and Computer Engineering Department, School of Engineering and Digital Sciences, Nazarbayev University, Kabanbay Batyr Ave. 53, Nur-Sultan 010000 Kazakhstan.
Email: ikechi.ukaegbu@nu.edu.kz

Funding information
Nazarbayev University (NU) Faculty-Development Competitive Research Grant, Grant/Award Number: 021220FD0451; NU Collaborative Research Grant, Grant/Award Number: 021220CRP0422; Ministry of Education and Science of the Republic of Kazakhstan, Grant/Award Number: AP08856931

Abstract

An ultra-low power and variable bandwidth transimpedance amplifier (TIA) for short-range optical interconnects is presented here. The TIA is implemented in a 0.13μm complementary metal oxide semiconductor (CMOS) technology. To reduce the power consumption, the TIA is designed using a regulated cascade topology with capacitor degeneration for frequency enhancement and also operates in the weak inversion mode. With a supply voltage of the range 0.7–0.92 V, a reduced power consumption of 2.9–4.6 mW and a variable bandwidth of the range 3–4.9 GHz are achieved. Clear eye diagrams are obtained at 2.5–6.135 Gbps and a BER of less than 10^{-12} with input power of −4.3 to −3 dBm at 2.5–6.135 Gbps, respectively. Also, the TIA achieved a transimpedance gain of 51.2–52.4 dBΩ. The small-sized chip occupied an area of 0.28 × 0.42 mm^2 with pads and 0.1 × 0.1 mm^2 without pads.

1 | INTRODUCTION

Optical interconnection technology is one of the potential and preferred technologies for meeting with the current trend of increasing the density of interconnection and reducing power consumption for the next-generation and high-performance computing systems, when compared to electrical interconnects. Optical interconnects exhibit several advantages over their electrical counterparts such as lower inter-channel crosstalk, higher bandwidth, and lower power consumption [1–4]. With power playing a significant role in determining system cost, the use of dynamic power management techniques is becoming increasingly common [5, 6]. There have been a number of reports that detail techniques to improve the I/O power efficiency in analog circuits and mixed signal circuits [7–12], and also in electrical interconnects [4, 5]. For example, device-level scaling is one of the low-voltage circuit techniques. However, one of the issues with this method is increased threshold variation. Threshold variation depends on both device and process parameters such as channel length and width, oxide thickness, junction depth, and substrate doping concentration. Other low-voltage circuit techniques include bulk-driven, floating gate techniques, flipped voltage follower technique, and bulk-driven flipped voltage follower technique. A scalable transceiver was reported with the power efficiency of 2.8–6.5 mW/Gbps by using scalable transceiver circuit blocks and joint optimization of supply voltage, bias currents, and driver power with data rate [13]. Similarly, it has been demonstrated that low swing voltage mode drivers significantly reduce driver power [14, 15].

Over a period of time, it has been proven that the use of optical interconnects have a number of benefits over their electrical counterparts [16]. While this is true, there have been reports of numerous research articles that deal with the minimization of power consumption in optical interconnects. Essentially, to reduce optical link power consumption, each component of the link should optimize the power efficiency. The transimpedance amplifier (TIA) is one of the important circuits of optical interconnects and extensive research has been pursued towards reducing the power consumption of the TIA in the past decade [17–19]. An optical receiver is made up of

TIA, limiting amplifier/gain stages and output buffer. Thus, the TIA is a very important part of an optical receiver. A 2.2 mW TIA was designed in 80 nm complementary metal oxide semiconductor (CMOS) technology with a trade-off of higher input-referred noise to achieve high speed and low power consumption [17]. Another work on an ultra-low power receiver achieved low power consumption by employing complicated design of RC double sampling front end and a dynamic offset modulation technique in a 65 nm CMOS technology [18]. However, these two designs although very interesting, are based on scaled technologies which are expensive and have complex circuit topology. To address this aspect, the regulated cascade (RGC) topology with capacitive degeneration and resistive feedback were employed to achieve low power and high bandwidth [19]. Although this design employs the RGC topology and capacitive degeneration, the resistive feedback and the extra buffer stage not only adds to the complexity but also affects its power consumption and total size. Overall, these circuits do not support operation for a wide range of supply voltage and the bandwidth may severely degrade at lower voltages and hence can be inoperable even at lower bit rate.

To address the above concern, a scalable supply voltage and frequency TIA with an active-load inductor to boost the bandwidth was introduced [20]. However, the active-load inductor in such a design might lead to flatness of the frequency response and hence can make the performance of the TIA at high frequency degraded. In addition, the noise and input sensitivity of the TIA, which are very important parameters in determining its performance, were also not reported in the paper. Furthermore, the use of variable resistors for different voltage levels complicates this architecture. Subsequently, a current controlling PMOS array and a tuneable resistive bank is implemented to optimize the power consumption and bandwidth but at the cost of increased complexity in the architecture [21]. There have been reports of transistors working in weak inversion region for ultra-low power consumption [7, 22]. In this region, there are some advantages including high voltage gain, less distortion, and ease of compensation with degradation in the noise margin.

Here, a simple TIA using RGC input and capacitive degeneration in the gain stage with the transistors working in weak or moderate inversion mode has been explored for ultra-low power consumption in 130 nm CMOS technology. The TIA operates in the weak or moderate inversion mode and as a result, the bandwidth of the TIA is reduced due to the lowering of the cut-off frequency of the transistor in such modes. However, in these modes, the voltage gain of the transistor increases, and the bandwidth improves due to the capacitive degeneration. Also, due to operation in the weak or moderate inversion mode, low power consumption is achieved. A comparison table and discussion demonstrates the effectiveness of the proposed topology. Though the circuit allows for variable bandwidth operation, if designed in lower technology node, has the potential to provide a number of benefits associated with lower technology nodes. Section 2 provides extensive description of the proposed circuit and the corresponding analysis. Section 3 is dedicated to measurements and discussion while the Section 4 concludes this paper.

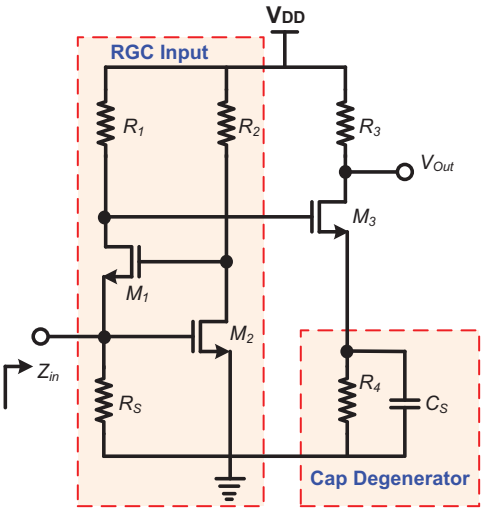

FIGURE 1 Schematic of the proposed TIA

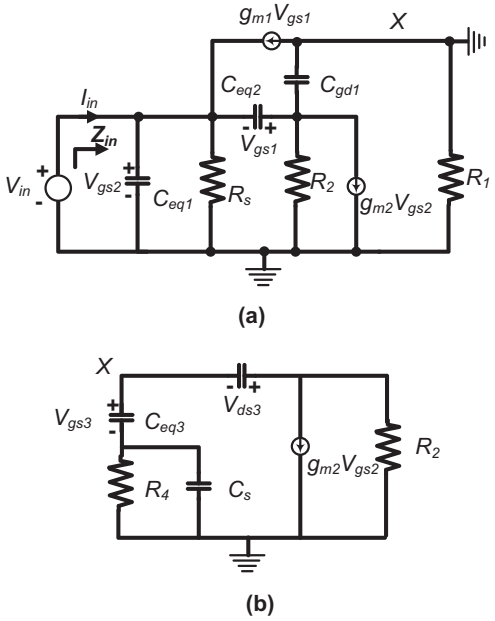

FIGURE 2 Small-signal circuit model of (a) the RGC and (b) the output stage of the proposed TIA

2 | CIRCUIT DESIGN AND ANALYSIS

The schematic of the proposed TIA employing RGC topology is shown in Figure 1. The RGC topology reduces the input impedance by the amount of its own voltage gain. The RGC topology reduces the capacitive effect of the photodiode (PD) and also prevents the input pole from dominating the bandwidth of the entire TIA.

Figure 2 shows the small-signal circuit model of the proposed TIA. The input impedance of the RGC input is given as:

$$Z_{in} = \frac{1}{gm_1\,(1 + gm_2 gm_2)}, \tag{1}$$

where $1 + gm_2R_2$ is the gain of the local feedback. Thus, the amount of reduction of the input parasitic effect is determined by the size of the local feedback.

A transistor biased in the weak inversion region maintaining approximate relation between the drain current, gate-to-source voltage V_{gs} and drain-to-source voltage V_{ds} is given by expression (2) [22]. Here, n and I_{D0} can be extracted from experimental data, k is Boltzmann's constant, T is the absolute temperature, and n is the channel-noise factor of MOSFET.

$$I_D = \left(\frac{W}{L} I_{D0} e^{qV_{gs}/nkT}\right)\left(1 - e^{-V_{ds}/V_t}\right). \tag{2}$$

The value of n ranges from approximately 1.6 in weak inversion to 1.3 in strong inversion for an nMOS device [23]. The transconductance can be deduced by differentiating Equation (2) with respect to V_{gs} as expressed in Equation (3). It is apparent that the drain current directly affects the transconductance in the weak inversion region.

$$g_m = \frac{dI_D}{dV_{gs}} = I_{D0}\frac{W}{L}\frac{q}{nkT} e^{qV_{gs}/nkT} = \frac{q}{nkT} I_D. \tag{3}$$

Subsequently, the transimpedance of the TIA can be expressed by Equation (4). In this expression, gm_1, gm_2, and gm_3 are the transconductances of M_1, M_2, and M_3, respectively.

$$Z_T(s) = R_{1eq}\frac{1 + \frac{sC_{eq2}}{g_{m2}}}{\left[1 + \frac{sC_{eq1}}{(1+g_{m2}R_{2eq})g_{m1}}\right]\left[1 + sR_{2eq}\left(C_{eq3} + C_{eq2}\right)\right]} \times \frac{g_{m3}R_{3eq}}{1 + g_{m3}R_{4eq}} \times \frac{1 + sR_{4eq}C_s}{1 + s\frac{R_{4eq}C_s}{1+g_{m3}R_{4eq}}}. \tag{4}$$

Furthermore, $C_{eq1} = C_{pd} + C_{gs1} + C_{sb1}$; $C_{eq2} = C_{gs1} + C_{gd2}$; $C_{eq3} = C_{ds2} + C_{gs3}$; $R_{1eq} = R_1 || r_{ds1}$; $R_{2eq} = R_2 || r_{ds2}$; $R_{3eq} = R_3 || r_{ds3}$; $R_{4eq} = R_4 || (r_{ds3}+R_3)$.

In the above, $r_{ds1,2,3}$ is the drain–source resistance which is the small-signal output impedance $r_o \approx (1/\lambda I_d)$, which is inversely proportional to λ, the channel length modulation factor. It can be inferred from Equation (4) that the TIA has two zeros and three poles; in particular, it has a zero at $-(1/R_4C_s)$ and a pole at $-(1 + gm_3R_4)/R_4C_s$ from the degeneration stage. With the appropriate value of R_4, C_s and g_{m3}, the zero from the gain stage can be used for compensating the dominant pole of the TIA and the 3-dB frequency is determined by the second-lowest pole of the circuit $1/(R_2(C_{eq3} + C_{eq2}))$. However, the capacitor degeneration works as a filter for the gain stage to enhance noise performance of the TIA. Further, the degeneration capacitor value should be carefully chosen so as to improve bandwidth performance. An optimal value of 450 fF was used as C_s.

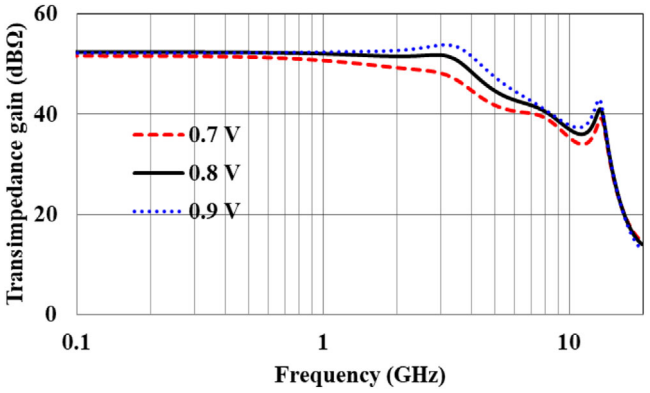

FIGURE 3 Transimpedance gain of the proposed TIA with different supply voltages

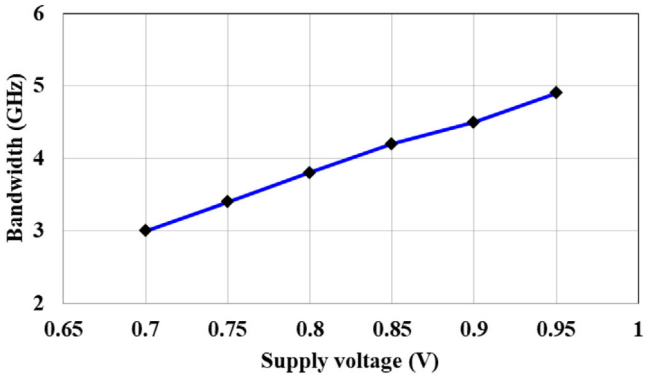

FIGURE 4 Bandwidth versus supply voltage

Now the low frequency gain of the TIA can be expressed by Equation (5).

$$Z_T(0) = R_{1eq} \times \frac{g_{m3}R_{3eq}}{1 + g_{m3}R_{4eq}} = (R_1 \parallel r_{ds1}) \times \frac{g_{m3}\frac{R_3 r_{ds3}}{R_3 + r_{ds3}}}{1 + g_{m3}\frac{R_4 r_{ds3}}{R_4 + r_{ds3}}}$$

$$= (R_1 \parallel r_{ds1}) \times \frac{R_3(R_4 + r_{ds3})g_{m3}r_{ds3}}{(R_3 + r_{ds3})(R_4 + r_{ds3} + R_4 g_{m3} r_{ds3})}, \tag{5}$$

$$Z_T(0) = (R_1 \parallel r_{ds1}) \times \frac{R_3(R_4 + r_{ds3})K_3}{(R_3 + r_{ds3})(R_4 + r_{ds3} + R_4 K_3)}. \tag{6}$$

The term K_3 in Equation (6) is expressed in Equation (7).

$$K_3 = g_{m3}r_{ds3} = \frac{q}{nkT} I_D \frac{1}{\lambda I_D} = \frac{q}{nkT\lambda}. \tag{7}$$

In Equation (6), because $r_{ds3} >> R_3$ and $r_{ds3} >> R_4$, when the I_D changes in the weak region, a small change in r_{ds3} does not have much effect on the low frequency gain of the TIA. This is also clear from the small/negligible change of transimpedance gain at low frequency in the frequency response plot in Figure 3.

Figures 4 and 5 show the relationship between bandwidth with supply voltage and transimpedance gain with supply voltage of the proposed TIA under moderated and weak inver-

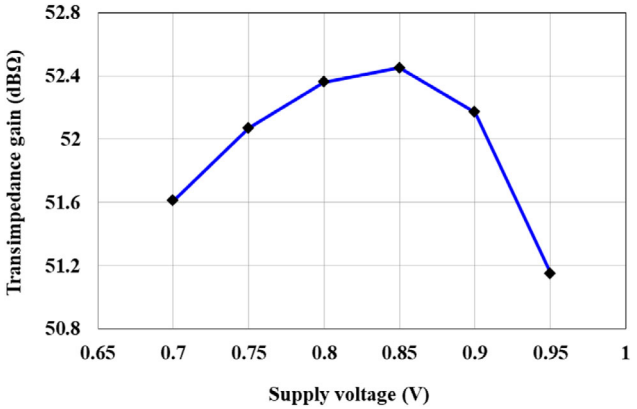

FIGURE 5 Transimpedance gain versus supply voltage

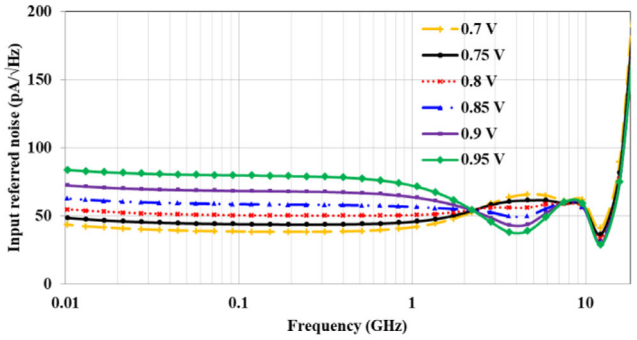

FIGURE 6 Simulation results of input-referred noise with different supply voltages

sion modes. In the range 0.7–0.95 V of supply voltage, the bandwidth linearly increases with the supply voltage while the gain does not change significantly.

The sensitivity is another important parameter for a TIA and it is dependent on the input-referred noise of the TIA. The input-referred noise of the proposed TIA is given by Equation (8). Here, k is the Boltzmann's constant, T is the absolute temperature, and Γ is the channel-noise factor of MOSFET.

$$I_{n,eq} \cong 4kT\left(\frac{1}{R_1}+\frac{1}{R_s}\right)+\frac{4kT\omega^2\left(C_{eq2}\right)^2}{g_{m1}^2}\left(\Gamma+\frac{1}{R_1}\right) + 4kT\frac{\left(\Gamma+\frac{1}{R_2}\right)R_2}{1+g_{m2}R_2}\times\left[\frac{1}{R_s^2}+\omega^2\left(C_{eq1}+C_{gs2}+C_{sb1}\right)^2\right] \times 4kT\omega^2\left(\frac{\Gamma+\frac{1}{R_6}\parallel C_s+\frac{1}{R_2}}{g_{m3}^2}\right)\left(C_{db1}+C_{eq3}+C_{gd1}\right). \quad (8)$$

It can be observed in Equation (8) that the low frequency noise is dominated by thermal noises whereas the high frequency noise worsens as the input parasitic capacitances increase. The simulation results of the input-referred noise of the TIA with different supply voltages is given in Figure 6. Apparently, as the supply voltage increase, the noise of the

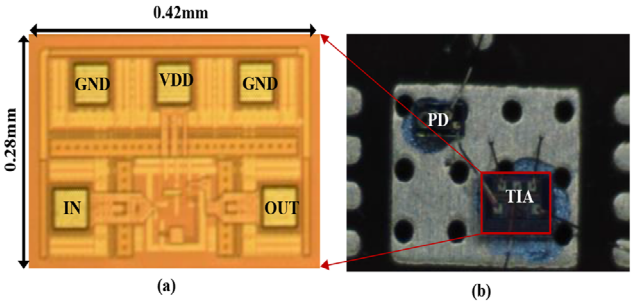

FIGURE 7 Photographs of (a) TIA chip and (b) its optical packaging

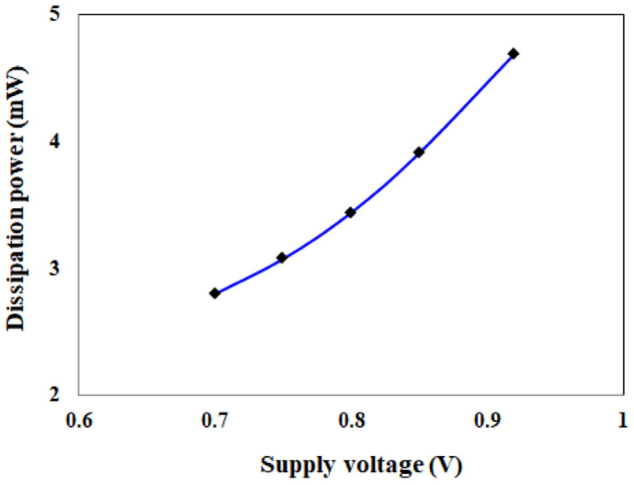

FIGURE 8 Total dissipation power versus supply voltage of the TIA

TIA degrades at low frequency but improves at 3-dB frequency. However, the 3-dB frequency can be further increased at higher supply voltages in the absence of high noise. In brief, high noise constitutes one of the trade-offs of operation in weak inversion mode.

3 | MEASUREMENT AND DISCUSSION

The TIA was designed and fabricated in a 0.13 μm CMOS technology with six metal layers. The Figure 7 depicts the photographs of TIA chip and its packaging. Including the ESD pads, the TIA chip occupies a total area of 0.42 mm × 0.28 mm. The TIA was die bonded to an evaluation printed circuit board and wire bonded to a commercial 850 nm photodiode. The capacitance of the photodiode is 0.24 pF. A commercial optical transceiver was used to measure the optical characteristics of the TIA.

Figure 8 provides the relationship between the supply voltage and the total power dissipation. The power consumption scales from 2.8 to 4.69 mW when the supply voltage scales from 0.7 to 0.92 V. The results show that the total power consumption is propotional to the square of the supply voltage. This relationship confirms the power consumption saving possibility by voltage scaling/variation.

A 2^{31} – 1 pseudorandom binary sequence input signal generated from Anritsu MP1763B pulse-pattern generator and an

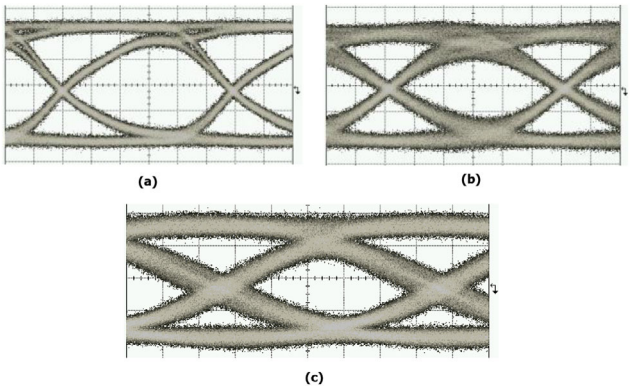

FIGURE 9 Eye diagrams of the TIA at (a) 2.5 Gbps, 4.2 mV/div, 67.2 ps/div; (b) 5 Gbps, 5.2 mV/div, 33.4 ps/div; (c) 6.135 Gbps, 5.5 mV/div, 27.5 ps/div at the input power of −4.3 dBm

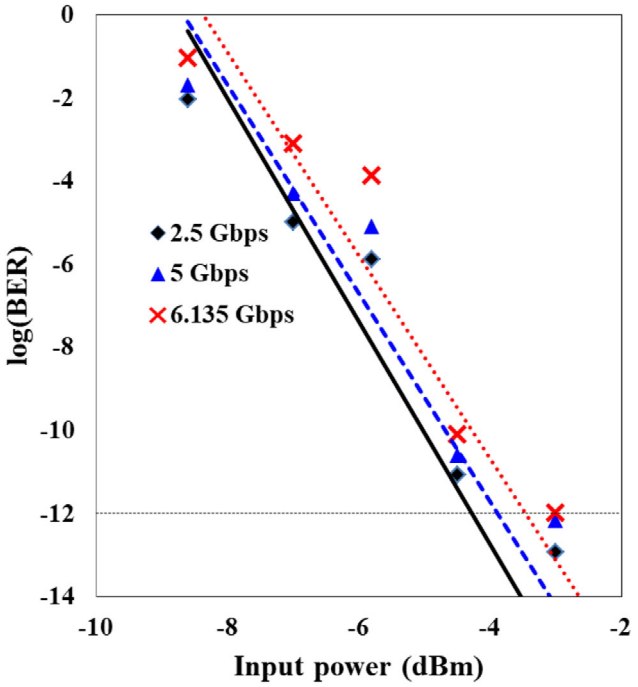

FIGURE 10 BER perfomance of the TIA at 2.5, 5, and 6.135 Gbps

Aglient 86100 oscilloscope were used to measure the dynamic response. Figure 9 shows the observed eye diagrams of the TIA at 2.8, 5, and 6.135 Gbps at −4.3 dBm input power with the supply voltage of 0.7, 0.85, and 0.92 V, respectively. Figure 10 shows measured BER performance of the TIA at 2.5, 5, and 6.135 Gbps. The minimum input power required to get a BER of 10^{-12} is −3 dBm at data rate of 6.135 Gbps. At 2.5 Gbps, in order to get BER of 10^{-12}, an input power of −4.3 dBm is required. Table 1 shows the comparison of the proposed TIA with other works. Due to the operation in the weak or moderate inversion mode, the proposed TIA outperforms other TIA in terms of power consumption while maintaining high gain. At input supply voltage of 0.7–0.92, a low power consumption of 2.9–4.6 was achieved which is lower when compared to designs of similar technologies (as in [20, 28]) and of lower technologies (as in [13, 21, 25]). Also the transimpedance gain is high when

TABLE 1 Comparison of the proposed TIA with other works

Reference	[13]*	[20]	[21]*	[24]	[25]*	[26]	[27]	[28]	[29]*	This work
Technology (CMOS)	0.065 µm	0.13 µm	0.065 µm	0.065 µm	0.040 µm	0.090 µm	0.18 µm	0.13 µm	0.18 µm	**0.13 µm**
Supply voltage (V)	0.68–1.05	1.2–0.6	0.48-0.98	1.2	1.3	1.2	1.8	1.5	1.5	**0.7–0.92**
Bandwidth (GHz)/bitrate (Gb/s)	—/5–15	7.3–2.3/8–4	0.86–13.1/1.25–20	21.6/40	14.5/3–25	3.5/5	8/—	7/—	1.96/-	**3–5/2.8–6.135**
Input-referred noise ($pA/\sqrt{Hz}$)	—	—	8.46–18	<30	22.4	15.26	40	31.3	11.7	**37.9–55.9**
PD capacitance (pF)	—	0.3	1	0.2	0.1	0.16	0.25	0.25	0.5	**0.24**
3-dB Transimpedance gain (dBΩ)	—	57.7–59.6	43–61	46.7	64	53.9	46	50.1	42.24	**51.2–52.4**
Power consumption (mW)	6–41	36–5	0.32–13.2	8.2 (TIA core only)	8 (TIA only)	1.52	31.5	7.5	0.972 (TIA core only)	**2.9–4.6**
Variable bandwidth/Weak inversion mode	Yes/No	Yes/No	Yes/No	No/No	Yes/No	No/No	No/No	No/No	No/No	**Yes/Yes**

*TIA + LA.
Others only TIA.

compared to designs of similar and lower technology. Based on the comparison of the proposed TIA with other works in Table 1, it can be seen that if designed in lower technology node, the proposed TIA has the potential to provide improved performance and a number of benefits associated with lower technology nodes.

4 | CONCLUSION

An ultra-low power TIA with variable bandwidth has been proposed and implemented in this study. In order to reduce the power consumption, the TIA was implemented using RGC topology with capacitor degeneration for frequency enhancement in the weak inversion mode. With a supply voltage of the range 0.7–0.92 V, a reduced power consumption of 2.9–4.6 mW, and a variable bandwidth of the range 3–4.9 GHz were achieved. When packaged with a 850 nm photodiode, the measured results showed clear eye diagrams at 2.5–6.135 Gbps. A BER of less than 10^{-12} with the input power of −4.3 dBm to −3 dBm at 2.5–6.135 Gbps, respectively, was achieved with a transimpedance gain of 51.2–52.4 dBΩ. The chip occupied a very small area of 0.28×0.42 mm^2 with pads and 0.1×0.1 mm^2 without pad. The designed TIA can be applied as a front-end circuit to convert the input photocurrent to output voltage that is high enough to feed to the next stages of an optical receiver such as the limiting amplifier stages (gain stages) and the output buffer, and is applicable for chip-to-chip optical interconnects.

ACKNOWLEDGMENT

The authors wishes to thank Nazarbayev University (NU) Faculty-Development Competitive Research Grant (021220FD0451); NU Collaborative Research Grant (021220CRP0422); and Ministry of Education and Science of the Republic of Kazakhstan (AP08856931) for financial support.

ORCID

Ikechi A. Ukaegbu https://orcid.org/0000-0002-9370-8969

REFERENCES

1. Levi, F.J.: Optical interconnections in systems. Proc. IEEE. 88(6), 750–757 (2000)
2. Lytel, R., et al.: Optical interconnections within modern high-performance computing systems. Proc. IEEE. 88(6), 758–763 (2000)
3. Benner, F., et al.: Exploitation of optical interconnects in future server architectures. IBM J. Res. Develop. 49(4–5), 755–775 (2005)
4. Taubenblatt, M.A.: Optical interconnects for high-performance computing. J. Lightwave Technol. 30(4), 448–457 (2012)
5. De Micheli, G., Benini, L., Bogliolo, A.: Dynamic power management of electronic systems. NATO Science Series (NSSE), 263–292 (1999)
6. Benini, L., De Micheli, G.: Dynamic Power Management of electronic circuits and systems. Design Techniques and CAD Tools. Kluwer, Philadelphia (1997)
7. Toumazou, C., Lidgey, F. J., Haigh, D. G. (eds.): Analogue IC Design: The Current-Mode Approach. Peter Peregrinus: London (1990)
8. Sánchez-Sinencio E., Andreou, A. G.: (ed.): Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits.. IEEE Press, New York (1999)
9. Yan, S., Sánchez-Sinencio, E.: Low voltage analog circuit design techniques: A tutorial. IEICE Trans. Analog Integr. Circuits Syst. 2(E83), 1–17 (2000)
10. Rajput, S.S., Jamuar, S.S.: Low voltage analog circuit design techniques. IEEE Circuits Syst. Mag. 2(1), 24–42 (2002)
11. Carvajal, R.G., et al.: The flipped voltage follower: A useful cell for low voltage low-power circuit design. IEEE Trans. Circuits Syst. I Regul. Pap. 52(7), 1276–1291 (2005)
12. Singh, P., Niranjan, V., Kumar, A.: Low power transimpedance amplifier (TIA) using bulk driven FVF. In: IEEE International Conference on Information Systems and Computer Networks, pp. 179—182 (2019)
13. Balamurugan, G., et al.: A scalable 5–15 Gbps, 14–75 mW low-power I/O transceiver in 65 nm CMOS. IEEE J. Solid-State Circuits 43(4), 1010–1019 (2008)
14. Poulton, J., et al.: A 14 mW 6.25 Gb/s transceiver in 90 nm CMOS for serial chip-to-chip communications. IEEE J. Solid-State Circuits. 42(12), 2745–2757 (2007)
15. Wong, K.-L.J., et al.: A 27 mW 3.6 Gb/s I/O transceiver. IEEE J. Solid-State Circuit. 34(11), 1591–1599 (2004)
16. Forbes, M.: Optically interconnected electronic chips: A tutorial and review of the technology. Electron. Commun. Eng. J. 13(5), 221–232 (2001)
17. Kromer, C., et al.: A low-power 20-GHz 52-dB Transimpedance amplifier in 80-nm CMOS. IEEE J. Solid-State Circuits. 39(6), 885–894 (2004)
18. Nazari, M.H., Neyestanak, E.A.: A 24-Gb/s double-sampling receiver for ultra-low-power optical communication. IEEE J. Solid-State Circuits. 48(2), 344–357 (2013)
19. Nguyen, N.T.H., et al.: 0.013 mm^2 and low-power 10 Gb/s transimpedance amplifier for short-reach optical interconnects. Microwave Opt. Technol. Lett. 55(10), 2484–2487 (2013)
20. Chen, X., Wei, G.Y., Peh, L.S.: Design of low-power short distance optoelectronic transceiver front-ends with scalable supply voltage and frequencies. In: International Symposium on Low Power Electronics and Design (ISLPED), pp. 277–282 (2008)
21. Dash, P.P., Cowan, G., Liboiron-Ladouceur, O.: A variable bandwidth, power-scalable optical receiver front-end in 65 nm. In: IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 717–720 (2013)
22. Vittoz, E., Fellrath, J.: CMOS analog integrated circuits based on weak inversion operation. IEEE J. Solid-State Circuits. 12(3), 224–231 (1977)
23. Enz, C.C., Krummenacher, F., Vittoz, E.A.: An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. J. Analog Circuits Signal Process. 8(1), 83–114 (1995)
24. Bashiri, S., et al.: A 40 Gb/s transimpedance amplifier in 65 nm CMOS. In: Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS) Symposium Digest., pp. 757–760.(2010)
25. Chien, Y.-H., Fu, K.-L., Liu, S.-L.: A 3–25 Gb/s four-channel receiver with noise-cancelling TIA and power-scalable LA. IEEE Trans. Circuits Syst. II: Express Briefs 61(11), 845–849 (2014)
26. Zohoori, S., Dolatshahi, M.: A low-power CMOS optical communication front-end using a three-stage TIA for 5 Gb/s applications. Majlesi J. Electr. Eng. 11(4), 11–19 (2017)
27. Chen, D., et al.: Cross-coupled current conveyor based CMOS transimpedance amplifier for broadband data transmission. IEEE Trans. Very Large Scale Integr. VLSI Syst. 21(8), 1516–1525 (2013)
28. Taghavi, M.H., et al.: 10-Gb/s 0.13-μm CMOS inductor less modified-RGC transimpedance amplifier. IEEE Trans. Circuits and Syst. I 62(8), 1971–1980 (2015)
29. Zohoori, S.: An inverter-based, CMOS, low-power optical receiver front-end. Fiber Integr. Opt. 38(1), 1–20 (2019)

How to cite this article: Nguyen N.T.H., et al.: Ultra-low power TIA with variable bandwidth in 0.13μm CMOS for short-range optical interconnects. J. Eng. 2021:, 295–300. (2021) https://doi.org/10.1049/tje2.12034