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# Data Acquisition System for Microwave Kinetic Inductance Detectors

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**Abstract.** Energetic Cosmos Laboratory is developing Kinetic Inductance Detectors (MKID) for mm/submm astronomy purposes. In order to measure the instantaneous resonance frequency and dissipation of superconducting microresonators of the MKID arrays, we have developed a data acquisition system with emphasis on precision, readout speed and digital processing capabilities. We use IQ mixer to down convert the MKIDs signal in the range of 20-80 MHz, then digitize them by 250 MSPS ADC. Processed data at FPGA-Kintex 7 will be transferred to the PC for further analysis by the rate of 10 Gbit/sec. In this report, we describe the technical details and the algorithm we developed.

## 1. Introduction

The Energetic Cosmos Laboratory investigates the birth and evolution of the universe using state-of the art instrumentation. One of the instrumentations that we are working on is sub mm cryo-detectors known as Kinetic Inductance Detectors (MKIDs). MKIDs are superconducting detectors capable of counting single photons and measuring their energy in the vast range from microwave to X-ray [1]. They feature intrinsic frequency domain multiplexing (FDM) at microwave frequencies, allowing the construction and readout of large arrays with only one cryo-amplifier [2].

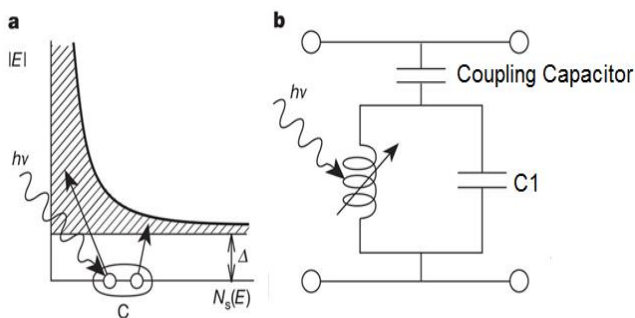
In order to measure the instantaneous resonance frequency and dissipation of superconducting microresonators of the MKID array, we perform frequency domain multiplexed real-time complex microwave transmission measurements. A frequency comb waveform is generated that has a number of tones that is between 1.3 to 1.4 GHz, to excite MKID resonant frequencies. The direct frequency



synthesis and the data acquisition heavily relies on a large FPGA using parallelized and pipelined processing. FPGA adapted FFT algorithm (channelizer) is used in order to maintain an acceptable readout rate.

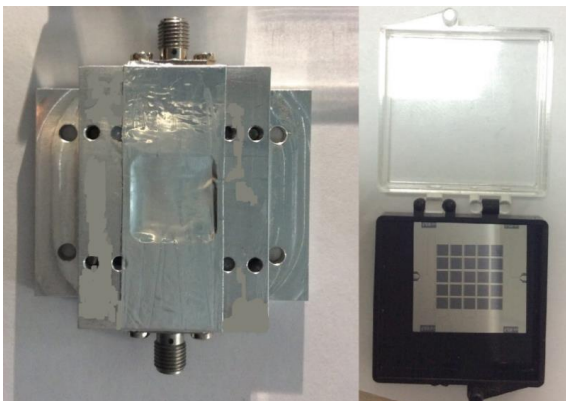
## 2. Detector description

One of the most important advantages of MKIDs is that they allow superconducting microresonators to be multiplexed in the frequency domain at microwave frequency [2]. Photons that hit the MKID change the surface impedance of a superconductor through the kinetic inductance effect. The kinetic inductance occurs due to energy stored in the supercurrent of a superconductor [3]. The equivalent circuit diagram (figure 1) for an MKID is a simple LC resonator with a variable inductance. When a photon hits the detector, the inductance changes. Consequently, the resonant frequency of the resonator changes, and the phase response changes as well. The phase of a probe tone passing through the MKID with frequency equal to the resonant frequency will shift, which is a function of the energy of the incident photon [4].



**Figure 1.** MKID equivalent circuit

We create a comb of tones to pass through the feedline, with each tone corresponding to the resonant frequency of each resonator. Each MKID imprints an indication of incident photons only on its tone in the comb. This way, thousands of MKIDs can be read out by a single wire [5]. As the frequency comb passes through the MKIDs all of these tones are distinguished from one another, so each can be analyzed in parallel for changes in phase. MKIDs that we are using for our data acquisition design is 25 pixels and resonates between 1.3 and 1.4 GHz with a loaded quality factor in the order of 50K (measured). These are mm-wave detectors, optimized at 150 GHz optical frequency (figure 2).



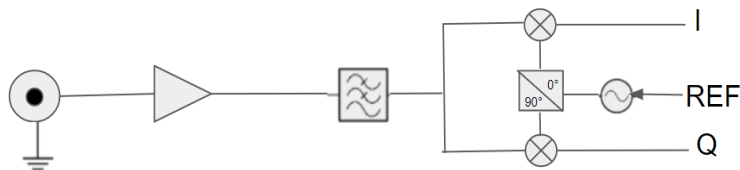
**Figure 2.** ECL 25 Pixel MKID Array

### 3. Data Acquisition System

In order to read out the MKID, we generate a tone at the resonant frequency of the MKID and send it to the MKID, and capture the phase change of the received signal that show that the MKID was hit by a photon. We used two ways to perform the readout: analog front end and fully-digital readout.

#### 3.1. Analog front end

In the analog part of the data acquisition system, we used Ettus UBX-160. Figure 3 shows schematic of this circuit. RX is the receiving port where we receive the signal from an MKID, and amplify it with LNA, and down convert to a lower frequency using IQ mixer. We use the TX port for feeding the signal to the MKID to sweep the frequencies. After DAC, there is an IQ up converter and digital attenuator which is fed back to MKID in the cryostat.

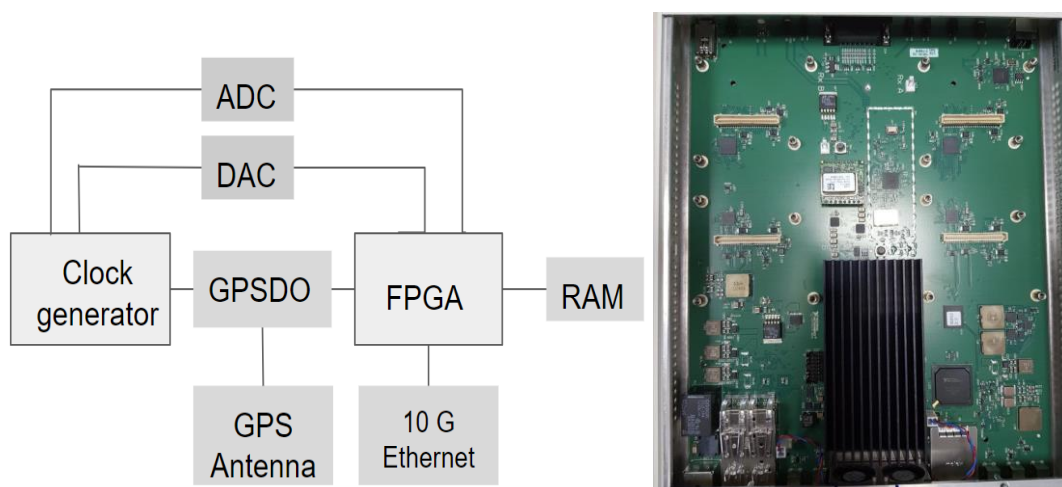


**Figure 3.** Analog Readout Schematics

#### 3.2. Digital Readout

In order to assemble the digital readout setup we implemented the Ettus USRP board (figure 5). Ettus architecture combines two extended-bandwidth daughterboard slots covering DC – 6 GHz with up to 160 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA which provides a well-supported back-end for the signal processing functionalities.

Both the 16 bit DAC and 12 bit ADC have been proved to meet datasheet specifications such as SNR, SFDR, IMD and so on. DAC is able to work up to 1.23Gbps; ADC is able to work up to 210 Mps. A clock generator receives input frequency from the 96 MHz oscillator and distributes it to the FPGA. We have a 1 GB RAM next to the FPGA to provide extra memory capacity for processes such as FIFO etc. In order to synchronize the system, we use a GPS antenna that imports 1pps signal.

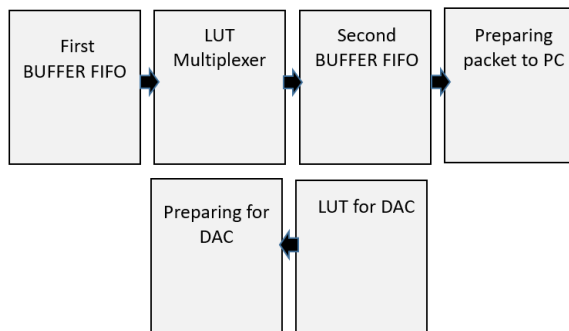


**Figure 4.** MKID Readout Setup

#### 4. FPGA Firmware Development

The FPGA Firmware performs various tasks including data readout, ADC and clock distributor configuring, digital signal processing, and communicating with PC through the Ethernet and USB interfaces. We used the Xilinx Kintex-7 FPGA to program all the blocks of our design. To have the no data loss, we implemented a digital FIFO (First Input, First Output) for each ADC in the Xilinx Kintex-7 FPGA (figure 5) to save the stream of data temporarily in real time. Simultaneously, the data is saved in a DDR3 RAM for computational processes. The control process of DDR3 RAM, FIFOs, and handshaking signals are implemented by an automatic state machine (ASM). At the same time, there is an extra FIFO for each channel, which saves the ADC data temporarily for further computations in Xilinx Kintex-7 FPGA or transferring to PC. We call this FIFO the second FIFO (figure 5).

In order to transfer the raw data to PC, in each trigger of the system, we implemented a high speed Ethernet interface with the rate of 1 Gbit/sec. We modified the Xilinx Ethernet IP core embedded in the Kintex-7 FPGA. To send the data packets through the Ethernet interface, we constructed an ASM to control the data flow and handshaking signals [6].

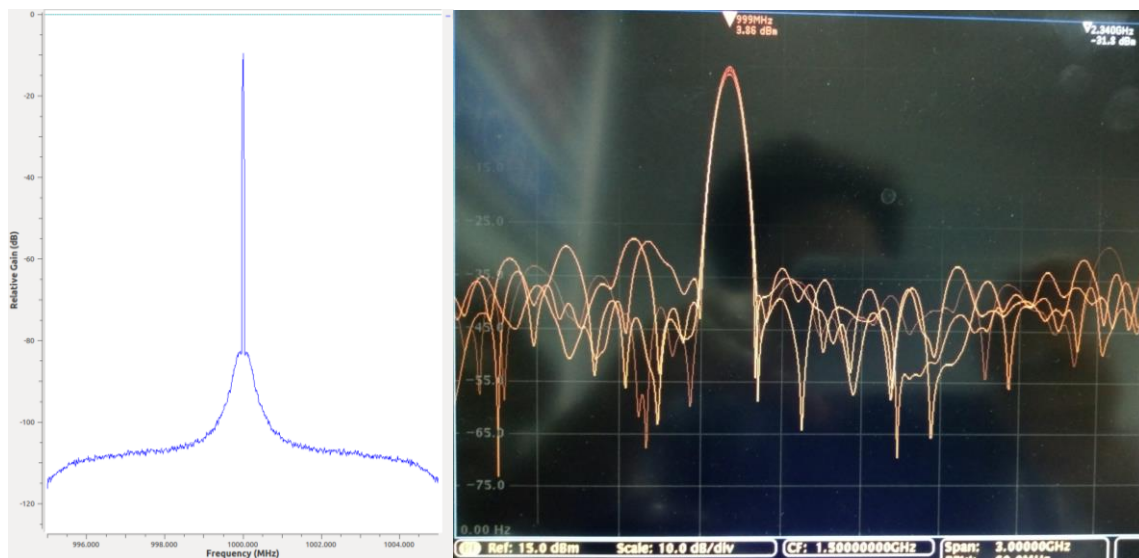


**Figure 5.** FPGA Raw Data Acquisition

To achieve an accurate transfer of data packets, first, the ASM copies the data of the first FIFO to the second FIFO and then assigns the header and end signs to each data packet. The ASM also controls the handshaking signals of the Ethernet IP core. In this protocol, PC operates on a master mode and it sends high level commands such as start recording, standby mode, readout command of board temperature and power supply voltages, readout command of voltage data of each channel, manual assignment of the initialization parameters of the digital attenuators, ADCs and clock distributor [7]. All the FPGA VHDL codes are compiled in the Vivado 2017.2 development software provided by Xilinx Company [8].

The output signal from the MKID, containing all the frequencies of the comb, is first split to two signals (I and Q), multiplied by the sine and cosine waves of the tone of interest and finally low pass filtered in order to keep only the lower side band of the signal. Then by using I and Q signal component we can measure amplitude ( $I^2 + Q^2$ ) and phase ( $\arctan(Q/I)$ ) of each transmitted tones.

FPGA DAQ test with synthetic signals produced by a fast synthesizer is show in figure 6. These pictures show 1 GHz signal that we could measure in PC (e.g., as measured data from MKIDs) and the oscilloscope shows the excitation signal produced by DAC in the electronic system. We can perform time domain multiplexing meaning we will excite MKIDs with different frequencies in specific determined time intervals (e.g., for 100 us, 1GHz at time=0, 1.1 GHz at time=100us, and so on). For fast processing, we need to do Frequency Domain Multiplexing (FDM) which we are working on. In FDM we add all frequencies and simultaneously send them to MKIDs.



**Figure 6.** FPGA Data Acquisition System Test

### Acknowledgement

We would like to thank Dr. Jonas Zmuidzinas for his support and encouragement. We would also like to thank Vipin for FPGA discussions and his helpful feedback about our firmware design.

### Conclusion

We have successfully implemented raw data acquisition from the MKID to PC with a high speed Ethernet interface (1Gbs and 10 Gbs). Digital readout system has many advantages over Vector Network Analyzer as it can provide more comprehensive data handling. In the future, we would like to improve the digital readout and make it faster with higher precision.

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